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70th ANNIVERSARY

2023 COMMEMORATIVE SUPPLEMENT to the DIGEST OF TECHNICAL PAPERS

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70th Anniversary

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Welcome

Welcome to the special ISSCC 2023 Commemorative Supplement celebrating the 70th Anniversary of the International Solid-State Circuits Conference (ISSCC).

The theme for ISSCC 2023 is *"Building on 70 Years of Innovation in Solid-State Circuit Design."* The integrated circuit (IC) design community has proven to be agile and resilient in a world scarred by the worldwide pandemic, and this year ISSCC commemorates the 70th anniversary of ISSCC with an edition that is more than ever focused on innovation. To enhance our lives and support increasingly more innovative developments, ISSCC promotes and shares new circuit ideas with potential to advance the state-of-the-art for IC design and to enable systems with ever-improving functionality and efficiency.

The Supplement includes an update of the ISSCC Author Honor Roll which was initiated on the occasion of the 50th Anniversary. Regrettably, two of its members are no longer with us: James Meindl (https://spectrum.ieee.org/remembering-the-career-of-microelectronics-pioneer-james-d-meindl) and David Hodges (https://engineering.berkeley.edu/news/2022/11/david-hodges-former-dean-of-engineering-and-pioneer-in-integrated-circuit-design-dies-at-85/). Also included in this Supplement are tables identifying the Conference leadership from North America, Asia, and Europe. Another table and associated graphs document the accepted papers by region over the history of ISSCC.

Yet another addition to this Anniversary Supplement, is an upgrade to what was first introduced for 2012 and presented then in the IEEE SSCS Magazine, "Through the Looking Glass: The 2023 Edition Trends in Solid-State Circuits from ISSCC".

Finally, the Supplement contains an updated article relating to the history of *"The Saratoga Group"*. This group is composed largely of graduate students from ECE, University of Toronto, who volunteer each year to help with speaker registration, presentation-slide corrections, operate the projection computers during the Conference, recording the live presentation and processing files for on-demand, amongst other tasks. The Saratoga Group began in 1990 with 8 members (all non students), and has evolved to be dominated by student volunteers to a number which is currently 25, including 20 students.

As at ISSCC 2003 and ISSCC 2013, the 2023 Anniversary includes some celebratory events: the top contributors from 70-years will be recognized during the Plenary Session; an anniversary cake will be unveiled and served at the Monday Social Hour; a special Tuesday Evening Panel will look at the *"What will be the Essential Skills for IC Designers in the Next Decade?"*; and each in-person attendee will receive a 70th Anniversary commemorative canvas bag.

In closing, we would like to thank all of those who contributed to this Supplement. Thanks are also due to the members of the 70th Anniversary Committee, which besides myself includes Steve Bonney, Anantha Chandraskasan, Dustin Dunwell, Jim Haslett, Brad Phillips, K. C. Smith, Piet Wambacq, and Melissa Widerkehr.

We hope you will enjoy this compilation of 70 years of excellence at ISSCC!

Laura Chizuko Fujino

Chair, ISSCC 70th Anniversary Committee

February 2023

70 Years of ISSCC Technical and General Chairs

Year	Technical Chair	Affiliation	City/State/County	General Chair	Affiliation	City/State/Country
1954	J. G. Linvill	Bell Labs		I. Wolf	RCA	
1955	H. E. Tompkins	Burroughs Corp.		D. Fink	Philco	
1956	H. Woll	RCA Labs	Princeton, NJ	G. L. Haller	General Electric	Syracuse, NY
1957	G. Royer	IBM	Poughkeepsie, NY	A. L. Samuel	IBM	
1958	R. Baker	MIT Lincoln Labs	Lexington, MA	J. H. Mulligan, Jr	New York Univ.	New York, NY
1959	A. P. Stern	General Electric	Syracuse, NY	J. Morton	Bell Labs	Murray Hill, NJ
1960	T. R. Finch	Bell Labs	Murray Hill, NJ	A. P Stern	General Electric	Syracuse, NY
1961	J. J. Suran	General Electric	Syracuse, NY	T. R. Finch	Bell Labs	Murray Hill, NJ
1962	R. B. Adler	MIT	Cambridge, MA	J. J. Suran	General Electric	Syracuse, NY
1963	S. K. Ghandhi	Philco Scientific Lab	Blue Bell, PA	F. H. Blecher	Bell Labs	Murray Hill, NJ
1964	P. B. Myers	Marietta Corp	Baltimore, MD	E. O. Johnson	RCA	Somerville, NJ
1965	G. B. Herzog	RCA Labs	Princeton, NJ	J. B. Angell	Stanford Univ.	Stanford, CA
1966	G. B. Herzog	RCA Labs	Princeton, NJ	J. D. Meindl	US Army Electronics Cmd.	Fort Monmouth, NJ
1967	R. H. Baker	MIT	Cambridge, MA	J. S. Mayo	Bell Labs	Holmdel, NJ
1968	R. L. Petritz	Texas Instruments	Dallas, TX	J. S. Mayo	Bell Labs	Whippany, NJ
1969	R. S. Engelbrecht	Bell Labs	Murray Hill, NS	J. D. Meindl	Stanford Univ.	Stanford, CA
1970	T. E. Bray	General Electric	Syracuse, NY	R. S Engelbrecht	Bell Labs	Holmdel, NJ
1971	R. R. Webster	Texas Instruments	Dallas, TX	J. A. Raper	General Electric	Syracuse, NY
1972	S. Triebwasser	IBM Research	Yorktown Heights, NY	R. R. Webster	Texas Instruments	Dallas, TX
1973	V. I. Johannes	Bell Labs	Holmdel, NJ	S. Triebwasser	IBM Research	Yorktown Heights, NY
1974	H. Sobol	Collins Radio	Dallas, TX	V. I. Johannes	Bell Labs	Holmdel, NJ
1975	W. D. Pricer	IBM	Essex Junction, VT	H. Sobol	Collins Radio	Dallas, TX
1976	J. H. Wuorinen	Bell Labs	Whippany, NJ	W. D. Pricer	IBM	Essex Junction, VT
1977	D. A. Hodges	Univ. of California	Berkeley, CA	J. H. Wuorinen	Bell Labs	Whippany, NJ
1978	J. D. Heightley	Sandia Labs	Albuquerque, NM	D. A. Hodges	Univ. of California	Berkeley, CA
1979	W. S. Kosonocky	RCA Labs	Princeton, NJ	J. D. Heightley	Sandia Labs	Albuquerque, NM
1980	J. D. Plummer	Stanford Univ.	Stanford, CA	J. A. Raper	General Electric	Syracuse, NY
1981	B. A. Wooley	Bell Labs	Holmdel, NJ	J. A. Raper	General Electric	Syracuse, NY
1982	P. R. Gray	Univ. of California	Berkeley, CA	J. A. Raper	General Electric	Syracuse, NY
1983	L. M. Terman	IBM Research	Yorktown Heights, NY	J. A. Raper	General Electric	Syracuse, NY
1984	P. W. Verhofstadt	Fairchild uProc. Div.	Mountain View, CA	J. A. Raper	General Electric	Syracuse, NY
1985	H. J. Boll	Bell Labs	Murray Hil, NJ	J. A. Raper	General Electric	Syracuse, NY
1986	A. Grebene	Micro Linear Corp	San Jose, CA	J. A. Raper	General Electric	Syracuse, NY
1987	R. Baertsch	General Electric	Schenectady, NY	J. A. Raper	General Electric	Syracuse, NY
1988	W. Herndon	Fairchild Research Ctr.	Palo Alto, CA	W. D. Pricer	IBM	Essex Junction, VT
1989	H. E. Mussman	AT&T Bell Labs	Naperville, IL	W. D. Pricer	IBM	Essex Junction, VT
1990	C. W. Gwyn	Sandia Labs	Albuquerque, NM	W. D. Pricer	IBM	Essex Junction, VT
1991	J. T. Trnka	IBM	Rochester, MN	W. D. Pricer	IBM	Essex Junction, VT
1992	A. R. Shah	Texas Instruments	Dallas, TX	W. D. Pricer	IBM	Essex Junction, VT
1993	R. C. Jaeger	Auburn Univ.	Auburn, AL	W. D. Pricer	IBM	Essex Junction, VT
1994	D. Monticelli	National Semiconductor	Santa Clara, CA	W. D. Pricer	IBM	Essex Junction, VT
1995	T. Tredwell	Eastman Kodak	Rochester, NY	W. D. Pricer	IBM	Essex Junction, VT
1996	F. W. Hewlett	Sandia Labs	Albuquerque, NM	W. D. Pricer	IBM	Essex Junction, VT
1997	R. K. Hester	Texas Instruments	Dallas, TX	J. T. Trnka	IBM	Rochester, MN
1998	J. Cressler	Auburn Univ.	Auburn, AL	J. T. Trnka	IBM	Rochester, MN
1999	S. S. Taylor	Triquent Semiconductor	Hillsboro, OR	J. T. Trnka	IBM	Rochester, MN
2000	R. Crisp	Rambus, Inc.	Mountain View, CA	J. T. Trnka	IBM	Rochester, MN
2001	G. Gulak	Univ. of Toronto	Toronto, Canada	J. T. Trnka	IBM	Rochester, MN
2002	W. Sansen	Katholieke Univ.	Leuven, Belgium	T. Tredwell	Eastman Kodak	Rochester, NY
2003	A. Chandrakasan	MIT	Cambridge, MA	T. Tredwell	Eastman Kodak	Rochester, NY
2004	A. Kanuma	Toshiba	Kawasaki, Japan	T. Tredwell	Eastman Kodak	Rochester, NY
2005	I. Young	Intel	Hillsboro, OR	T. Tredwell	Eastman Kodak	Rochester, NY
2006	J. Sevenhans	Consultant	Brasschaat, Belgium	T. Tredwell	Eastman Kodak	Rochester, NY
2007	J. Van der Spiegel	Univ. of Pennsylvania	Philadelphia, PA	T. Tredwell	Eastman Kodak	Rochester, NY
2008	Y. Hagihara	Sony	Atsugi City, Japan	T. Tredwell	Carestream Health	Rochester, NY
2009	W. Bowhill	Intel	Hudson, MA	T. Tredwell	Carestream Health	Rochester, NY
2010	A. Theuwissen	Harvest Imaging/Delft U.	Bree/Delft, Belgium	A. Chandrakasan	MIT	Cambridge, MA
2011	W. Gass	Texas Instruments	Dallas, TX	A. Chandrakasan	MIT	Cambridge, MA
2012	H. Hidaka	Renesas Electronics	Itami, Japan	A. Chandrakasan	MIT	Cambridge, MA
2013	B. Nauta	Univ. of Twente	Enschede, The Netherlands	A. Chandrakasan	MIT	Cambridge, MA
2014	T. Stetzler		Houston, TX	A. Chandrakasan	MIT	Cambridge, MA
2015	H.-J. Yoo	KAIST	Daejeon, Korea	A. Chandrakasan	MIT	Cambridge, MA
2016	K. Zhang	Intel	Hillsboro, OR	A. Chandrakasan	MIT	Cambridge, MA
2017	B. Murmann	Stanford University	Stanford, CA	A. Chandrakasan	MIT	Cambridge, MA
2018	A. Burdett	Sensium Healthcare	Oxfordshire, United Kingdom	A. Chandrakasan	MIT	Cambridge, MA
2019	E. Cantatore	Eindhoven Univ. of Tech.	Eindhoven, The Netherlands	J. van der Spiegel	Univ. of Pennsylvania	Philadelphia, PA
2020	U.-K. Moon	Oregon State Univ.	Corvallis, OR	J. van der Spiegel	Univ. of Pennsylvania	Philadelphia, PA
2021	M. Ikeda	University of Tokyo	Tokyo, Japan	K. Zhang	Taiwan Semiconductor	Hsinchu, Taiwan
2022	E. Beigné	Meta	Menlo Park, CA	K. Zhang	Taiwan Semiconductor	Hsinchu, Taiwan
2023	P. Wambacq	imec	Heverlee, Belgium	E. Cantatore	Eindhoven Univ. of Tech.	Eindhoven, The Netherlands

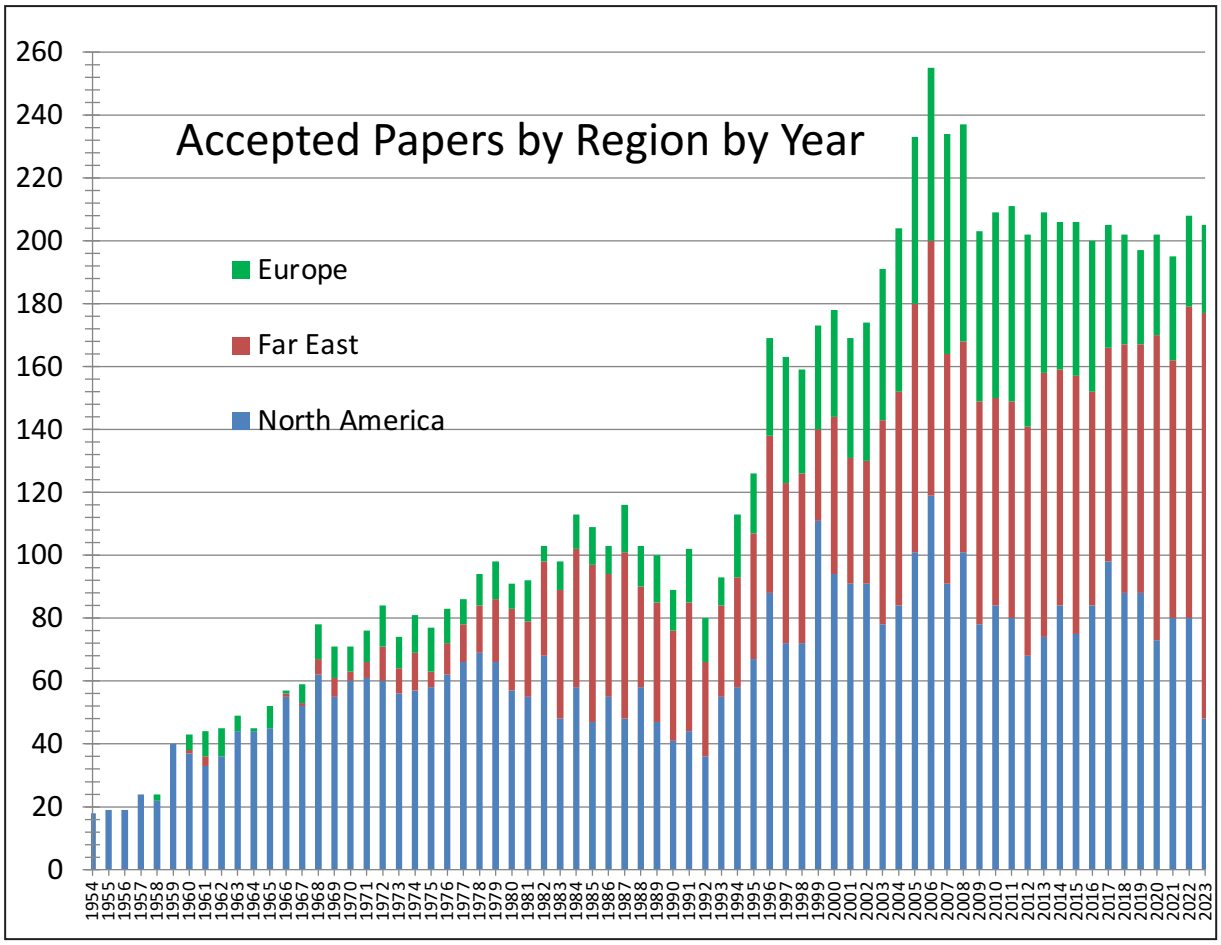
Far-East Chairs and Secretaries

Year	Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country	Asst. Sec.	Affiliation	City	Country
1971	**T. Sugano**	Univ. of Tokyo	Tokyo	Japan								
1972	**T. Sugano**	Univ. of Tokyo	Tokyo	Japan	**S. Hamada**	NTT	Tokyo	Japan				
1973	**S. Hamada**	NTT	Tokyo	Japan	**H. Mukai**	NTT	Tokyo	Japan				
1974	**S. Hamada**	NTT	Tokyo	Japan	**K. Kataoka**	NTT	Tokyo	Japan				
1975-1976	**Y. Tarui**	Electrotechnical Lab	Tokyo	Japan	**T. Sekigawa**	Electrotechnical Lab	Tokyo	Japan				
1977-1978	**M. Uenohara**	Nippon Elect. Co.	Kawasaki	Japan	**K. Ayaki**	Nippon Elect. Co.	Kawasaki	Japan				
1979	**M. Watanabe**	NTT	Tokyo	Japan	**K. Kataoka**	NTT	Tokyo	Japan				
1980	**M. Watanabe**	NTT	Tokyo	Japan	**K. Kurumada**	NTT	Tokyo	Japan				
1981-1982	**K. Kurokawa**	Fujitsu	Kawasaki	Japan	**H. Ishikawa**	Fujitsu	Tokyo	Japan				
1983-1984	**M. Nagata**	Hitachi CRL	Tokyo	Japan	**M. Kubo**	Hitachi CRL	Tokyo	Japan				
1985-1986	**Y. Takeishi**	Toshiba	Kawasaki	Japan	**Y. Nishi**	Toshiba	Kawasaki	Japan				
1987-1988	**H. Sasaki**	NEC	Kawasaki	Japan	**A. Morino**	NEC	Kawasaki	Japan				
1989-1990	**T. Sudo**	NTT	Atsugi	Japan	**S. Horiguchi**	NTT	Atsugi	Japan	**T. Wakimoto**	NTT	Atsugi	Japan
1991-1992	**T. Nakano**	Mitsubishi	Itami	Japan	**O. Tomisawa**	Mitsubishi	Itami	Japan	**K. Okada**	Mitsubishi	Itami	Japan
1993-1994	**H. Ishikawa**	Fujitsu	Atsugi	Japan	**S. Hijiya**	Fujitsu	Atsugi	Japan	**K. Yamashita**	Fujitsu	Atsugi	Japan
1995-1996	**G. Kano**	Matsushita	Osaka	Japan	**T. Baba**	Matsushita	Osaka	Japan	**S. Katsu**	Matsushita	Osaka	Japan
1997-1998	**M. Kubo**	Hitachi	Tokyo	Japan	**K. Shimohigashi**	Hitachi CRL	Tokyo	Japan	**K. Kimura**	Hitachi	Tokyo	Japan
1999-2000	**Y. Unno**	Toshiba	Yokohama-City	Japan	**A. Kanuma**	Toshiba	Kawasaki	Japan	**Y. Miyazawa**	Toshiba	Kawasaki	Japan
2001-2002	**H. Watanabe**	NEC	Kawasaki	Japan	**T. Arai**	NEC	Kawasaki	Japan	**M. Yamashina**	NEC	Sagamihara	Japan
2003	**Y. Hagiwara**	Sony	Atsugi	Japan	**M. Katakura**	Sony	Atsugi	Japan	**T. Yamazaki**	Sony Electronics	San Jose	CA-USA

Year	Chair	Affiliation	City	Country	Vice Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country	Asst. Sec.	Affiliation	City	Country
2004	**Y. Hagiwara**	Sony	Tokyo	Japan	**K. Iizuka**	Sharp	Nara	Japan	**J. Chung**	Pohang Univ. of Science & Tech.	Pohang	Korea				
2005-2006	**K. Iizuka**	Sharp	Nara	Japan	**J. Chung**	Pohang Univ. of Science & Tech.	Pohang	Korea	**T. Kawahara**	Hitachi	Tokyo	Japan				
2007	**J. Chung**	Pohang Univ. of Science & Tech.	Pohang	Korea	**T. Kawahara**	Hitachi	Tokyo	Japan	**S. Park**	Samsung	Yongin	Korea				
2008	**J. Chung**	Pohang Univ. of Science & Tech.	Pohang	Korea	**T. Kawahara**	Hitachi	Tokyo	Japan	**H-J. Yoo**	KAIST	Daejeon	Korea				
2009-2010	**T. Kawahara**	Hitachi	Tokyo	Japan	**H-J. Yoo**	KAIST	Daejeon	Korea	**M. Ikeda**	University of Tokyo	Tokyo	Japan				
2011	**H-J. Yoo**	KAIST	Daejeon	Korea	**M. Ikeda**	University of Tokyo	Tokyo	Japan	**M. Hamada**	Toshiba	Kawasaki	Japan				
2012	**H-J. Yoo**	KAIST	Daejeon	Korea	**M. Ikeda**	University of Tokyo	Tokyo	Japan	**K. Arimoto**	Renesas Elect	Itami	Japan				
2013	**M. Ikeda**	University of Tokyo	Tokyo	Japan	**K. Arimoto**	Okayama Pref. Univ.	Okayama	Japan	**J-Y. Lee**	Samsung	Yongin	Korea				
2014	**K. Arimoto**	Okayama Prefectural Univ.	Okayama	Japan	**J-Y. Lee**	Samsung	Yongin	Korea	**T-H. Lin**	National Taiwan Univ.	Taipei	Taiwan				
2015	**J-Y. Lee**	Samsung	Yongin	Korea	**T-H. Lin**	National Taiwan Univ.	Taipei	Taiwan	**A. Inoue**	Fujitsu	Kawasaki	Japan				
2016	**T-H. Lin**	National Taiwan Univ.	Taipei	Taiwan	**A. Inoue**	Fujitsu	Kawasaki	Japan	**S. Choi**	SK Hynix Semiconductor	Icheon	Korea				
2017	**A. Inoue**	Fujitsu	Kawasaki	Japan	**S. Choi**	SK Hynix Semiconductor	Icheon	Korea	**T-C. Lee**	National Taiwan Univ.	Taipei	Taiwan				
2018	**S. Choi**	SK Hynix Semiconductor	Icheon	Korea	**T-C. Lee**	National Taiwan Univ.	Taipei	Taiwan	**M. Takamiya**	University of Tokyo	Tokyo	Japan				
2019	**T-C. Lee**	National Taiwan Univ.	Taipei	Taiwan	**M. Takamiya**	University of Tokyo	Tokyo	Japan	**L. Yan**	Samsung Electronics	Hwaseong	Korea				
2020	**M. Takamiya**	University of Tokyo	Tokyo	Japan	**L. Yan**	Samsung Electronics	Hwaseong	Korea	**Y-S. Shu**	Mediatek	Hsinchu	Taiwan				
2021	**L. Yan**	Samsung Electronics	Hwaseong	Korea	**Y-S. Shu**	Mediatek	Hsinchu	Taiwan	**J. Deguchi**	Kioxia	Kawasaki	Japan	**M-K. Law**	University of Macau	Taipa, Macau	China
2022	**Y-S. Shu**	Mediatek	Hsinchu	Taiwan	**J. Deguchi**	Kioxia	Kawasaki	Japan	**M-K. Law**	University of Macau	Taipa, Macau	China	**J. Choi**	KAIST	Daejeon	Korea
2023	**J. Deguchi**	Kioxia	Kawasaki	Japan	**M-K. Law**	University of Macau	Taipa, Macau	China	**J. Choi**	KAIST	Daejeon	Korea	**W-Z. Chen**	National Yang Ming Chiao Tung University	Hsinchu	Taiwan

European Chairs and Secretaries

Year	Chair	Affiliation	City	Country	Vice Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country
1971-1972	**J. C. van Vessem**	Philips	Nijmegen	The Netherlands					**O. Folberth**	IBM	Boeblingen	Germany
1973-1974	**J. C. van Vessem**	Philips	Nijmegen	The Netherlands					**H. Ruechardt**	Siemens	Munich	Germany
1975	**O. Folberth**	IBM	Boeblingen	Germany					**H. Ruechardt**	Siemens	Munich	Germany
1976	**O. Folberth**	IBM	Boeblingen	Germany					**O. W. Memelink**	Tech. Hogeschool Twente	Enschede	The Netherlands
1977-1978	**N. C de Troye**	Philips Research	Eindhoven	The Netherlands					**S. S. Roy**	Inter. Computers, Ltd	Manchester	England
1979	**N. C de Troye**	Philips Research	Eindhoven	The Netherlands					**W. Engl**	Tech. Hochschule Aachen	Aachen	Germany
1980-1983	**H. H. Berger**	IBM	Boeblingen	Germany					**P. Jespers**	Katholieke Univ.	Louvain	Belgium
1984-1985	**J. Borel**	Thomson EFCIS	Grenoble	France					**P. Schouter**	Thomson-CSF	St. Egreve	France
1986-1988	**J. Lohstroh**	Philips Research	Eindhoven	The Netherlands					**J. Danneels**	Bell Telephone	Antwerp	Belgium
1989-1994	**K. Hoffman**	Univ. der Bundeswehr	Neubiberg	Germany					**R. van de Plassche**	Philips Research	Eindhoven	The Netherlands
1995-1996	**R. van de Plassche**	Philips Research	Eindhoven	The Netherlands					**M. Degrauwe**	CSEM	Neuchatel	Switzerland
1997-2000	**R. van de Plassche**	Philips Research	Eindhoven	The Netherlands					**W. Sansen**	Katholieke Univ.	Leuven	Belgium
2001	**R. van de Plassche**	Philips Research	Eindhoven	The Netherlands					**J. Sevenhans**	Alcatel	Antwerpen	Belgium
2002	**R. van de Plassche**	Philips Research	Eindhoven	The Netherlands	**J. Sevenhans**	Alcatel	Antwerpen	Belgium	**A. Theuwissen**	Philips Semicond.	Eindhoven	The Netherlands
2003	**J. Sevenhans**	Alcatel	Antwerpen	Belgium	**A. Theuwissen**	Philips Semicond.	Eindhoven	The Netherlands	**R. Koch**	Infineon Technologies	Munchen	Germany
2004	**J. Sevenhans**	LEA Asics of Broadband	Antwerpen	Belgium	**A. Theuwissen**	DALSA BV	Eindhoven	The Netherlands	**R. Koch**	Infineon Technologies	Munchen	Germany
2005-2006	**A. Theuwissen**	DALSA BV	Eindhoven	The Netherlands	**R. Koch**	Infineon Technologies	Munchen	Germany	**Q. Huang**	ETH Zurich	Zurich	Switzerland
2007-2008	**R. Koch**	Infineon Technologies	Munchen	Germany	**Q. Huang**	ETH Zurich	Zurich	Switzerland	**B. Nauta**	Univ. Twente	Twente	The Netherlands
2009	**Q. Huang**	ETH Zurich	Zurich	Switzerland	**B. Nauta**	Univ. Twente	Twente	The Netherlands	**A. Baschirotto**	Univ. of Milan-Bicocca	Milano	Italy
2010	**Q. Huang**	ETH Zurich	Zurich	Switzerland	**B. Nauta**	Univ. Twente	Twente	The Netherlands	**A. Pärssinen**	Nokia	Helsinki	Finland
2011	**B. Nauta**	Univ. Twente	Twente	The Netherlands	**A. Pärssinen**	Nokia	Helsinki	Finland	**E. Cantatore**	Eindhoven Univ. of Tech.	Eindhoven	The Netherlands
2012-2013	**A. Pärssinen**	Renesas Mobile	Helsinki	Finland	**E. Cantatore**	Eindhoven Univ. of Tech.	Eindhoven	The Netherlands	**A. Burdett**	Toumaz Technology	Abingdon	United Kindom
2014	**A. Burdett**	Toumaz Microsystems	Abingdon	United Kindom	**M. Ortmanns**	University of Ulm	Ulm	Germany	**M. Ortmanns**	University of Ulm	Ulm	Germany
2015	**A. Burdett**	Toumaz Microsystems	Abingdon	United Kindom	**M. Ortmanns**	University of Ulm	Ulm	Germany	**D. Stoppa**	Fondazione Bruno Kessler	Trento	Italy
2016	**M. Ortmanns**	University of Ulm	Ulm	Germany	**D. Stoppa**	Fondazione Bruno Kessler	Trento	Italy	**M. Verhelst**	KU Leuven	Heverlee	Belgium
2017	**D. Stoppa**	Fondazione Bruno Kessler	Trento	Italy	**M. Verhelst**	KU Leuven	Heverlee	Belgium	**K. Doris**	NXP	Eindhoven	The Netherlands
2018	**M. Verhelst**	KU Leuven	Heverlee	Belgium	**K. Doris**	NXP	Eindhoven	The Netherlands	**Y. Manoli**	University of Freiburg - IMTEK	Freiburg	Germany
2019	**K. Doris**	NXP	Eindhoven	The Netherlands	**Y. Manoli**	University of Freiburg IMTEK	Freiburg	Germany	**T. Piessens**	Icsense	Leuven	Belgium
2020	**Y. Manoli**	University of Freiburg - IMTEK	Freiburg	Germany	**T. Piessens**	Icsense	Leuven	Belgium	**B. Rae**	ST Microelectronics	Edinburgh	United Kindom
2021	**T. Piessens**	Icsense	Leuven	Belgium	**B. Rae**	ST Microelectronics	Edinburgh	United Kindom	**B. Wicht**	University of Hannover	Hannover	Germany
2022	**B. Rae**	ST Microelectronics	Edinburgh	United Kindom	**B. Wicht**	University of Hannover	Hannover	Germany	**M. Bassi**	Infineon Technologies	Villach	Austria
2023	**B. Rae**	ST Microelectronics	Edinburgh	United Kindom	**M. Bassi**	Infineon Technologies	Villach	Austria	**V. Schaffer**	Texas Instruments	Freising	Germany



70 Years of Paper History by Region

Year	America	Far East	Europe	Year	America	Far East	Europe	Year	America	Far East	Europe
1954	18	0	0	1978	69	15	10	2002	91	39	44
1955	19	0	0	1979	66	20	12	2003	78	65	48
1956	19	0	0	1980	57	26	8	2004	84	68	52
1957	24	0	0	1981	55	24	13	2005	101	79	53
1958	22	0	2	1982	68	30	5	2006	119	81	55
1959	40	0	0	1983	48	41	9	2007	91	73	70
1960	37	1	5	1984	58	44	11	2008	101	67	69
1961	33	3	8	1985	47	50	12	2009	78	71	54
1962	36	0	9	1986	55	39	9	2010	84	66	59
1963	44	0	5	1987	48	53	15	2011	80	69	62
1964	44	0	1	1988	58	32	13	2012	68	73	61
1965	45	0	7	1989	47	38	15	2013	74	84	51
1966	55	1	1	1990	41	35	13	2014	84	75	47
1967	52	1	6	1991	44	41	17	2015	75	82	49
1968	62	5	11	1992	36	30	14	2016	84	68	48
1969	55	6	10	1993	55	29	9	2017	98	68	39
1970	60	3	8	1994	58	35	20	2018	88	79	35
1971	61	5	10	1995	67	40	19	2019	88	79	30
1972	60	11	13	1996	88	50	31	2020	73	97	32
1973	56	8	10	1997	72	51	40	2021	80	82	33
1974	57	12	12	1998	72	54	33	2022	80	99	29
1975	58	5	14	1999	111	29	33	2023	48	129	28
1976	62	10	11	2000	94	50	34				
1977	66	12	8	2001	91	40	38				

Data Compiled by: John Trnka and Brad Phillips

Through the Looking Glass – The 2023 Edition

Trends in solid-state circuits from ISSCC

Shahriar Mirabbasi, Laura C. Fujino, and Kenneth C. Smith

***Abstract*— The International Solid-State Circuits Conference (ISSCC) is the flagship conference of the IEEE Solid-State Circuits Society. The theme for ISSCC 2023 is "Building on 70 Years of Innovation in Solid-State Circuit Design." The integrated circuit (IC) design community has proven to be agile and resilient in a world scarred by the worldwide pandemic, and this year's ISSCC commemorates the 70th anniversary of ISSCC with an edition that is more than ever focused on innovation. To enhance our lives and support increasingly more innovative developments, ISSCC promotes and shares new circuit ideas with potential to advance the state-of-the-art for IC design and to enable systems with ever-improving functionality and efficiency.**

ISSCC covers a spectrum of design approaches in various technical areas and advances, broadly categorized as analog systems, power management, analog-to-digital data conversion, communication systems, digital systems (including machine learning and artificial intelligence (AI)), and memory. It also covers innovative topics such as imagers, sensors, quantum technologies, and biomedical devices, including forward-looking solutions that may be several years away from becoming commercialized.

The 12 ISSCC technical subcommittees annually update their analysis of industry trends for the benefit of the community at large. This article summarizes some of these views in selected technical areas.

Analog Systems

Subcommittee Chair: Maurits Ortmanns, University of Ulm
Institute of Microelectronics, Ulm, Baden-Württemberg, Germany

At ISSCC 2023, new analog circuit techniques for advancing the performance of amplifiers, oscillators, and sensor interfaces continue to emerge.

Despite their high maturity, Class-D amplifiers continue to advance in performance, thanks to new creative solutions revealed in this year's papers. A capacitively-coupled chopper Class-D amplifier with digital input combines feedback after the output filter with other techniques to achieve the highest dynamic range (DR), >120dB. A chopper-stabilized amplifier uses a relaxed fill-in technique to reduce the interaction between the input signal and the chopper clock that causes IMD. The reduced input switching activity results in 25× less input current and a 15% power saving, achieved by power-cycling the fill-in OTA.

In the sensor area, significant advances are made as well. A shunt-based current sensor uses a calibration scheme based on an accurate on-chip current source to achieve ±0.2% gain error over 40°C to 125°C. Magnetic current sensors are widely used in applications where galvanic isolation and wide bandwidth (BW) are desired. By using Hall plates for low frequencies and pick-up coils for high frequencies, a hybrid magnetic sensor achieves high resolution over a wide frequency range, ±1.1% gain flatness, and significantly improved energy efficiency over previous designs.

Other papers describe significant advances in Integrated stress sensors, and temperature sensors. Bipolar junction transistor (BJT)-based high-accuracy temperature sensors with only 1 point trim are demonstrated by using capacitive biasing and continuous-time current-mode readout techniques, achieving 0.34pJ·K^2 resolution figure of merit (FoM) with sub-1V supply and 0.85pJ·K^2 resolution FoM with 3σ inaccuracy of ±0.1°C, respectively (Figure 1), and both sensors cover the military temperature range.

Significant advances in the aging resilience of RC frequency references and the startup time and energy of crystal oscillators (XOs) are also disclosed. By periodically locking to a less-aged reference oscillator, an RC oscillator achieves ±1030ppm frequency inaccuracy from 40°C to 85°C after accelerated aging for 500 hours at 125°C. XOs reduce startup time and improve energy efficiency with new schemes that expand the tolerable injection frequency error up to 10,000ppm. A BAW-based oscillator uses a new divider to achieve a frequency stability of ±4ppm and jitter of <90fs.

Power Management

Subcommittee Chair: Bernhard Wicht
Leibniz University, Hannover, Germany

Power management supports a diverse application space with a range of requirements coming from automotive, computing, communications, biomedical, consumer and other applications. Some systems may operate at less than 1V, but draw energy from a high-voltage supply, others may draw power from low-voltage batteries, however, require hundreds of volts to kV to operate; some systems must respond to near-instantaneous changes in voltage and current levels; some require extreme reliability and careful design to minimize electromagnetic interference (EMI); some must transfer power and/or signals across isolation boundaries, and yet others must efficiently process and recover energy from intermittent low-power transducers. Thus, while there is no single figure of merit for the wide scope of power management systems and technologies, most of them strive to achieve high performance, minimal power loss, small size, and low cost.

Trends seen at this year's ISSCC align with the growing diversity of applications and goals outlined above. Power-conversion topologies continue to evolve, many leveraging hybrid architectures that mix switched-capacitor (SC) architectures with inductor(s). A number of these topologies focus on multiple-output designs, some using single-inductor multiple-output (SIMO) techniques, others using shared- or multi-stage designs. There are a variety of efforts to address key challenges in hybrid designs such as balancing flying capacitors and achieving safe startup, as well as other efforts to improve voltage regulation and transient response.

This year we have seen growth in universal serial bus (USB) and computing power delivery with a number of designs addressing challenging aspects (cost, density, transient response) of these applications. Among USB-focused designs, some leverage the USB cable inductances as passive energy storage elements to improve these metrics and reduce heat generated in the system battery chargers while providing bi-directional operation. Some designs focus on compute power delivery and work to

place a final power-conversion stage close to the load using a vertical power-delivery concept. In power delivery for computing applications, the use of high switching frequencies and meeting strict transient requirements remain a core objective and a key challenge, respectively.

Gallium nitride (GaN) designs are expanding in scope and demonstrating higher levels of integration for high-voltage and automotive applications. This year, we have seen an increase in the complexity and feature set of monolithic GaN designs with new analog circuit concepts providing functionalities that previously were reserved for silicon-only designs. There are new concepts in gate driving for GaN and SiC which achieve high common-mode transient immunity (CMTI) and provide adaptive switching for improved performance, as well as spread-spectrum techniques to reduce EMI. Additional concepts include gate drive signaling across (up to 20kV) galvanic-isolation barriers which are also subject to high dV/dt transients. GaN-based power conversion designs include high conversion ratio, bidirectional buck-boost and flyback topologies.

Other areas of focus at ISSCC 2023 include wireless power transfer (WPT) and energy harvesting. In particular, energy-harvesting techniques such as bias-flip piezoelectric, multi-source harvesting, and maximum power-point tracking (MPPT) are explored in several papers. Wireless power transfer papers include techniques for foreign object detection and methods to improve the spatial distribution of electromagnetic energy using multi-path transmitters. Other concepts such as new receivers and rectifiers with adaptive zero-current switching (ZCS) and hybrid techniques, some pushing to very high operation frequencies, are also explored.

Data Converters

Subcommittee Chair: Jan Westra
Broadcom, Bunnik, The Netherlands

Data converters are a critical link between the analog physical world and the world of digital computing and signal processing, prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and linearity while continuing to increase power efficiency. This year, ISSCC not only continues the trend of reporting highly energy-efficient analog-to-digital converters (ADCs), but also showcases new and exciting converter architectures, which opens new possibilities for data conversion.

Time-based quantization and hybrid pipelined-SAR architectures are expanding the speed limits of the current state-of-the-art in Nyquist converter design, while incremental converters are reaching new levels of efficiency. In noise-shaping converter design, delta-sigma and noise-shaping-SAR converters are continuing their prominent role and show their strengths in both high-efficiency, as well as high-speed data conversion. Various types of dynamic amplifiers such as ring-amp and floating inverter amplifiers are one of the key aspects in pushing the limit of power efficiency in these architectures.

Figures 2, 3, and 4 represent traditional metrics that capture the innovative progress in ADC design. Figure 2 plots power dissipated relative to the Nyquist sampling rate (P/f_{snyq}), as a function of signal-to-noise-and-distortion ratio (SNDR), to give a measure of ADC power efficiency. Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 1fJ/conversion-step. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of the signal-to-noise ratio, represented by the solid line. Designs published from 1997 to 2022 are shown in circles. ISSCC 2023 designs are shown in red stars.

Figure 3 plots signal fidelity versus the Nyquist sampling rate normalized to power consumption. At low sampling rates, converters tend to be limited by thermal and flicker noises, independent of the sample rate. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner, indicated by the roll-off vs. frequency in the dashed line. The last ten years have resulted in an improvement of over 10dB in power-normalized signal fidelity, or a 10× improvement in speed for the same normalized signal fidelity. At ISSCC this year, hybrid pipelined-SAR and noise-shaping SARs are continuing the trends in the speed vs efficiency corner of the graph. Time-based conversion of signal and time-domain quantization are becoming an integral part of converters in scaled nodes. Time-interleaving multiple channels with error correction over process, voltage and temperature (PVT) as well as clock skew between channels is a necessity in these architectures to achieve robust performance in high-speed conversion rates.

Figure 4 plots ADC bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. While ten years ago, a state-of-the-art data converter showed an aperture error of approximately $1ps_{rms}$, in recent years, designs with aperture errors below $100fs_{rms}$ have been published, many of which have been published at ISSCC.

Finally, this year's ISSCC presents multiple time-assisted data converters with over gigahertz sampling speed with extremely power- and area-efficient implementations.

Finally, this year's ISSCC presents two converters advancing the state-of-the-art in incremental converter design, showing the strength of this architecture for extremely efficient and very small converters required for IoT applications.

Communication Systems: Radio-Frequency Subcommittee

Subcommittee Chair: Jan Craninckx
imec, Leuven, Belgium

ISSCC 2023 features record-setting advancements in phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), RF transceiver building blocks, and THz signal generation driven by emerging requirements in 5G and 6G communications, the Internet of Things (IoT), radars, and imaging at RF, mm-wave, and THz frequencies. This document highlights such trends that will be presented at ISSCC 2023.

Frequency Generation: ISSCC 2023 highlights new results in voltage-controlled oscillators (VCOs) and features several approaches that demonstrate better-than 190dBc/Hz FoMs. First, a Class-F VCO with inherent common-mode-noise self-cancelation and isolation achieves 192.8dBc/Hz FoM at 1MHz offset. Second, an ~26GHz dual-path synchronized quad-core oscillator with a 193.3dBc/Hz FoM at 10MHz offset is reported. Third, 25-to-30GHz 4- and 20-core VCOs achieving a 193.3dBc/Hz FoM at 1MHz offset are introduced. Finally, a W-band 3rd-harmonic-extraction VCO employing a multi-resonance/core/mode technique is demonstrated with excellent phase-noise-FoM balance and a 21% tuning range.

ISSCC 2023 also introduces new PLL concepts for generating RF, microwave, and mm-wave frequency carriers with several record-setting low-jitter and low-power-consumption prototypes that ultimately push the jitter-power FoM below -250dB as shown in Figure 5. A 16GHz charge-pump PLL-based FMCW synthesizer is presented with robust duty-cycled operation achieving 1.5GHz modulation bandwidth and 41kHz rms error with below 1µs re-lock time. A 0.6-to-7.7GHz LO generator achieves 135fs rms jitter using a single LC-VCO-based Subsampling PLL with a ring-oscillator-based sub-integer-N frequency multiplier. A 9-to-11GHz fractional-N digital PLL is discussed with inverse-constant-slope DTC and FCW subtractive dithering technique. A 2.4GHz fractional-N PLL, which operates from a 32kHz reference clock and employs nonuniform-timing reference oversampling, is demonstrated with 3.94ps rms jitter. A 9.25GHz bang-bang digital PLL employs a novel multi-DTC topology with phase-shifted quantization-error sequences and achieves -60.3dBc in-band fractional spur and $77fs_{rms}$ jitter. A W-band PLL employing a novel power-gating injection-locked frequency-multiplier-based phase detector reports $47fs_{rms}$ jitter and a 253dB FoM. Finally, a 2.4GHz ultra-low-voltage subsampling PLL operating from a 0.4V supply achieves 236fs rms jitter, 76.1dBc reference spur, and 253dB FoM. These integer-N and fractional-N PLLs continue to improve power consumption and integrated jitter to keep pace with advances in communications and sensing applications.

RF Transceiver Building Blocks: ISSCC 2023 will introduce several exciting developments in circuits applicable to GHz and mm-wave transceivers. These developments represent new benchmarks in output power and bandwidth. A quadrature digital power amplifier with eight-way power combining using IQ-reuse and Doherty techniques achieves 4.1W (36.1dBm) peak P_{out} and 33.6% peak PAE at 2.9GHz in 28nm bulk CMOS. The PA achieves the peak RF-output-power 1dB bandwidth from 2.6 to 3.2GHz and a peak PAE of more than 30% from 2.7 to 3.2GHz. A broadband mm-wave power amplifier uses asynchronously tuned coupled-resonator output match and adaptive feedback linearization to achieve 19.7-to-43.8GHz 3dB gain bandwidth and demonstrates linear performance with 5G NR FR2 waveforms from 24.24 to 43.5GHz. An E-band LNA evolves the noise-cancelling LNA with an asymmetric compensation transformer and a hybrid-phase combiner to exhibit 4.8-to-6.5dB noise figures across 70 to 86GHz in 40nm CMOS while consuming 25mW. A 4b RFDAC combined with direct-digital frequency synthesis demonstrates the generation of 4GHz-bandwidth FMCW chirps from 5 to 9GHz in 28nm CMOS with a maximum chirp slope of 800MHz/µs. An N-path filter is also presented with the center frequency tunable across 1 to 5GHz, supporting a 5-to-80MHz bandwidth, and achieving +23dBM IIP3 using a charge-pump-based clock booster and embedded frequency translation.

THz Signal Generation: ISSCC 2023 features three new contributions in signal generation from 200 to 689GHz. These developments improve peak output power, efficiency, phase noise, and tuning range. A 65nm CMOS lensless THz source radiates up to 9.1dBm output power at 675GHz from a 12×12 array while supporting a +/-45-degree H-plane beam steering, the frequency tuning range of 6.9%, and a peak DC-to-THz efficiency of 0.245%. Also, implemented in 65nm CMOS, a cascade of 2 subsampling PLLs and an H-band frequency doubler are used to generate 264 to 287GHz from a 940MHz reference. The D-band subsampling PLL adopts a dual path subsampling phase detector and achieves $75fs_{rms}$ jitter while exhibiting -2.5dBm output power and an 8.38% tuning range. A broadband frequency doubler in 0.13µm SiGe BiCMOS uses a slotline-based transformer at the doubler input to achieve output frequency range from 200 to 350GHz, output power between 1.1 and 4.7dBm, and the peak DC-to-RF efficiency of 1.13%.

Communication Systems: Wireless Subcommittee

Subcommittee Chair: Chih-Ming Hung
MediaTek, Taipei, Taiwan

Ultra-low-power (ULP) receivers have continued to make dramatic improvements that facilitate their widespread adoption. Selectivity, or interference rejection, is a critical metric for all receivers that operate in the presence of other incumbent transmitters. As the RF spectrum becomes more crowded, adequate SIR (signal-to-interference ratio), adjacent channel rejection (ACR), and IRR (image-rejection ratio) for heterodyne receivers are essential for scaling the number of users that can concurrently occupy a band. Figure 6 illustrates how recently published ULP receivers have steadily advanced this metric so that ULP receivers are now competitive with main connectivity radios such as WiFi and Bluetooth.

ISSCCC 2023 in particular has seen an increase in the number of papers published in UWB and back-scatter transceivers. UWB, which has seen a resurgence recently, has the benefit of exceptional energy-per-bit, ability to achieve high data-rate at low power, and accurate ranging for use in asset tracking or tags. Back-scatter communication is used for communication with passive tags, eliminating the need for a battery. This year the first passive Bluetooth tag using back-scatter was published at ISSCC, demonstrating communication to a tablet with no battery in the tag.

The continuing demand for higher wireless data-rates in the context of mobile battery limitations drives the high-throughput and power-efficient transceiver development at mm-wave and sub-THz bands. Wireless transceivers continue to evolve with a higher level integration and more blocker tolerance. This year at ISSCC 2023, implemented in a 22nm FinFET technology, a 140GHz fully integrated receiver consisting of a PLL and a 16GHz ADC achieves a data-rate of 128Gb/s and consumes only 246mW. Additionally, for the blocker-rich sub-6GHz band, a receiver with harmonic-reject N-path-filter/mixer topology able to handle the 3rd and the 5th harmonic blockers as large as 10dBm and 4dBm, respectively was demonstrated with less than 1dB compression.

Figure 7 shows the trend of energy efficiency for mm-wave (<100GHz) and sub-THz (>100GHz) receivers presented at ISSCC. A receiver presented at ISSCC 2023 leverages a low-noise quadrature PLL, a frequency tripler and energy-efficient time-interleaved ADCs to demonstrate <1.95pJ/b system efficiency and < 1pJ/b receiver front-end efficiency while achieving 160Gb/s with the front-end.

Communication Systems: Wireline Subcommittee

Subcommittee Chair: Yohan Frans
AMD, San Jose, California

Over the past few decades, electrical and optical interconnects have been key components bridging the gap between the exponentially growing demand for data bandwidth across electronic systems and the relatively gradual increase in pin/cable density. Ranging from handheld electronics to supercomputers, wireline data bandwidth must also grow exponentially to avoid limiting the performance scaling of these systems. By increasing the data per pin or cable of various electronic devices and systems, such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN, wireline I/O has fueled incredible technological innovation in electronic devices and systems for decades.

Figure 8 shows that data rate per pin has approximately doubled every four years across various I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 9 shows that the data rates for published transceivers have kept pace with these standards while taking advantage of CMOS scaling. Figure 10 shows published transceiver energy efficiency vs. channel losses at the Nyquist frequency in the 40-to-50dB range. In part, this incredible improvement is enabled by the power-performance benefits of process technology scaling. However, sustaining this exponential trend for I/O bandwidth requires more than just transistor scaling. Significant advances in energy efficiency, channel equalization and clocking must be made to enable the next generation of low-power and high-performance computing systems. Papers at ISSCC this year include examples of long-reach PAM-4 copper interconnect transceivers operating up to 112Gb/s with and without ADC+DSP equalization architectures. These include:

1. A PAM-4 medium-reach electrical receiver operating at 200Gb/s with a continuous-time FFE.
2. A PAM-8 short-reach electrical transmitter operating up to 100Gb/s.
3. A 32Gb/s die-to-die chiplet NRZ transceiver with high beachfront density
4. An NRZ WDM receiver module using 7 wavelengths and 50Gb/s/wavelength to achieve 350Gb/s aggregate throughput.
5. A PAM-4 optical receiver operating at up to 106.25Gb/s
6. A short-reach optical coherent receiver operating up to 24Gb/s.

New techniques for extending data rate, power reduction, channel equalization, and clock recovery are reported. These transceivers and building blocks are implemented in CMOS technology.

Scaling Electrical Interconnects to 100Gb/s and Reaching Out to >200Gb/s: Bandwidth requirements in data centers and telecommunication infrastructure continue to drive the demand for ultra-high-speed wireline communication. Recently, complete transceivers operating up to 112Gb/s were demonstrated across a long-reach copper channel with >45dB loss. Two notable trends in these transceivers, especially for long-reach channels, are the adoption of PAM-4 modulation and a transition to DAC/ADC architectures with DSP-based equalization. Although PAM-4 provides twice the data rate at the same baud rate as conventional NRZ to relax channel loss requirements for bandwidth doubling, it also comes with more stringent requirements for linearity and noise. This trend has motivated the development of low-power data converters, digital equalization and clock recovery along with linear, high-bandwidth TX and RX analog front ends. This year, ISSCC includes two implementations of 112Gb/s PAM-4 long-reach transceivers with low power consumption. In Paper 6.1, Broadcom demonstrates a non-ADC/DSP transceiver in 7nm CMOS for a wide range of data rates up to 112Gb/s for long-reach copper interconnects consuming 690mW for a channel with 43dB loss. In Paper 6.2, MediaTek presents an ADC/DSP-based 112Gb/s PAM-4 long-reach transceiver in 5nm CMOS operating over a 48dB loss channel consuming 521mW. In Paper 6.3, Peking University describes a 200Gb/s 5-tap coplanar-waveguide distributed-tap receiver FFE in 28nm CMOS. In Papers 6.5 and 6.6, MediaTek and Korea University demonstrate low power and fast-frequency-acquisition CDR architectures operating at 32Gb/s and 52Gb/s, respectively. In Paper 6.7, Peking University describes a 128Gb/s PAM-4 transmitter with improved transitions between non-adjacent levels. In Paper 6.8, Hanyang University demonstrates a 100Gb/s PAM-8 transmitter with 3-tap shuffler FFE in 40nm CMOS yielding an output swing up to $1.6V_{ppd}$.

In-Package Links for Chiplet Communications: As a consequence of the increasing demand for bandwidth in high-throughput systems used in AI, HPC and switch applications, multiple devices are integrated in the same package, and data is sent between chiplets on the same interposer. For these 2.5D package applications, relatively short distances have to be bridged with minimum power while targeting the highest possible throughput per millimeter of chip-edge (Gb/s/mm). Since channel attenuation and discontinuities in these links are mild, low-power analog-oriented equalization and forwarded clock architectures are adequate. In Paper 6.4, Samsung presents a 32Gb/s per lane NRZ XSR transceiver in 4nm CMOS achieving 8Tb/s/mm beach-front bandwidth density while consuming only 0.44pJ/b. It operates over 3mm silicon interposer signal traces, which are shielded against crosstalk.

Optical Links for Upcoming 400G Data Center Interconnects: The explosive growth of data and data-centric computing places stringent demands on the bandwidth and energy efficiency of data center interconnects, spurring the development of several 200-to-400G Ethernet standards. Low-power data converters and optical integration are the two key components for the development of high-performance optical pluggable modules using coherent detection. In Paper 12.1, AMD demonstrates an NRZ WDM receiver module with 350Gb/s aggregate data rate and bit-error rate (BER) without forward error correction. This design has 7 wavelengths in a fiber, with 1.5nm color spacing, and runs at 50Gb/s per wavelength. The module incorporates stacked 7nm CMOS and 45nm silicon photonic dies. It uses an array of thermally tuned cascaded ring resonators to distinguish laser colors. High sensitivity (11.1dBm median) was measured under 0.96pJ/b energy efficiency. In Paper 12.2, Cisco Systems and University of Illinois Urbana-Champaign demonstrate a differential TIA in an optical 106.25Gb/s PAM-4 receiver with asymmetric signal paths utilizing currents from both terminals of the PD to improve SNR, resulting in an optical sensitivity of 14dBm. In Paper 12.3, University of Illinois Urbana-Champaign reports a CDR of a 24Gb/s QPSK coherent optical link in 28nm. It applies 16-phase switched-inverter-based harmonic-rejection-mixers to achieve low CDR latency.

Concluding Remarks: Continuing to aggressively scale I/O bandwidth is essential for the industry, but the tradeoffs between bandwidth, power, area, cost and reliability are extremely challenging. Advances in circuit architecture, interconnect topologies, transistor scaling and integrated silicon photonics are changing how I/O will be done over the next decade. The most exciting and promising of these emerging technologies for electrical and optical interconnects will be highlighted at ISSCC 2023.

Digital Systems: Digital Architectures and Systems

Subcommittee Chair: Thomas Burd
Advanced Micro Devices, Santa Clara, California

This year's selection of processor papers highlights the industry adoption of the most advanced CMOS technology at the 4-5nm node. Innovative packaging technologies, including 3D stacking and direct bonding are being productized, which supports easy integration of multiple process nodes into a single socket (Figures 11 to 13). This has also fueled an exponential increase in on-system memory that drives increased performance (Figure 14). The drive to higher clock frequencies, which having slowed, still continues to tick higher, and is supplemented by a drive to increased core counts. Bump and through-silicon-via pitches continue to scale down at a rapid rate, enabling tremendous increase in bandwidth across multiple dies.

The mobile CPU continues to increase in both frequency and performance, while providing a wide range of performance and energy efficiency.

We see a continued push on application-processor performance and efficiency, along with video, display, and camera capabilities to fully leverage the ubiquitous connectivity smartphones provide (Figure 15). There are also major innovation efforts in 5G, artificial intelligence (AI), gaming and thermal management. 5G cellular technology is becoming more mature and the post-5G era is gaining more focus. The post-5G era will feature more antennas, more intelligence, and more use cases. The range of applications of neural network processing units (NPUs) is gradually expanding beyond image and speech recognition, to cellular performance improvement, SoC power and performance optimization. Therefore, not only the performance of the NPU is increasing, but also tiny NPUs for low-power operations are being applied everywhere. For better user experience and game quality, the main concern surrounding the display is moving from resolution to frame rate.

Circuits for Hardware Security: With the increasing risk and cost of information theft and safety hazards, hardware security has become a common requirement in intelligent and connected systems. Though focus on cryptographic implementation continues, cost-effective and low bit-error-rate physically unclonable functions (PUFs) are increasingly adopted in smart cards, sensor nodes, consumer devices, and automotive. True random-number generators (TRNGs) are also commonly required to strengthen secret key generation in cryptographic applications. Techniques to counteract side-channel attacks are enabling higher levels of security at lower design cost, thanks to the higher degree of design reuse and more digital circuit techniques. Counteraction of fault injection attacks is also becoming more common thanks to techniques ranging from logic-level fault detection to physical sensors. Quantum computers allow dramatic speed-ups in attacks on existing public-key algorithms. Standardization bodies such as National Institute of Standards and Technology (NIST) have started competitions to identify potential post-quantum cryptographic (PQC) schemes. Novel PQC accelerators are now being designed to efficiently and securely implement these schemes in hardware. Improvements in the efficiency of homomorphic encryption are being demonstrated to preserve both data usability and privacy in commercial cloud environments.

Figure 16 illustrates trends in area scaling in PUFs (area/bit) and TRNGs published recently at ISSCC, showing relentless area and cost reductions. With regards to techniques counteracting side-channel attacks (EM and power), Figure 17 shows the progressive improvement in the measurements-to-disclosure of cryptographic keys, as determined by the ratio of the power trace count necessary for a successful attack under protected and unprotected designs.

Figure 18 shows security primitives for the root of trust continue to evolve through design approaches enabling a higher level of integration with the existing silicon infrastructure (e.g., logic, memory), and merging multiple functions within unified designs. Some of these primitives are being employed in applications requiring high safety standards, such as automotive. Innovation continues in cryptographic accelerators and processors providing improvements in energy efficiency and flexible adaptation to pre- and post-quantum cryptography, as well as homomorphic encryption. The robustness against side-channel attacks continues to improve with a relentless increase in the mean traces to disclosure (MTD), which exceeds 100,000× under digital LDO- and machine learning-based protections. Countermeasures against semi-invasive and invasive attacks are devised to push physical security high enough that it does not become the weak link, while improving security on other fronts and types of attack. Solutions from sensing to logic are demonstrated to counteract fault injection, reverse engineering and power glitching attacks. In wireless links, physical security is also being enforced through secure directional links, which allow correct data reception only across the intended transmission direction.

Digital Systems: Digital Circuits

Subcommittee Chair: Keith Bowman
Qualcomm, Raleigh, North Carolina

The demand for more flexible and energy-efficient platforms ranging from embedded sensors to large neural engines continues to drive innovations in CMOS digital circuits and accelerators with goals of improving performance and energy efficiency. Digital circuit innovations also benefit from emerging technologies, such as non-volatile memories or deep-trench capacitors.

A continued trend in application-specific accelerators is the development of new circuit techniques that benefit a range of emerging applications, such as optimization problems in Ising or SAT-solvers, artificial intelligence at the edge for perception, speech recognition or advanced telecom channel decoders. Many of these accelerators leverage compute-in-memory (CIM) architectures or flexible tiled processing elements, including hybrid system partitioning between mixed-signal and digital-signal processing in memory, dedicated pipelines and machine learning in recurrent or spiking neural networks, while employing non-volatility with the right combination of all these techniques to optimize energy efficiency. Furthermore, custom data representation appears as a strong trend to reduce power consumption, whether with charge-domain computation or non-conventional number representation, along with an emphasis on data sparsification to skip unnecessary computations thanks to architectural clock or power gating. On the circuit side, we observe an increasing trend for custom memory bitcells integrating computing elements or non-volatility.

In addition, continued improvements in traditional digital circuit blocks for integrated power management and clocking are permitting new usage scenarios.

Integrated Voltage Regulators: Compute-intensive digital loads have been pushing the demand for high current loads of integrated voltage regulators. Block-level regulation with digital low-dropout (LDO) linear regulators is maturing for integration into scaled process nodes to allow multiple processor cores on the same input voltage rail to operate at unique voltages according to the core workload. Concurrently, high-efficiency voltage down-conversion has driven inductor-based regulators (LCVR) and switched-capacitor voltage regulators (SCVR) at finer granularities for dynamic voltage and frequency scaling (DVFS) of individual functional blocks. With the demand for high loads, the challenge for LDOs and down-conversion regulators is to maintain good area efficiency for large-scale integration, without sacrificing energy efficiency and response time. This year's papers address flexible output voltages under the constraint of high current density, limiting the dependency between input and output voltages with adaptive linear transfer function or adaptive ganged capacitors. Figure 19 describes the achieved current density of these integrated voltage regulators across calendar years, indicating a breakthrough improvement of an order of magnitude in current density.

Digital Clocking Circuits for Low-Jitter Applications: Clock generators continue an architectural migration from historical PLLs to multiplying delay-locked-loops (MDLL), injection-locked clock multipliers (ILCM) and fractional output dividers (FOD) to provide more functionality, variability management and lower design complexity at advanced nodes. Demand for compact low-jitter clocking circuits continues to increase with integer or fractional multiplication ratios with respect to a low-frequency reference.

In addition, power and area reductions achieved by digital and mixed-signal PLLs allow new usage models as analog functional block drivers, but these new usages come with additional signal integrity constraints, leading to the development of digital circuit techniques for spurious-tone (Spur) cancellation due to frequency mixing with a reference or a fractional multiplier. Figure 20 describes a key figure of merit (FoM) combining jitter and power for digital clock generators across calendar years, highlighting a continued trend in FoM reduction to the point that fractional multiplier architectures now compete with integer multiplier architectures, while the second plot shows the major effort on reference and fractional spur cancellation.

Machine Learning and AI

Subcommittee Chair: SukHwan Lim
Samsung Electronics, Mountain View, CA

In response to the growing interest in deep learning in recent years, ISSCC established a subcommittee dedicated to machine learning & AI in 2020. As deep neural networks (DNNs) are becoming widely deployed in wearables, mobile devices, edge and servers, the size and computational complexity of these DNN models increases dramatically. This results in increasing demand for higher efficiency and performance of neural-network computing chips. This year's submissions are grouped into two sessions. First, a full session has been formed to discuss heterogeneous ML processors in support of the popular DNN models. Due to differing requirements in various applications, general-purpose processors or domain-specific accelerators are deployed. They optimize for a wide variety of applications ranging from sparse transformers, to point cloud networks to spiking neural networks (SNNs) as shown in Figure 21. Deploying heterogeneous cores allows the designs to tackle a diverse set of layers and compute needs at the expense of additional area (Figure 22). Another full session on compute-in-memory (CIM)-based processors for ML includes contributions describing CIM processors supporting different reconfigurable circuit modes (NMC/IMC, SLC/MLC), while making use of several memory technologies (RRAM, eDRAM, SRAM) for various applications (DNN training, multimodal transformer, beyond-NN applications).

It is important to note that metrics that matter at the system level are energy-per-inference (or -per-training-example), and inferences/second (or training-examples/second) on a specific task at a *given inference (or final trained) accuracy*. This year's submissions significantly push the state-of-the-art on the efficiency and throughput metrics yet again, often by combining multiple enhancement techniques within a single chip (or multiple chiplets). One important aspect to note is that increased attention is paid to non-convolutional operations, as they become the bottleneck once the convolutions are accelerated significantly.

Some of the key emerging trends in machine learning and AI at ISSCC are:

1) Compute-in-memory (CIM) processors are becoming more popular. They make use of SRAM, RRAM and eDRAM technologies. Digital CIM continues the trend of system-level integration to avoid excessive data movements (especially off-chip). Design directions trend towards increased efficiency, reconfigurability and flexibility by using multi-mode memory arrays, mixed NMC and IMC circuits, as well as unified fixed-point and floating-point units.

2) Exploitation of sparsity in various forms has been an important focus of both inference and training acceleration. Emerging techniques continue in the direction of workload reduction via skipping unnecessary compute that range from sparse convolution, sparsity generation using forward gradient, entropy-based early exiting and local attention use. These techniques aim to leverage sparsity in convolution kernels, forward gradients, execution paths and attention spans, respectively.

3) Incorporating the concept of dynamic adaption into ML processors is featured in several papers, which leads to better energy efficiency, while minimizing accuracy loss. Typical dynamic tuning knobs include data precision, dataflow in the pipeline, resource switching as well as body biasing.

4) Attention to SNNs has increased due to their low power consumption. An asynchronous SNN processor is proposed to realize the ultra-low power on-device training by using software-hardware co-design. A hybrid approach to both SNNs and CNNs has been presented as well.

5) Deploying a heterogeneous set of cores within an SoC has become more commonplace. As workloads such as deep convolutions are optimized heavily, the remaining operations from a diverse set of operators become the new bottleneck necessitating the need to handle other operations well. A heterogeneous architecture has been presented in ISSCC 2023, which can take the "best of both" approaches and operate at a point that is more optimal. For example, an SNN engine is combined with a CNN engine to be a complementary DNN processor for reducing both the inference and training power. It leverages task switching between the ultra-low-power SNN core and the accurate CNN core.

6) Domain-specific ML processors are covering more novel application scenarios, ranging from transformer, point-cloud network, speech enhancement, object detection and tracking, AI-IoT and beyond-NN applications. Several domain-specific architectures have been proposed using HW/SW co-design methodologies to efficiently execute specific computing and storage operations.

7) ISSCC 2023 shows machine learning processors being implemented across a wide variety of technologies (CMOS, FD-SOI), as well as with package-level innovations (MCM). Other computational tasks, exploiting sparcity and data-reuse, achieve improvements in energy efficiency. Figure 26 helps illustrate this taxonomy between digital, analog, OFF-memory and IN-memory compute.

As different accelerators or processors are often characterized on a different set of tasks, network topologies, and accuracy levels, a direct comparison of the true system-level benchmarking metrics (e.g. energy/inference or inference/s) is not always straightforward. Therefore, it is instructive to look at the reported low-level metrics of operations/s and energy/operation within the neural network. Figure 23 displays the energy efficiency vs. throughput operating points demonstrated by the accelerators presented at ISSCC 2023 (red), compared to the state-of-the-art in 2016-2020 (blue), 2021 (black), and 2022 (green). Figure 24 plots the evolution of both energy efficiency and area efficiency (throughput-per-unit-area) over the past few years.

From these graphs, the improvement in terms of low-level metrics of operations/s and energy/operation is not very apparent. ML accelerators are clearly still improving at a very fast, almost exponential pace. Yet, ISSCC attendees should keep in mind that these TOPS/W and TOPS specifications depend strongly on the level of integration of the chip, and on the particular neural-network topologies being used. We have been seeing a clear trend towards more complete integration, in which the highly efficient MAC

compute arrays that were introduced over the past years are now integrated into full processing systems. Going forward, as the field matures, we believe that a common benchmarking methodology must be established which can properly account for the application context and provide proper translation between low-level and system-level performance metrics [1]. In the meantime, clever combinations of sparsity, variable precision and in-memory computing technologies are continuing to enhance deep-learning processor efficiency and throughput. With the increase of system-level integration of machine-learning engines together with other important subsystems (imaging chips, image pre-preprocessing, audio filtering and pre-processing, etc.), these performance improvements will continue to open up new AI applications.

Memory

Subcommittee Chair: Meng-Feng Chang
TSMC, Hsinchu, Taiwan

The demand for high-density, high-bandwidth, and low-energy memory systems continues to grow everywhere: from high-performance computing to SoC, wearables and IoT.

Innovations to 3D NAND flash, a very high density 5b/cell, will be introduced. New methods for improving reliability and quality of DRAM will be explained including probabilistic aggressor tracking against row-hammer attacks and core bias modulations to overcome process limitations. Meanwhile, the evolution of the memory high-speed interface continues by using single-ended PAM4 technology to achieve speeds of 16Gb/s/pin. Non-volatile memory continues to be applied to more advanced process nodes and continues to expand into a wider range of applications. This year a 16nm STT-MRAM that can operate in automotive environments (increased temperature range) and a 22nm near-memory-computing-macro using STT-MRAM are presented. In addition, the latest compute-in-memory developments are shown: increased energy efficiency, throughput, precision, and accuracy.

Top papers from ISSCC 2023 include:

- A 1.67Tb, 5b/Cell Flash Memory Fabricated in 192-Layer Floating Gate 3D NAND Technology and Featuring 23.3Gb/mm^2 Bit Density
- A 16nm 32Mb Embedded STT-MRAM with 6ns Read Access Time, 1M Cycles Write Endurance, 20 Years Retention at 150°C and MTJ-OTP Solutions for Magnetic Immunity
- A 22nm 8Mb STT-MRAM Near-Memory-Computing Macro with 8b-Precision and 46.4-160.1TOPS/W for AI-Edge Devices
- A 22nm 832kb Hybrid-Domain Floating-Point SRAM In-Memory-Compute Macro with 16.2-70.2TFLOPS/W for High-Accuracy AI-Edge Devices
- A 4nm 16Gb/s/pin Single-Ended PAM4 Parallel Transceiver with Switching Jitter Compensation and Transmitter Optimization
- CTLE-Ising: A 1440-Spin Continuous-Time Latch-Based Ising Machine with One-Shot Fully-Parallel Spin Updates Featuring Equalization of Spin States
- A 1.1V 16G DDR5 DRAM with Probabalistic Aggressor Tracking, Refresh Management Function, Per-Row Hammer Tracking, Multi-Step Precharge, and Core Bias Modulation for Security and Reliability Enhancement

Compute in Memory: Memory still turns out to be the bottleneck to performance and energy not only for traditional architectures but also for non-Von-Neumann architectures, including deep learning and potentially other emerging non-conventional computing paradigms. Innovations in compute-in-memory (CIM) continue to improve energy and area efficiency while maintaining the overall network accuracy. This session showcases latest developments in SRAM-based CIM with increased energy efficiency, throughput, precision, and accuracy. Both analog and digital CIM papers are presented this year. National Tsing Hua University reports a hybrid-domain floating point SRAM CIM macro. University of California, Santa Barbara introduces a continuous-time latch-based Ising machine implementation.

High-Reliability and High-Density DRAM: Industry requires ever-increasing DRAM performance and density for various applications (Figure 25). Furthermore, the ability to curtail row-hammer attacks has been a challenge to DRAM design, with improvements already discussed in other research areas. This year, this reliability enhancement is applied to a 16Gb DDR5 DRAM, and a 24Gb DDR5 with the highest density is presented in a 4th-generation 10nm DRAM technology.

Non-Volatile Memory (NVM): In the past decade, significant investment has been put into emerging memories to find an alternative to floating-gate-based non-volatile memory. Emerging NVMs, such as phase-change memory (PCM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and resistive memory (ReRAM), are showing the potential to achieve these high-cycling capabilies and lower-power-per-bit read/write operations. However, conventional flash memories are continuously improving, reaffirming them as the mainstream today and into the near future.

This year's papers report improvements in write performance (194MB/s) and read performance (34µs) for conventional 3D TLC flash memories. Also reported are improvements in memory bit density for TLC (more than 20Gb/mm^2) through advancements in 3D architectures, more than 300 stacked-WL and, for the first time, 5b/cell (PLC) with the highest bit density (23.3Gb/mm^2). Figure 26 shows non-volatile memory capacity trends.

NAND Flash Memory: NAND flash memories continue to advance towards higher density, lower power and higher performance; resulting in low-cost storage solutions that are replacing traditional magnetic hard-disk storage with solid-state disks (SSDs). The 3D memory technology is the mainstream for NAND flash memories in mass-production by semiconductor industries. Periphery-under-the-array is currently the reference architecture for TLC and QLC and PLC: it is enabling higher-bit density and multiple planes for throughput improvement.

The state-of-the-art for high performance TLC uses more than 300-stacked-WL. This year, for the first time, a 5b/cell has been presented, showing the highest bit density in the industry. Industries confirm investment to improve performance and bit density, which is expected to continue.

Figure 27 shows the observed trend in NAND Flash memory density at ISSCC over the past 20 years (and for the first time the PLC device is reported).

Innovative Topics: Medical

Subcommittee Chair: Rikky Muller
University of California, Berkeley, CA

Biomedical systems that interface with the body and nervous system in wearable and implantable applications continue to evolve toward more intelligent, multi-modal, and high-performance solutions, as well as closed-loop operation. Wearable and implantable SoCs record weak biological signals with high accuracy, stimulate neural activity, and extract key biological features under stringent power and size constraints. These new SoCs pave the way toward intelligent microdevices that enable innovations in health technologies with long-term measurement to treat on demand.

State-of-the-art biomedical integrated circuits and systems have further advanced this year at ISSCC 2023 with more intelligence as a significant trend in implantable and wearable devices, while improving dynamic range, power efficiency, and input impedance in the AFE and providing more application-oriented system-level integration towards closed-loop operation in interfacing with both the central and peripheral nervous systems. Multi-modal interfaces sense physiological signals such as PPG, BIOZ, and ExG, and provide nerve stimulation. High-dynamic-range sensing systems improve tolerance to large-amplitude interference and motion artifacts. Miniaturization combined with a high level of integration and wireless power/data transfer enables high-performance interfacing with the nervous system. Novel on-chip algorithms break the trade-off between hardware resources and real-time performance and can detect seizures on unseen patients without collecting their data for classifier training.

Innovations in intelligent classification of neurological signals (with minimal to no pre-training), enabled by on-chip or off-chip machine learning, have the potential to offer improved patient-independent neural interfaces to treat on-demand and in closed-loop. Incorporating machine learning with a high channel count of recording and stimulation will enable emerging therapeutic techniques to restore a healthy condition from chronic pain or other disorders without the side effects of drugs. These advances offer tremendous market potential in the medical market space.

Innovative Topics: Imagers

Subcommittee Chair: Rikky Muller
University of California, Berkeley, CA

In the field of image sensors, consumer applications push the evolution of fabrication processes to achieve advanced autofocusing capabilities in a small-pixel-pitch over large arrays. Samsung is further evolving the multi-photodiode pixel structure concept for all-direction autofocus with no compromises on other parameters, reporting a 50-MP CIS with 20k e- FWC, 0.98 e- random noise, and 86.2 dB dynamic range based on a quad-pixel structure. This is achieved thanks to highly customized front-side deep-trench isolation between pixels and between photodiodes in the pixel.

The race to shrink pixel size has expanded from conventional intensity imagers to event-based vision sensors, whose trend is dominated by hybrid approaches that combine intensity information with temporal contrast change detection and the 3D integration of the sensing layer with advanced processing stages. Omnivision achieves a record 4.6 Gevent/s rate on a 15Mpixel imager + 1Mpixel event vision sensor built upon a three-wafer stack. Sony addresses the pixel shrinking challenge in two 3D stacked works, both showing high dynamic range capabilities: one with a 35.6Mpixel array featuring 1.22μm pitch and 1.57e- random noise for the RGB intensity pixels and 4.88μm pitch for the event pixels, and another one that matches the resolution of the intensity and event images with a pitch of 2.97μm thanks to a shared front-end for contrast change detection.

On-chip image processing is also at the core of ultra-low-power imagers and high-dynamic-range sensors. This year, ISSCC presents a 55pW/pixel peak power imager powered by a 3.3×3.3mm^2 solar cell that can operate with no interruptions even in dim light conditions. Another work introduces a novel approach to HDR imaging that combines pixel-wise exposure coding with a binary readout scheme that compares the pixel flux to a sinusoidal reference, achieving 95 dB dynamic range.

Advances on the non-visible part of the spectrum witness the appearance of a SPAD-based X-ray detector and of the first 10Kpixel THz imager showing high-resolution images in the 3.08-to-3.86THz frequency range. The former is made of a high-frame-rate, high-dynamic-range, and low-power SPAD imager coupled to an X-ray scintillator. HDR is achieved working in a seamless global shutter mode, combining photon counting at low photon flux regimes and a time-encoded intensity estimation at high photon flux regimes. In the latter, a step-covered patch antenna and a defected ground structure achieve a high sensitivity at >3.0THz frequencies over a large pixel array.

Innovative Topics: Technology Directions

Subcommittee Chair: Ali Hajimiri
California Institute of Technology, Pasadena, California

Technology innovations bring the promise of enabling new system functionalities or substantially increasing the efficiency of existing ones. Harnessing such innovations for solving tangible real-world problems requires novel system-level solutions. With a focus on envisioning the future, emerging trends in Technology Directions this year at ISSCC 2023 covers a wide range of topics including quantum engineering, emerging sensor systems, internet-of-things (IoT), optical computation and photonics. ISSCC 2023 features four sessions representing the latest technological innovations in the following areas:

Quantum Computing: Quantum computers often comprise an array of quantum devices operated at cryogenic temperatures that must be controlled by an electronic interface. To fulfill the quantum-computing promise of a disruptive computational advantage, significant research efforts are pushing the scaling of those quantum processors and, consequently, their electronic interface. ISSCC 2023 mirrors this trend by presenting SoCs that can improve system reliability and complexity by operating at cryogenic temperatures to reduce the gap between the control electronics and the cryogenic qubits. To this end, a single SoC is shown driving both single-qubit and two-qubit operations on superconducting qubits, and two papers present advances in the microwave-driver architecture for superconducting qubits to reduce power dissipation and chip area. While ad-hoc circuit techniques are introduced to improve the performance of individual cryogenic circuit blocks, such as flicker-noise reduction in the presented cryo-CMOS VCO, novel functionalities are also explored, such as a THz backscatter transceiver to avoid heat-transferring cables for data transmission between room-temperature and cryogenic electronics.

Emerging Systems and IoT: ISSCC 2023 pushes the frontiers of integrated sensing and ultra-low-power IoT systems across a diverse space of emerging applications including biomedical, electrochemical, material and energy sensing. We see new advances in biosensing and bio-manipulation on-chip with demonstration of optics and electronics co-integration enabling chip-scale fluorescence sensor arrays, and 2D cell manipulation with on-chip electrodes. State-of-the-art performance in low-power operation and higher sensitivity are demonstrated with sub-THz electron paramagnetic resonance systems, low-power electrochemical and battery health monitoring ICs for electrical vehicles. Energy-efficient and scalable networks are needed to enable the future world of intelligent sensors. On that front, ultra-low-power IoT tags are demonstrated that can harvest energy from LTE to backscatter Bluetooth into WiFi channels.

Ideas for the Future and Ideas Outside the Box: This year, ISSCC 2023 includes two sessions focused on presenting out-of-the-box ideas for the future, highlighting topics both familiar and less-familiar to ISSCC that push the envelope of solid-state circuits and systems that are bound to inspire the next generation of engineers and scientists. These sessions cover a wide range of topics including 3D memory, dielectric waveguides, DNA nanotechnology, bioresorbable implantable devices, 2D materials, energy harvesting systems and advanced photonics, and photonic design techniques.

Summary

According to the Semiconductor Industry Association (SIA), global semiconductor sales have increased from US $139.0 billion in 2001 to US $555.9 billion in 2021, at a compound annual growth rate of 7.18 percent per year. Based on the recent World Semiconductor Trade Statistics (WSTS) forecast [2], worldwide semiconductor industry sales are expected to reach US $601 billion in 2022 and US $633 billion in 2023. The year-on-year growth rate in 2022 is expected to reach 8.8 percent. In this environment, ISSCC continues to be the premier technical forum for presenting advances and predicting trends in solid-state circuits and systems. Semiconductors are crucial components of electronic devices and the industry is highly competitive. Beyond this article, a complete trends document will be available at www.isscc.org. These trends will be highlighted in papers presented at the 70th ISSCC, being held at the San Francisco Marriott Marquis during February 19th to 23rd, 2023. Attendance at ISSCC 2023 is expected to be around 2,700. Corporate attendees from the semiconductor and system industries typically represent about 60% of attendees. We look forward to seeing you there!

Acknowledgments

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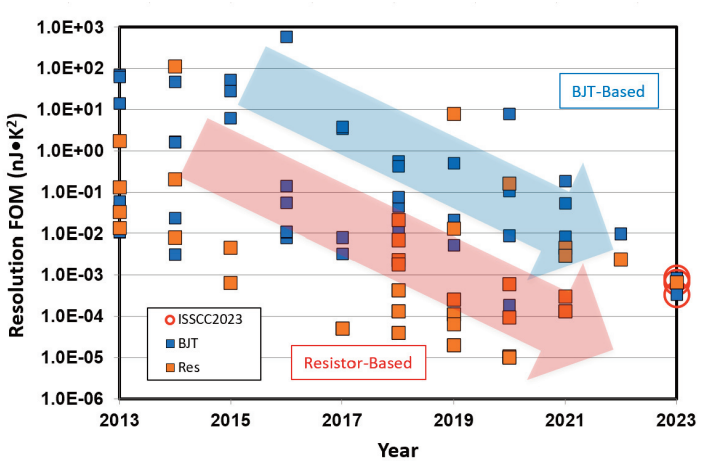


Figure 1. Trends in power efficiency of temperature sensors.

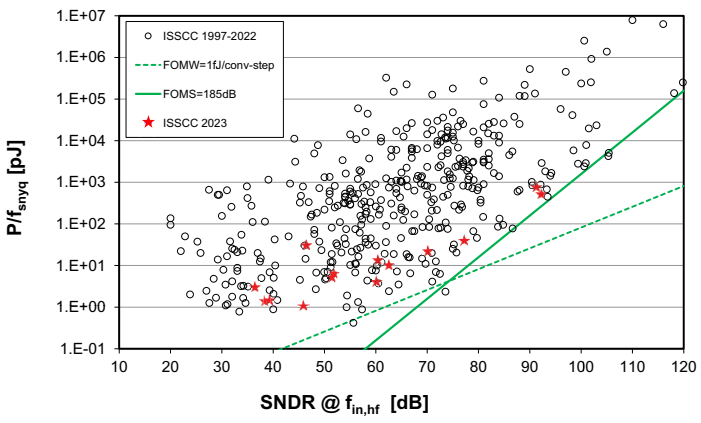


Figure 2: ADC power efficiency (P/f_{snyq}) as a function of SNDR.

70th Anniversary

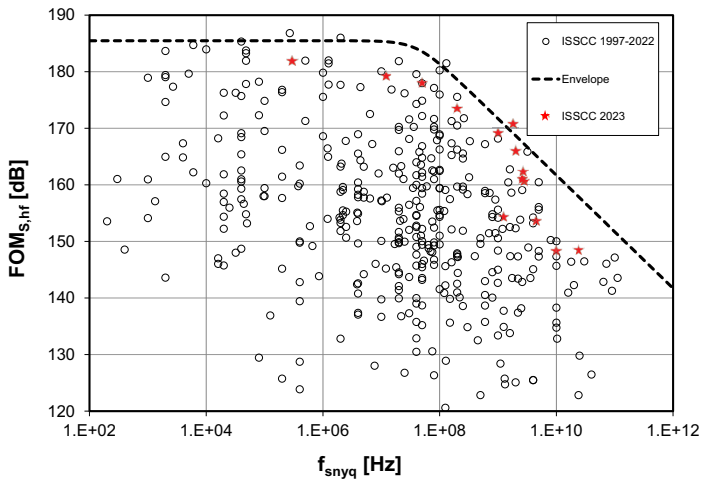


Figure 3: Power normalized noise and distortion versus the Nyquist sampling rate.

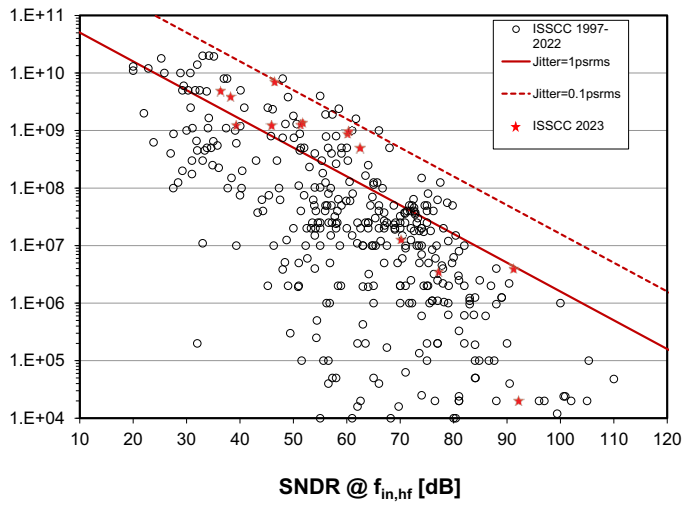


Figure 4: Bandwidth versus SNDR.

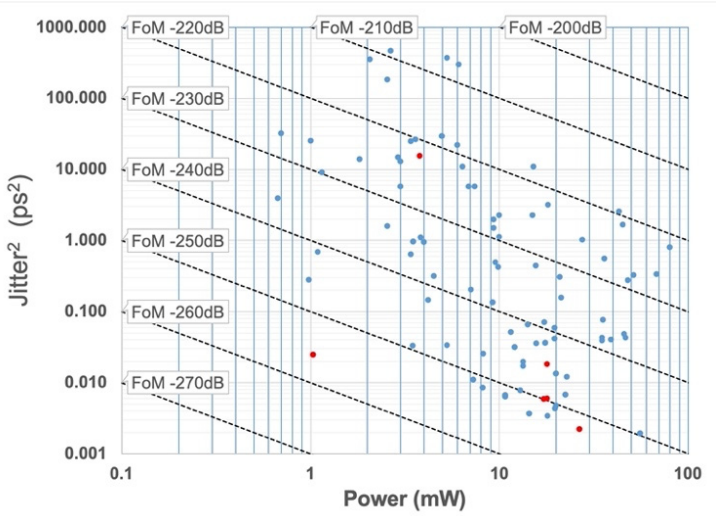


Figure 5: PLL trends.

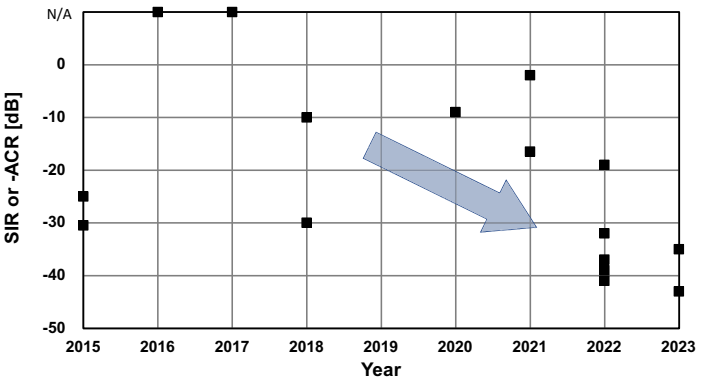


Figure 6: Plot of signal-to-interference ratio (SIR) or adjacent channel rejection (-ACR) versus year as reported by ULP receivers published at ISSCC.

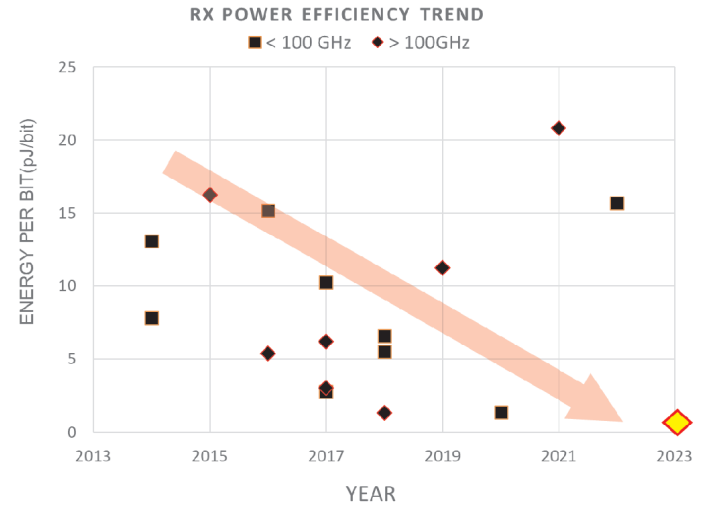


Figure 7: Receiver power efficiency trend of mm-wave and sub-THz high-speed wireless communications.

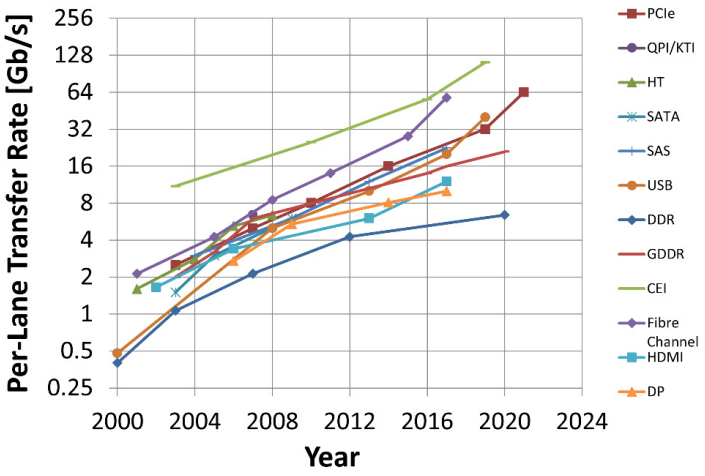


Figure 8: Per-lane data rate versus Year for a variety of common I/O standards.

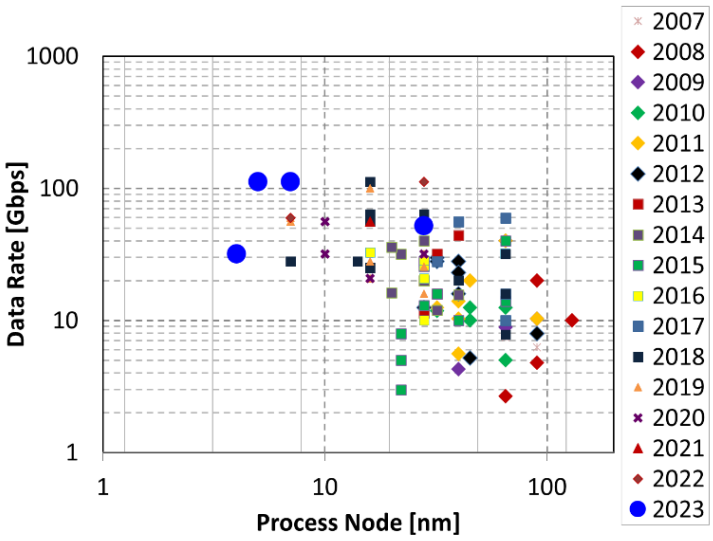


Figure 9: Data-rate versus process node and year.

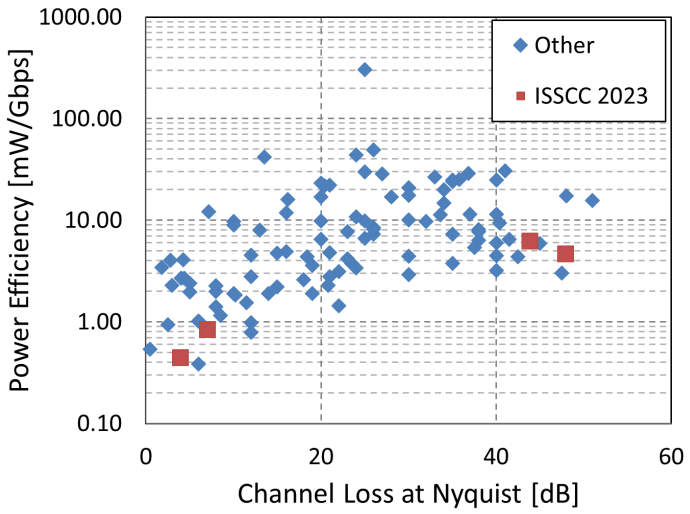


Figure 10: Power Efficiency versus channel loss and year.

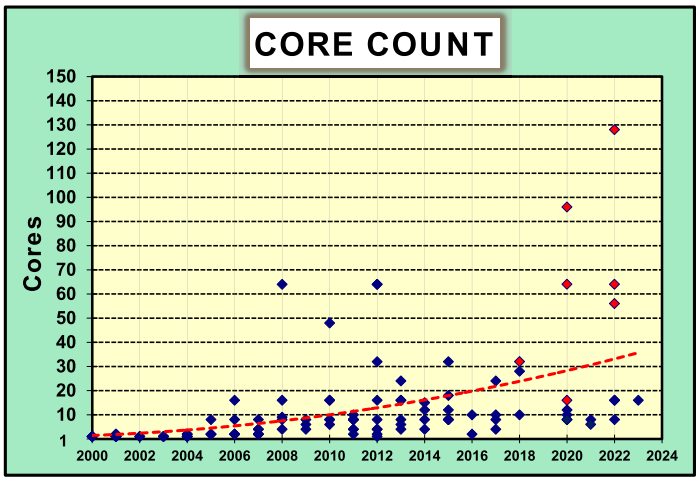


Figure 11: Core-count trends (red diamond designates multi-chip module).

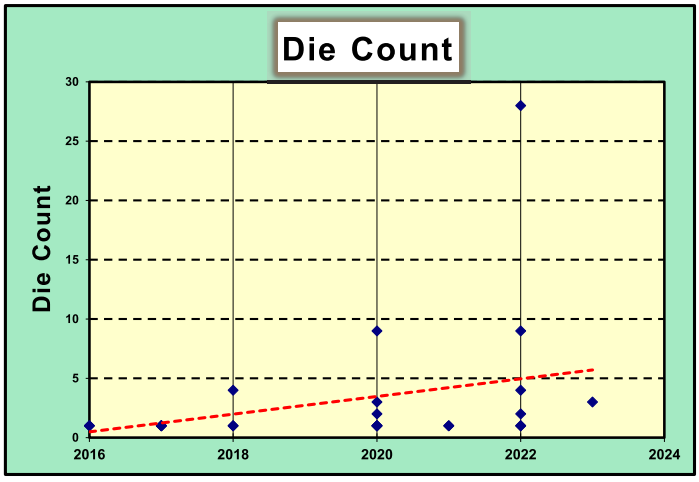


Figure 12: Die counts in a system trends.

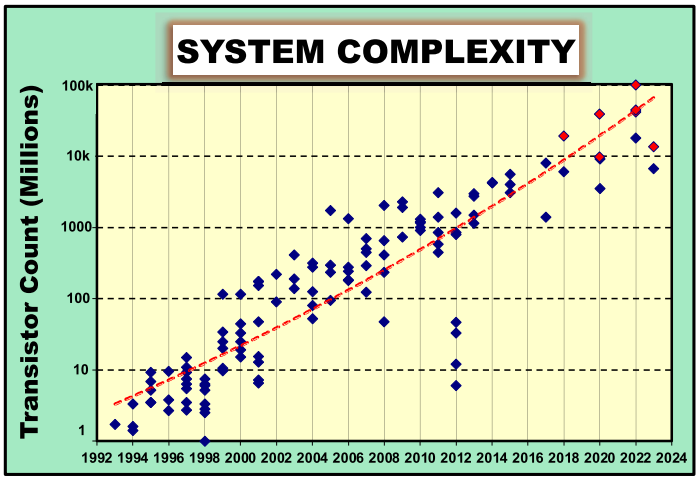


Figure 13: Chip-complexity scaling trends (red diamond designates multi-chip module).

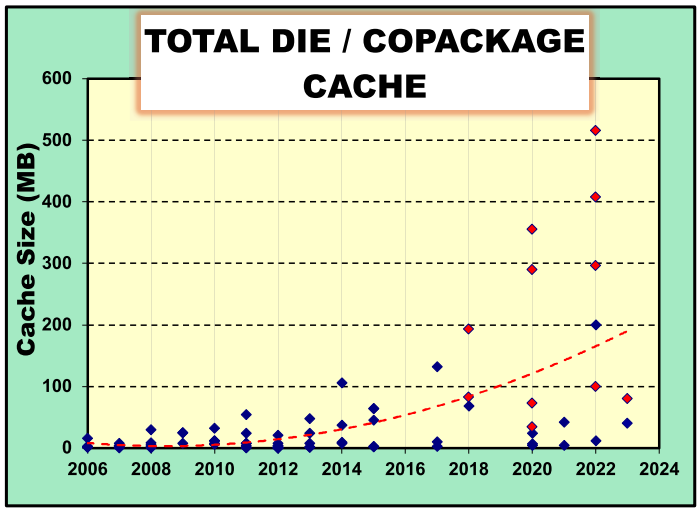


Figure 14: On-die cache-size trends (red diamond designates multi-chip module).

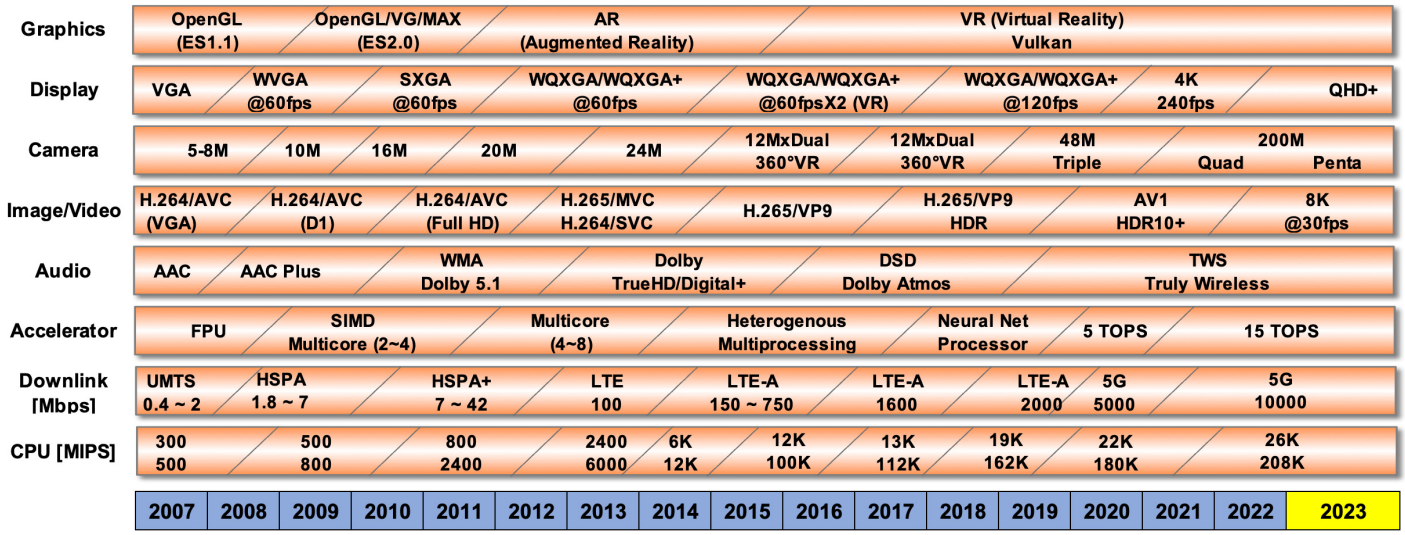


Figure 15: Application-processor trends in smartphones.

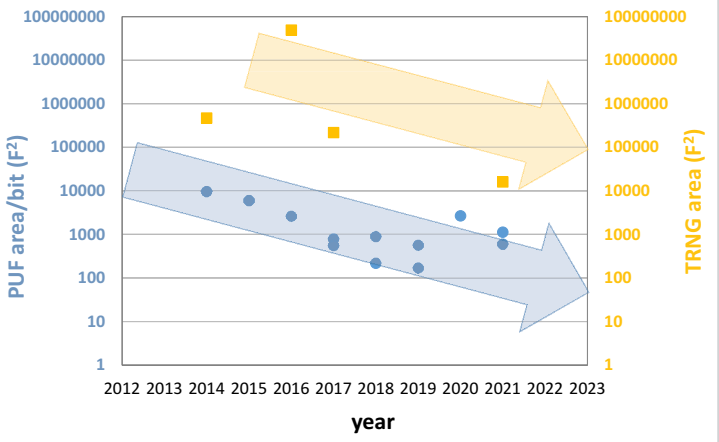


Figure 16: Area/bit trends for physically unclonable functions (PUFs) and area trends for true random number generators (TRNGs) published recently at ISSCC.

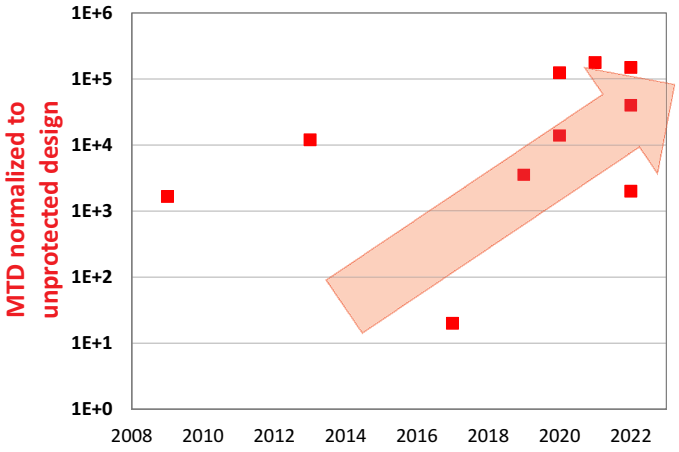
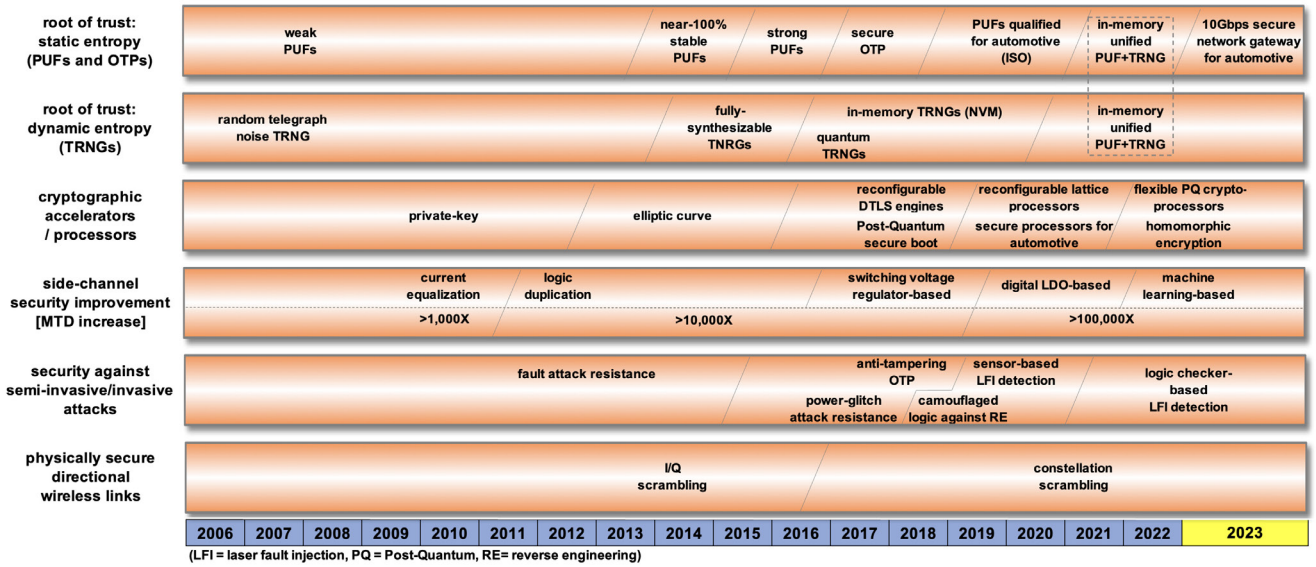


Figure 17: Improvement in measurements-to-disclosure (MTD) of cryptographic keys of side-channel counteraction techniques (normalized to unprotected design).



(LFI = laser fault injection, PQ = Post-Quantum, RE= reverse engineering)

Figure 18: Security trends.

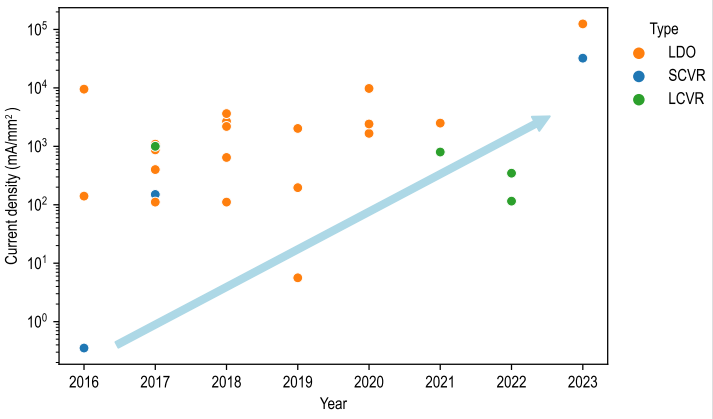


Figure 19: Integrated voltage regulator trends in current density with respect to active area.

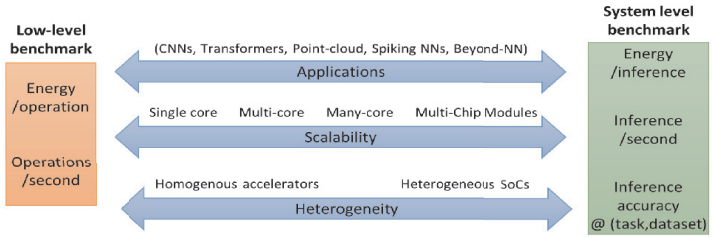


Figure 21: Various parameters impacting low-level and system-level benchmarking metrics.

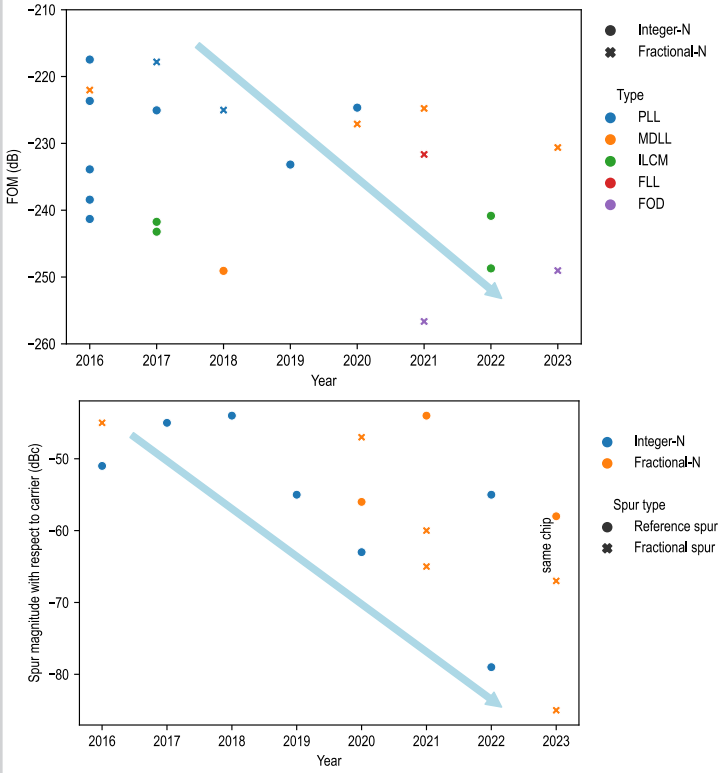


Figure 20: Top: Digital clock generators key figure of merit (FoM) across recent years, defined as: FoM = 10 × $\log_{10}$((Jitter$_{RMS}$ / 1s)^2 × (Power/1mW)); Bottom: Spurious tone reduction trends.

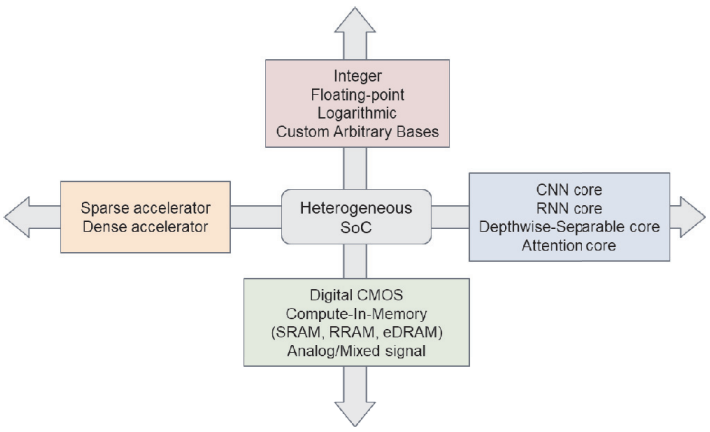


Figure 22: Heterogeneity in deep-learning accelerators.

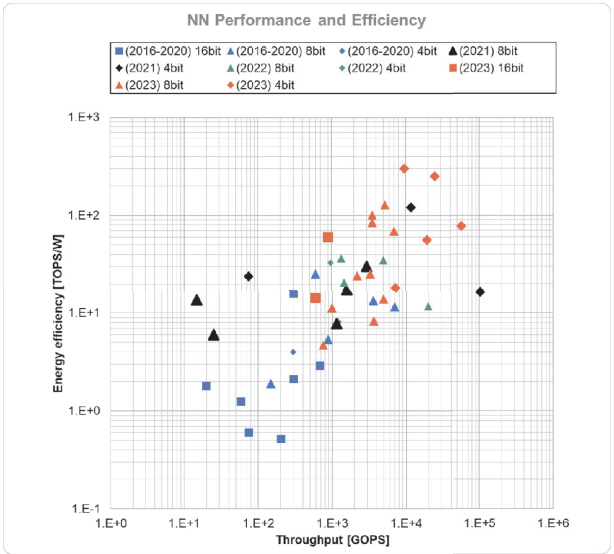


Figure 23: Deep-learning processor energy-efficiency (TOPS/W) and throughput (GOPS).

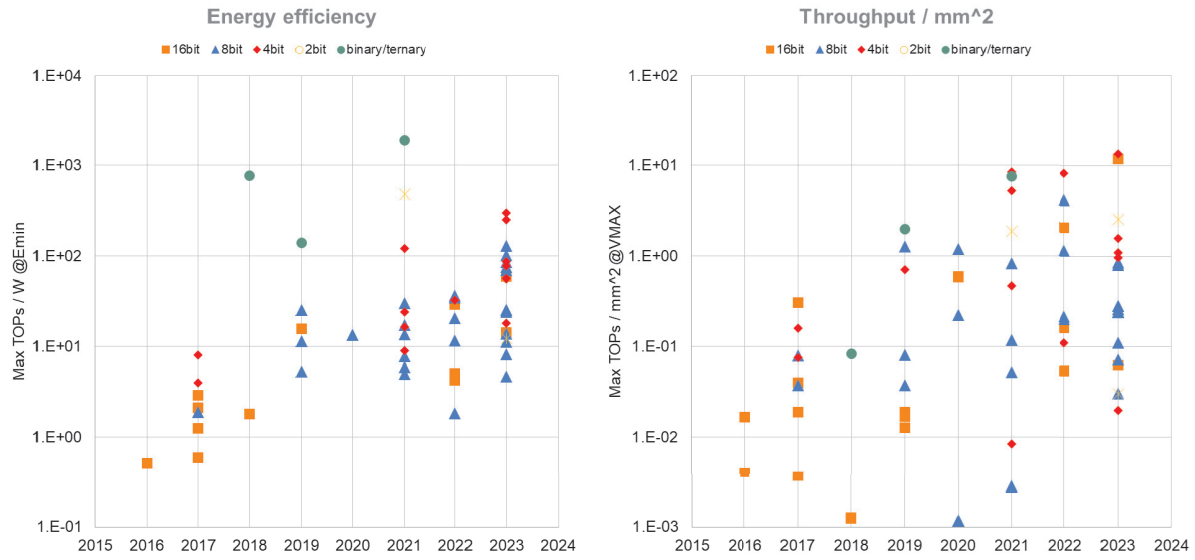


Figure 24: Evolution in energy efficiency (TOPS/W) and throughput per unit area (TOPS/mm²) of ML inferencing processors.

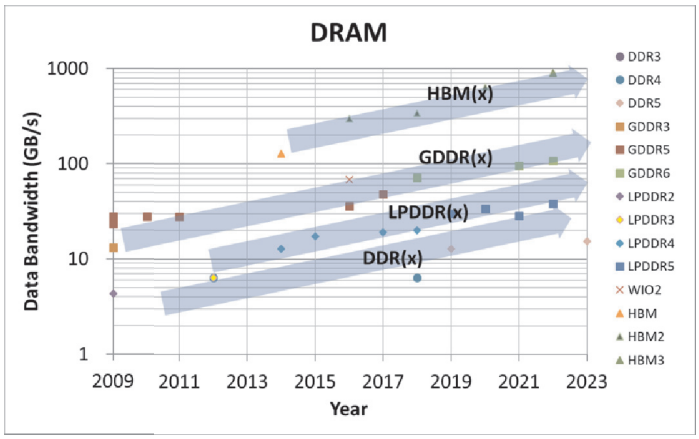


Figure 25: DRAM data bandwidth growth.

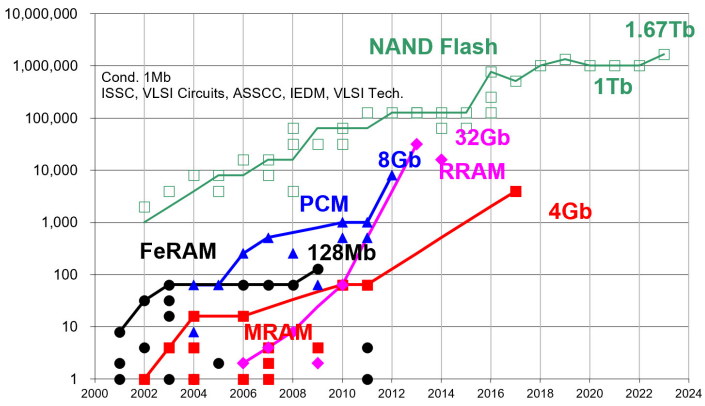


Figure 26: Non-volatile memory capacity trend.

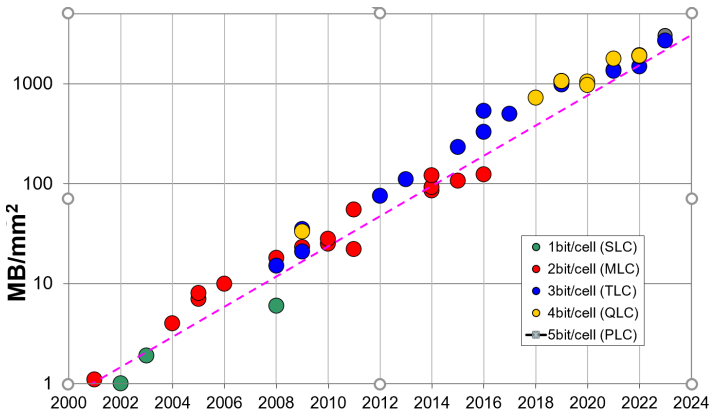


Figure 27: NAND flash memory density trend.

Thirty-Three+ Years of Volunteering at ISSCC
The Saratoga Group

This year, the 2023 IEEE International Solid-State Circuits Conference (ISSCC 2023) marks the 33rd year of the Saratoga Group, a group annually dedicated to the in-conference, real-time creation of the conference record (previously named the "Slide Supplement" and now known as the "Visuals Supplement"), which first appeared in a book version for ISSCC 1990. The idea of providing attendees with all presentation material arose as a result of a variety of comments made by attendees in a survey conducted for ISSCC 1989. The survey crystallized ideas that had been expressed for many years concerning the need to reconcile two problems that had long bothered attendees. The first was dissatisfaction with those who snapped photos of the slides during presentations. The second was the often-heard lament that the audience was shown marvelous things that were not recorded or depicted in the *Digest of Technical Papers*.

The data reduction of the survey was assigned to K.C. Smith, so Laura Fujino did all of it, and she was graciously allowed to present the findings at the August Executive Committee (ExCom) meeting in 1989. Amid discussion of various topics raised by the survey, a decision was made by the ExCom that a solution lay in developing some mechanism to provide copies of all presentation slides to every attendee after the conference. Subsequent to the meeting, ExCom Chair David Pricer was assigned to seek some mechanism for the resolution of this problem. Shortly thereafter, he contacted Laura with an invitation to join the ExCom to address this challenge. Within a few weeks, a concept emerged on how to proceed: the existence of a photocopier with a 35-mm slide projector attachment was identified from which medium-size paper copies of the slides could be made. Also, this photocopier had a paper-to-paper enlarging/reduction facility, which, although limited in range, could be used in multiple passes to acquire a paper image of the desired size.

The following new production process was implemented. Soon after the completion of his or her talk, the author's slide carousel was used to produce a set of paper images from the 35-mm slides. Later, these images were sized using the photocopier to provide paper images that were combined on an eight-per-page presentation using a manual cut-and-paste process. This was combined with the title, author data, and abstract in a nominal two-page format with extensions at the back of the compiled book, called the "Slide Supplement" to the *Digest of Technical Papers*.

During ISSCC 1990 held at the San Francisco Hilton, a group of volunteers and one part-time casual employee met in the Saratoga Room of the hotel to implement this process. The group included John Eggert (*Digest* and "Supplement" printer) and his wife, Shirley; John Wuorinen (*Digest* editor) and his wife, Susan; Nancy Pricer, Pricer's wife; Henry Osborne (a casual convention services employee); and Smith. All were under the direction of Fujino. Thus, thereafter, this group was called the "Saratoga Group." Because the process was machine-limited, it took long days to maintain a reasonable schedule with two operators (Osborne and Fujino). John Eggert led the manual final layout process, while Nancy Pricer collected the slides and sized paper copy. The others were involved primarily with image sizing. (It was pleasing to note that no blood was spilled during the cut-and-paste process.) The final product, the ISSCC 1990 "Slide Supplement" (193 pages) was printed, bound, and mailed to all attendees approximately one month after the conference.

Later Developments

The acceptance of the first edition of the "Slide Supplement" was strong enough that we were encouraged to continue the logical development of the original concept. For the next two years, during ISSCC 1991 and 1992, the process continued with some modification in the Saratoga Room at the San Francisco Hilton. However, for ISSCC 1993, operations were moved to the San Francisco Marriott, where the conference has remained to this day.

For ISSCC 1991 and 1992, the major change was the replacement of some of the initial volunteers and casual employee in the Saratoga Group by graduate student volunteers from the University of Toronto. For ISSCC 1994, following a change of the printer, Pat Duplessis joined the team and was placed in charge of manual page layout, for which he introduced the use of a waxer for image adhesion. This process continued with one major change (until the introduction of electronic projection in 2001): the major change, introduced at ISSCC 1993, was to use author-provided hard copy of the 35-mm slides to simplify image production, which required a slide-to-paper checking process; this, in turn, required more volunteer students but was otherwise faster and did not depend as much on unreliable equipment. Steve Bonney joined Duplessis for page layout for ISSCC 1997. For ISSCC 1998, 1999, and 2000, we replaced much of the photo reduction by scanning the author's hard copy and doing the sizing and page layout by computer.

For ISSCC 2000, an experiment was conducted with electronic projection (replacing 35-mm slides with computer-driven projectors) in three sessions, necessitating some additional image processing to produce the supplement. For ISSCC 2001, electronic projection for day sessions became the norm. This included the use of multiple computers for backup and reliability, with more student volunteers needed to operate them and provide setup and checking. At the same time, the name "Slide Supplement" was changed to "Visuals Supplement," and the task of page layout was assigned solely to professionals.

The Graduate Student Volunteer Group

Today, the graduate student volunteers are involved in a diverse set of tasks. Before the conference, they set up and check the laptops, of which four are used for each regular session to provide projection, projection backup, and audio recording, as required. In addition, the student volunteers:

- organize speaker and committee registration material
- handle corresponding speaker and committee registration
- set up equipment for speaker rehearsal
- assist with speaker rehearsals and the plenary speaker rehearsal
- unpack, check, organize, and transport award plaques to the ballroom
- manage the press desk
- interact with unionized audio/ visual staff
- check slides with speakers prior to their presentation
- operate the computer projection system for tutorials, forums, plenary sessions, regular sessions, evening sessions, and short course
- assist speakers during the Q&A period
- operate the recording system for plenary sessions, tutorials, and short course
- act as videographers for various events
- take photos of ongoing events
- complete data reduction for tutorials, forums, short course, and regular sessions
- help with crisis intervention, and so on.

For the past 33 years, the annual number of graduate student volunteers has ranged from three for ISSCC 1991 to a peak of 22 for ISSCC 2008 (to support the audio recording of the entire conference) to 17 since ISSCC 2011. Thisyear, our volunteer student group now at 20 will handle the live Q&A sessions for regular papers, tutorials, short course, and forums, record and process all presentations, run the Plenary Session, and so on.

There is an interesting anecdote concerning the performance of the volunteer students early on in the context of their handling of electronic-projection systems. Virtually from the concerning a magical process they witnessed during the Q&A periods of sessions they attended. Their common comment was that, miraculously, during an audience member's formation of his or her question, a highly relevant slide illustrating the subject of the question and, often, its answer would appear suddenly on the screen. The question to me was what marvelous artificial intelligence software had we acquired to allow such instant insight and response. My response was that it was not magically artificial but really human, the consequence of care in selecting and assigning the graduate student volunteers. Each was carefully chosen from among senior members of a large graduate student body in the Department of Electrical and Computer Engineering at the University of Toronto, typically from the Ph.D. or advanced M.S. degree program and representing a range of circuit-related specializations. Furthermore, they were assigned to sessions in the area of their research interests. Thus, they were among the most astute listeners in the audience.

It is interesting to note that a large fraction of these Saratoga Group graduate student volunteers have gone on to very successful careers in the solid-state area, both in industry and academia. Increasingly, they have been seen presenting papers at the ISSCC. For example, at ISSCC 2019, marking the 30th anniversary, there were six papers with coauthorship by an alumnus of the Saratoga Group. Moreover, one gave a short course and also received the ISSCC 2018 Lewis Winner Outstanding Paper Award. Meanwhile, their roles have expanded. Over the years, volunteers have provided emergency first aid for a torn muscle, and others have served as a translator for speakers whose native language is traditional Mandarin. Another interesting phenomenon, the result of this three-plus decade history, is that many volunteers are second-generation members, their advisor or a sibling having been one at an earlier stage in their careers.

Conclusions

Reflecting on the past 33 years, one may be surprised that such a process evolved through vast technological and personnel changes as well as vagaries of attendance variation, and most recently Covid. Beyond the annual appearance of the increasingly higher quality of slide material, including videos and animation, the process has influenced an enormous number of young lives, hundreds of individuals whose outlook on life is different because of their time of frenetic yet focused activity at the ISSCC, which many identify as being much akin to start-up dynamics.

In "Thirty-Three Years of Participation," you will find a list of members of the Saratoga Group over this period of hyperactivity along with the years of their membership. This list is dominated by student volunteer members, but it includes others, some volunteers, some assigned professionals.

Reminiscences

In recognition of the significance of the success of this 34-year adventure, some Saratoga Group alumni have been motivated to reveal some secrets of the past. The following six were group leaders in their own time.

Reminiscences by Vincent Gaudet (1997–2000 and 2003), University of Waterloo, Waterloo and Warren Gross (1999–2003), McGill University, Montreal

We both spent several years with the Saratoga Group, and we were there at an important time of transition away from projection by carousel and toward the new electronic age of PowerPoint. In the old days, Saratoga Group members spent most of their time behind closed doors, painstakingly verifying that the actual (physical) slides presented corresponded to what we had on file, allowing us to put together a true record for distribution after the conference. This all changed around 2000, and we were honored to be the two group members who oversaw the very first PowerPoint presentation at ISSCC, for a groundbreaking microprocessor design. We managed the laptops at the back of the room, advancing slides at the request of the presenter and with the aid of a sound signal. During the question period, we quickly understood that a question pertained to a particular slide, and we discreetly moved the presentation to that point, thus starting a new ISSCC tradition and a far more visible role for the Saratoga Group!

Reminiscences by Kostas Pagiamtzis (2001–2006), Alphawave, Toronto

Being a member of the Saratoga Group was a defining aspect of my graduate school studies. The deal was that, in return for volunteering in the group, you got to visit San Francisco and attend ISSCC. What a deal! However, being part of the Saratoga Group was difficult. Among other tasks, we spent long hours preparing and running the multiple computers during the sessions. Our goal was to make the presentations appear to run perfectly from the point of view of the audience, regardless of any behind-the-scenes glitches. Although any individual failure was a rare event, with about 200 presentations compressed into five parallel sessions over three days, multiple rare failures were common. Many problems were solved by having a backup laptop that could be swapped into production in the case of a crash or lockup. We made a special note of slow-loading slides, preloading them on the backup laptop and swapping the live and backup machines in real time to avoid a slide delay or hiccup. All this was done while paying close attention to the technical presentation so that we were able to select and display the relevant slide during the Q&A period. The tasks were physically and mentally taxing, but Fujino arranged for the most valuable reward possible to engineering graduate students: abundant free food! So the tradeoff was long hours in return for being at the foremost circuits conference and getting free meals. It was a good deal!

I was part of the Saratoga Group in three roles: as a student volunteer, as the lead student volunteer, and, after graduation, as a technical editor. Perhaps the most memorable role was being the lead student, also known as the "king," a tongue-in-cheek title for the lead volunteer given that he actually has no power over the other students. After all, who actually has the power to influence the behavior of graduate students? Even academic advisors often fail to conjure this power, but there is someone who has it: Fujino! She is the dynamo powering the Saratoga Group. Fujino, along with Smith, led the Saratoga Group by example. You can't help but give your best effort in achieving the shared goal when supporting them. My strongest memories of the Saratoga Group are of relationships with fellow students and with Fujino and Smith. To this day, I count many fellow student members of the Saratoga Group as friends and colleagues. I also count Fujino and Smith as friends. And, for me, their friendship and guidance is the most lasting legacy of the Saratoga Group.

Reminiscences by Andrew Shorten (2011–2017), Apple, Cupertino, California, and Mario Milicevic (2011–2017), MaxLinear, Carlsbad, California

Leading the Saratoga volunteer team from 2012 to 2016 was one of the most rewarding experiences of graduate school. Three floors beneath the San Francisco Marriott Marquis, our 16-hour days at ISSCC were fueled by high doses of adrenaline during Q&A slide changes, unexpected equipment failures, impromptu photo sessions, and on-the-fly plenary slide edits. "Survived again" quickly became the team's mantra year after year as we swiftly improvised solutions to technical hiccups, leaving attendees none the wiser as to the effort required to pull off what appeared to be a flawless conference.

But that was the easy stuff. The real adventure was in the months leading up to the conference, when we had to assemble the right team to make ISSCC happen. With about one-third of the team graduating each year, we had to constantly be on the lookout for new volunteers. We learned the hard way after our first year that we needed to interview prospective team members. We would look for incoming graduate students in the electronics and computer research groups who were broad-based, self-motivated, and technically savvy. As volunteers, they would be rewarded with the opportunity to help run the flagship conference of the IEEE Solid-State Circuits Society. As group leaders, we did our part to make sure that everyone performed well to earn this opportunity.

By day two at ISSCC, the team is usually exhausted, having enjoyed the live music a little too much at Foley's piano bar the previous night. At this point, newcomers are hit with the realization that ISSCC is a marathon and, if they're going to survive, they'll need to make new friends. This is when the magic begins to unfold. Team members who, back home, sit only a few cubicles away from each other finally start to talk! Dressed in full suits—a rather unusual sight for an engineering graduate student— they open up to each other and form amazing friendships.

While the adrenaline from slide changes and pointer-mouse replicator glitches keeps the team going at the conference, it is the friendships and camaraderie that bring team members back to ISSCC, year after year, even long after they have graduated. We are honored to have been given the opportunity to make this magic happen, and we look forward to reuniting with old friends at each year's conference.

Reminiscences by Samantha Murray (2019–present), PhD Candidate, University of Toronto

Since the Saratoga group switched to electronic slides and computers in 2001, our team's roles and responsibilities have largely remained consistent, albeit with innovations and technological upgrades along the way. Given the ISSCC's lengthy history, we all take great satisfaction in consistently putting on a conference of the highest caliber. Sadly, for the team that arrived at the Marriott in 2020, that period of smooth sailing and repetition abruptly came to a grinding halt.

By mid-February, everyone had heard about COVID-19, but we all remained hopeful that it would not spread worldwide. Due to travel limitations leading up to the conference, many papers were unable to be presented in-person by their first authors. There was a flurry of communication on how best to handle this unique situation. Were any co-authors present who could present the papers? Could the primary speakers present remotely? What about speaker rehearsal? Could we have the authors film a video of their talk? How would the Q&A period go for remote speakers?

These questions appear simple in retrospect, now that we have all participated in many virtual conferences, but we were all rushing with only a few days until the official opening of ISSCC 2020. Laura confidently announced, "The student volunteers are on it!" And so we were, with tireless support from Brad and Steve, of course. We created 16 different "ISSCC" Skype accounts for the 16 different speaker rehearsal rooms so that missing speakers could join remotely. These accounts were then assigned to the main salons by number. We quickly determined that the best strategy would be to play pre-recorded talks with live Q&A over Skype, minimising any bandwidth or audio issues.

In the end, we had 16 remote speakers plus one remote tutorial presenter. We hope that this process appeared seamless to the attendees, but there were some tense moments behind the scenes. The time zones were not working in our favor as many of the speakers' papers were shown at ISSCC after midnight in the speakers' local time zones. As a result, several nail-biting incidents occurred in which the speaker did not come online to coordinate with the student volunteers until after their video had already been playing for a few minutes! We also had to swap audio sources and adjust levels on the fly to switch between regular Q&As and those done remotely. Once our last remote speaker finished presenting, we all breathed a sigh of relief and closed out ISSCC 2020, hoping "surely next year will be back to normal." Ha, if only.

It was clear in the run-up to ISSCC 2021 that hosting an in-person event would be impossible, so the first-ever fully-remote ISSCC was born. At first, there was debate over whether student volunteers were needed; however, as the jobs started piling up, our services became necessary. In 2021, the conference was hosted on a combination of the Underline platform and Gathertown. Many rehearsals were held in the weeks leading up to the conference because we were all working with new tools and procedures. For the student volunteers, this was difficult as we suddenly had to work conference rehearsals into our class schedules! The actual week of the conference is during the "reading week" break in Canada, so the volunteers don't need to miss any class in a typical ISSCC year.

With the conference fully remote, the behind-the-scenes team was fully remote as well. We were all working from home on our personal computers with vastly different setups. Two monitors were a must for all of the recording and slide-sharing going on. We shared tips amongst ourselves on what recording software to use on Mac, how to hide the Windows task bar, and how to stop auto-advancing timed slides in PowerPoint. Despite the changes and on-the-fly learning, almost everything went off without a hitch. I say almost because I'm sure no one who was there will forget the audio feedback storm in Special Event 1 on Gathertown that managed to crash the entire thing and force the event to reschedule. At the end of ISSCC 2021, we all once again thought, "Finally, we made it; surely next year will be better..."

As 2022 approached, our hopes of reuniting in San Francisco were dashed for a second year by rising case counts and lengthy travel quarantines. The conference in 2022 was primarily held via Zoom and facilitated by the conference website and the Mira platform, which has long been the backbone of paper submissions. The student volunteers once again took on the slide-sharing and recording responsibilities from home. We faced similar challenges as in 2021, with many rehearsals eating up time in the weeks before the conference. At one point, we even ended up rehearsing for the rehearsal. Fortunately, everyone was familiar with online conferences and Zoom by this point, so everything went smoothly. Plus, being able to mute unruly participants was a blessing. Our 2021 online record was not perfect, however, with one of the plenary talks suspiciously stopping near its conclusion, before restarting to be wrapped up properly. For the most part, we were able to conduct another remote ISSCC with all of the behind-the-scenes scrambles masked from the attendees. Forum 6 finally finished, and we all celebrated: "ISSCC 2022 is done; surely next year will be back to normal."

As I write this, with 2023 on the horizon, it looks like we will once again be meeting in San Francisco (fingers crossed). Along with the rest of the volunteer team, I'm hoping for a return to the "easy" conferences of the pre-COVID era. However, with the first hybrid event, I am sure that new challenges await us. In any case, all we can hope for is to help present a high-quality conference and to continue learning along with the advancing field!

Acknowledgments

I wish to acknowledge that a major part of this article first appeared in the ISSCC 2019 *Digest of Technical Papers*, February 2019, prepared in recognition of the 30th anniversary of the Saratoga Group. Finally, I want to thank the generations of volunteer graduate students and others listed who have made all this possible.

—Laura Chizuko Fujino

The Saratoga Group Membership from 1990 to 2023

2008	Mohammed Abdalla
2002	Sherif Abdalla
2009-2011	Karim Abdelhalim
2022	Mohammad Abdolrazzaghi
2005	Mohamed Abdulla
2004-2008	Imran Ahmed
2019	Utku Alakusu
2007	Mehdi Alimadadi
2008, 2009	David Alldred
2013, 2014	Guy Alter
2014, 2015	Nadeesha Amarasinghe
1997	Jason Anderson
2006-2010	Ricardo Aroca
2003	Igor Arsovski
2003-2006	Navid Azizi
2015	Michael Baechle
2019-2023	Mohammad Bagherbeik-Tabrizi
2016, 2017	Robert Baker
1995, 1996	Srinivasa Banna
2007-2011, 2015	Kevin Banovic
2023	Ayandev Barman
2020-2021	Apurv Bharadwa
2007-2012	Mike Bichan
1996-1998	Jason Bickford
1994	Adi Bonen
1997-2023	Stephen Bonney
1993	Bertil Brandin
2007-2020	Nancy Bush
2005-2009	Trevor Caldwell
1999, 2000	Anthony Carusone
2001	David Cassan
2010, 2011	Pearl Cao
2005-2007	Theodoros Chalvatzis
2003	Trevis Chandler
2012-2015, 2017	Jingxuan Chen
2017-2019	Paul Chen
1995	Peter Chen
2017	Yu Ting Chen
2008	Horace Cheng
1996, 2000	Ruth Cherian
2000	Sarah Cherian
2003	Dickson Cheung
1992, 1994	Raymond Chik
2014, 2015	Stephen Alexander Chin
2004	Jeffrey Chow
1992	Terry Choy
1994	Jeremy Cooperstock
2019-2023	Jeremy Cosson-Martin
2022-2023	Wentao Cui
2002, 2004-2007	Ahmad Darabiha
1997	Sandy Decker
2005, 2006	Tod Dickson
1991	Ralph Duncan
2007-2013	Dustin Dunwell
1994-2000	Pat Duplessis
2017, 2018	Gairik Dutta
1990, 1991, 1993	John Eggert
1990, 1991	Shirley Eggert
2002, 2005	Yadollah Eslami
2001	Tooraj Esmailian
2002	Kamran Farzan
2009	William Feng
2023	Ashley Fang-Wei Hung
2001	Ted Fill
2009, 2010	Armin Fomani
2013, 2014	Ying Ying Fu
1990-2023	Laura Fujino
2013-2015	Michal Fulmyk
2006, 2007	Sean Garcia
2008, 2009	Ruslana Gelman
1997-2000, 2003	Vincent Gaudet
2016-2018	James Gentry
2004-2006	Dan Gerken
2004	Ahmed Gharbiya
2011-2013	Chris Gooch
1999-2003	Warren Gross
2020-2023	Rahul Gulve
2018, 2019	Nikita Gusev
2005, 2007	Afshin Haftbaradaran
2004-2012	David Halupka
2002	Anas Hamoui
2008	Adam Hart
2018	Peter Hermansen
2013-2015	Robert Hesse
2007-2009	Derek Ho
1999, 2001	Steve Hranilovic
2018, 2019	Hsuan Hsiao
2010	Safeen Huda
2020-2023	Kelly Hunter
2009, 2014	Alija Husic
2001-2006	Marcus van Ierssel
2004	Joel Ironstone
1998	Nadine Jackson
2009, 2011	Hamed Jafari
1991	Steve Jantzi
2020	Durand Jarrett-Amor
2019-2022	Violet (Wanlin) Jiang
2014	Ge Jin
2022-2023	Mustafa Ashiq Hussain Kanchwala
2008, 2009	Tony Kao
2004-2006	Rafal Karakiewicz
2015, 2016	Samira Karimelahi
2008	Mehdi Khanpour
2015	Alhassan Khedr
2015-2022	Jin Hee Kim
2012	Neno Kovacevic
1992	Karen Kozma
2012	Ivan Krotnev
2006	Fumie Kunimatsu
2006	Ian Kuon
2007	Mohamed Kwokgy
2018, 2019	Camilo Andres Tejeiro Lara
2005-2009	Katya Laskin
2001	Agustin Lebron
2003	Dora Lee
1992, 1993	Edward Lee
2022-2023	Edwin Kevin Ka-Yin Lee
2012	Junmin Lee
2005-2017	Bertram Leesti
1998	Oliver Leung
1993	Kam-Wing Li
2018-2023	Rophina Chi-Wai Li
2023	Zonghao Li
2013	Joshua Liang
1995	Tracy Liao
2013-2016, 2018	Sevil Zeynep Lüleç
2022	Helene Ma Yang
1997-1999	Dave McCausland
2007-2009	Scott McLeod
2011-2017	Mario Milicevic
2001-2003	Shahriar Mirabbasi
2016	Vincent Mirian
2017, 2018	Danial Mohammadi
1999	Elizabeth Morelli
2019-2020	Paula Miller
2019-2023	Samantha Murray
2015	Rosanah Murugesu
2016-2018	Javid Musayev
2006-2008	Akram Nafee
1995	Cuong Nguyen
2006	Sean Nicholson
2016-2023	Gerard O'Leary
1998	Javad Omidi
1990	Henry Osborne
2001-2006	Kostas Pagiamtzis
2006, 2007	Samir Parikh
2018, 2020-2022	Dhruv Patel
2009	Dimpesh Patel
2006, 2007	Jennifer Pham
2007-2023	Brad Philips
1997	Jason Podaima
2008	Gail Prestidge
1990-1996	Nancy Pricer
2015, 2016	Wahid Rahman
2001-2008	Jennifer Rodrigues
2000	Jonathan Rogers
2007, 2008	Bill Romer
2011	Alain Rousson
2009	Martin Rozee
2016-2020, 2022-2023	Daniel Rozhko
1996	Ricardo Saad
2001, 2002	Saman Sadr
1992	Reza Safaee-Rad
1995-1997	Mazen Saghir
2004-2008	Steve Samson
2016	Navid Sarhangnejad
1995	Angela Schultz
1993-1995	Kenneth Schultz
2007	Mahdi Shabani
2007-2009	Shahriar Shahramian
2010	Shayan Shahramian
2012	Alireza Sharif-Bakhtiar
1996, 1998	Ali Sheikholeslami
2012	Ravi Shivnaraine
2012	Stefan Shopov
2011-2017	Andrew Shorten
2000	Jim Small
1990-2023	Kenneth Smith
2010	Vadim Smolyakov
2013-2015	Dawei Song
2009	William Song
2009	Soroush Tabatabaei
2008, 2010	Tina Tahmoureszadeh
2018-2020	Ian David Taras
2019-2020	Camilo Tejeiro
2023	Zachary Teper
2011-2013	Clifford Ting
2012	Anita Tino
2009	Alex Tomkins
2005-2007	Olivier Trescases
1991	Patty Trnka
2012, 2013	Colin Tse
2005-2012	Aleksey Tyshchenko
2013, 2014	Jasmina Vaslijevic
2012-2015	Aynaz Vatankhahghadim
2023	Juan Camilo Vega
2012	Jeffrey Wang
2010, 2011	Jing Wang
2022	Lancy Wang
2012	Luke Wang
2004	Robert Wang
2023	Tian Wen Ma Yang
2023	Xinyuan Wang
2007	Guowen Wei
2011, 2013-2015	Yue (Victor) Wen
2003	Joyce Wong
2001	Laurie Wood
2002, 2003	Sarah Wood
1991	Steve Wood
1990	John Wuorinen
1990	Susan Wuorinen
2004, 2008	Navid Yaghini
2007-2011	Kentaro Yamamoto
2022-2023	Bender (Bangda) Yang
2010	Hemesh Yasotharan
2007, 2008	Kenneth Yau
2015-2017	Yue Yin
2016-2018	Jingshu Yu
2004	Ricky Yuen
2014	Mohammad Meysam Zargham
2017-2023	Saba Zargham
2010, 2011	Guangzhao (Andy) Zhang
2015, 2016	WeiJia Zhang
2019-2021	Yi Fan (Danny) Zhang

TOP ISSCC PAPER CONTRIBUTORS

ISSCC Authors with 20 or More Papers in the Past 70 Years as Compiled from IEEE Xplore

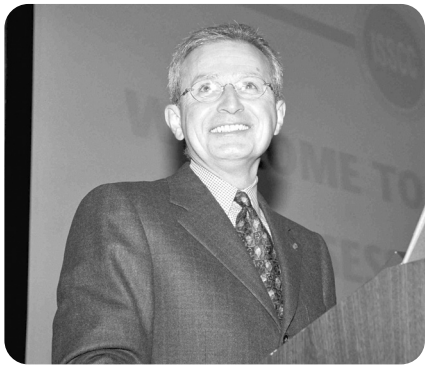
(Updated June 2023)

Author	Year of 1st Paper	Most Recent Paper	Affiliation	City	State/Country
Kofi A. A. Makinwa	2002	2023	Delft University of Technolgy	Delft	Netherlands
David Blaauw	2002	2023	University of Michigan	Ann Arbor	MI/USA
Anantha Chandrakasan	1993	2022	Massachusetts Institute of Technology	Cambridge	MA/USA
Dennis Sylvester	2000	2022	University of Michigan	Ann Arbor	MI/USA
Hoi-Jun Yoo	1995	2023	KAIST	Daejeon	South Korea
Rui P. Martins	2011	2023	University of Macau	Macau	China
Meng-Fan Chang	2003	2023	National Tsing Hua University	Hsinchu	Taiwan
Vivek De	1993	2023	Intel	Hillsboro	OR/USA
James Meindl*	1966	2010	Georgia Institute of Technology	Atlanta	Georgia/USA
Bram Nauta	1995	2022	University of Twente	Enschede	Netherlands
Tadahiro Kuroda	1992	2018	Keio University	Yokohama	Japan
Takayasu Sakurai	1984	2016	University of Tokyo	Tokyo	Japan
Gyu-Hyeong Cho	1997	2022	KAIST	Daejeon	South Korea
Piet Wambacq	2000	2023	imec	Leuven	Belgium
Behzad Razavi	1992	2022	University of California, Los Angeles	Los Angeles	CA/USA
Jan Craninckx	1995	2023	imec	Leuven	Belgium
Paul Gray	1970	2006	University of California, Berkeley	Berkeley	CA/USA
Asad Abidi	1984	2022	University of California, Los Angeles	Los Angeles	CA/USA
Michiel Steyaert	1988	2019	KU Leuven	Leuven	Belgium
Johan Huijsing	1975	2023	Delft University of Technology	Delft	Netherlands
Bruce Wooley	1970	2013	Stanford University	Stanford	CA/USA
Mark Horowitz	1982	2014	Stanford University	Stanford	CA/USA
Ali Hajimiri	1998	2023	California Institute of Technology	Pasadena	CA/USA
Masayuki Mizuno	1995	2015	NEC Corporation	Sagamihara	Japan
Hua Wang	2010	2023	Georgia Institute of Technology	Atlanta	Georgia/USA
Akira Matsuzawa	1984	2023	Tokyo Institute of Technology	Tokyo	Japan
Jri Lee	2005	2017	National Taiwan Univ.	Taipei	Taiwan
Hirotaka Tamura	1988	2019	Fujitsu Laboratories	Kawasaki	Japan
Eric Klumperink	2002	2020	University of Twente	Enschede	Netherlands
Kenichi Okada	2011	2023	Tokyo Institute of Technology	Tokyo	Japan
Joseph Tschanz	2002	2023	Intel	Hillsboro	OR/USA
Patrick Mercier	2009	2023	University of California, San Diego	San Diego	CA/USA
Shekhar Borkar	1995	2014	Intel	Hillsboro	OR/USA
Makoto Takamiya	2002	2018	University of Tokyo	Tokyo	Japan
Mototsugu Hamada	1998	2018	Toshiba	Kawasaki	Japan
Shoji Kawahito	1994	2022	Shizuoka University	Hamamatsu	Japan
Hooman Darabi	2001	2022	Broadcom	Irvine	CA/USA
Qiuting Huang	1995	2017	ETH Zurich	Zurich	Switzerland
Ram Krishnamurthy	2001	2020	Intel	Hillsboro	OR/USA
Daniel Friedman	1997	2021	IBM T. J. Watson Research Center	Yorktown Heights	NY/USA
Robert Brodersen	1975	2007	University of California, Berkeley	Berkeley	CA/USA
Tetsuro Itakura	1992	2017	Toshiba	Kawasaki	Japan
Francesco Svelto	1999	2018	University of Pavia	Pavia	Italy
Rinaldo Castello	1984	2013	University of Pavia	Pavia	Italy
David Hodges**	1963	1989	University of California, Berkeley	Berkeley	CA/USA
Pui-In Mak	2011	2023	University of Macau	Macau	China
Alexander Rylyakov	2001	2019	Elenion Technologies	New York	CA/USA

*1933 to 2020 **1937 to 2022

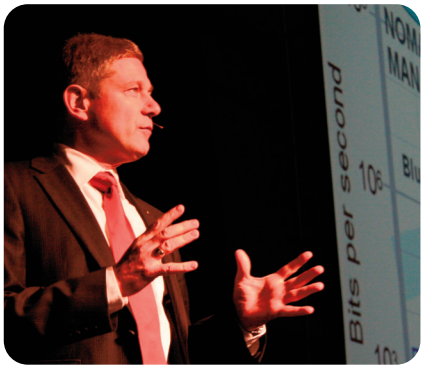
Memorable Plenary Talks

ISSCC 2003 Gordon Moore – Intel



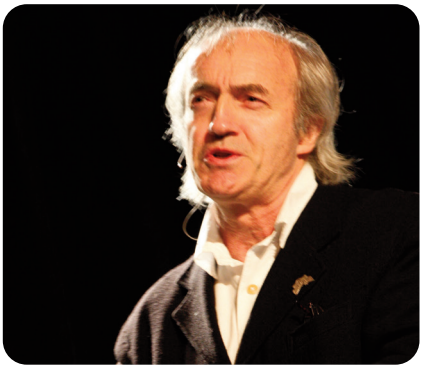
ISSCC 2004 Nick Donofrio - IBM

ISSCC 2005 Hugo De Man - IMEC



ISSCC 2006 Hermann Eul - Infineon

ISSCC 2007 Morris Chang - TSMC



ISSCC 2008 Bill Buxton
Microsoft Research

ISSCC 2009 John Cohn - IBM

ISSCC 2010 James Meindl
Georgia Institute of Technology

ISSCC 2011 Timothy Denison
Medtronic

ISSCC 2012 Eli Harari - SanDisk

ISSCC 2011 Reunion of Current and Past Members of the Saratoga Group. The Saratoga Group is largely composed of volunteer graduate students from ECE, University of Toronto.

ISSCC 2008 Plenary-Speaker Luncheon in The View Lounge.

ISSCC 2011: Paul Gray motivating the audience at the Student Research Preview.

ISSCC 2008 Award winners receiving instructions from Laura Fujino before Plenary Session.

ISSCC 2008 Press Gallery in the Mission Tunnel.

ISSCC 2003: Top ISSCC Paper Contributors being recognized at the 50th Anniversary Plenary.

Attendees at the Plenary-Session Break at ISSCC 2007.

ISSCC 2003 Plenary

ISSCC 2003 Plenary

ISSCC 2004

ISSCC 2005

ISSCC 2013: October Paper-Selection Meeting.

ISSCC 2006 Press Gallery

ISSCC 2013 Lisa Su & LeVar Burton

ISSCC 2015 Chris Mangelsdorf & friend

ISSCC 2016 Jan Van der Spiegel, Wanda Gass, Sophie Vandebroek (Plenary Speaker), Anantha Chandrakasan

ISSCC 2013 Ice Cream Social

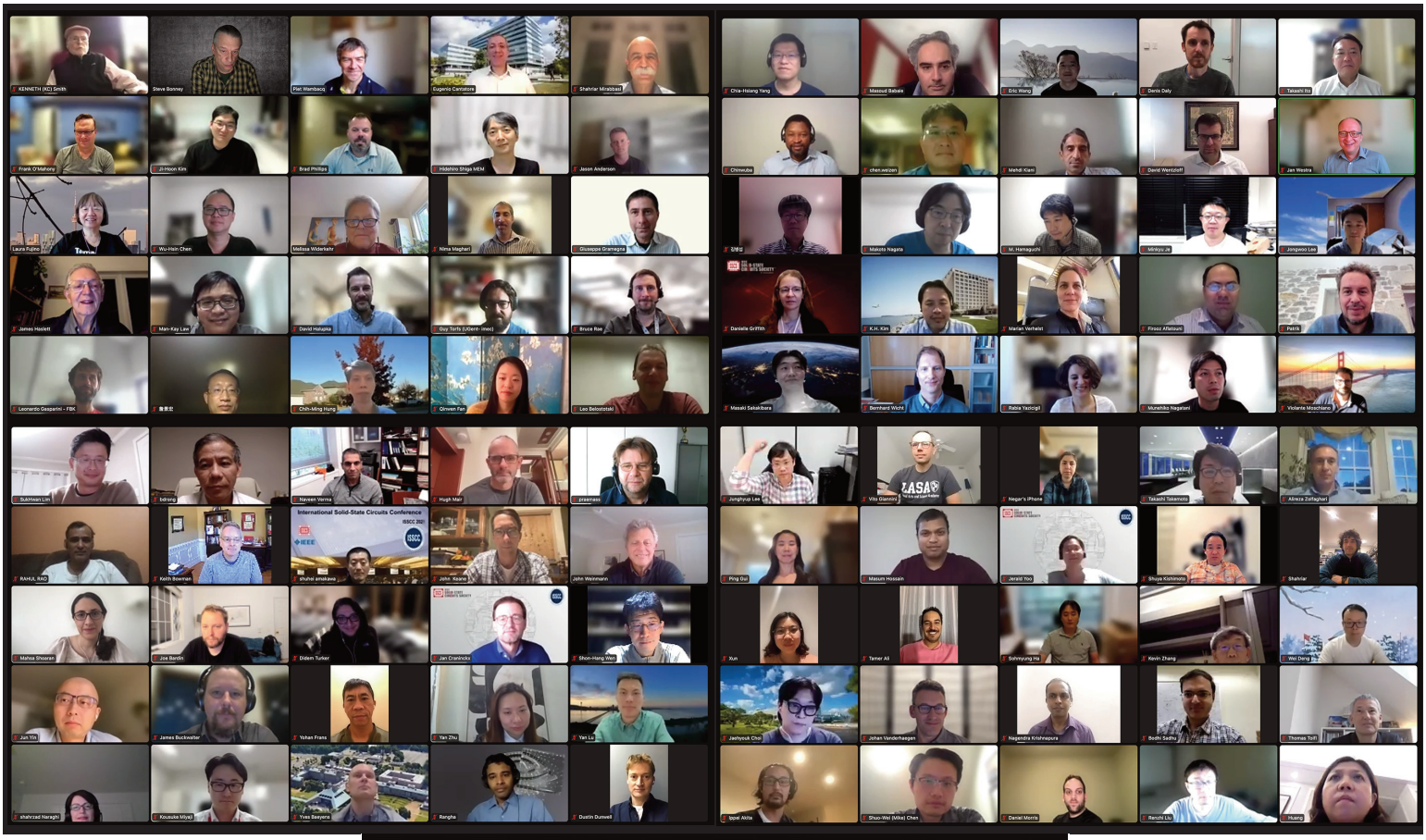
ISSCC 2017 Plenary - Willy Sansen

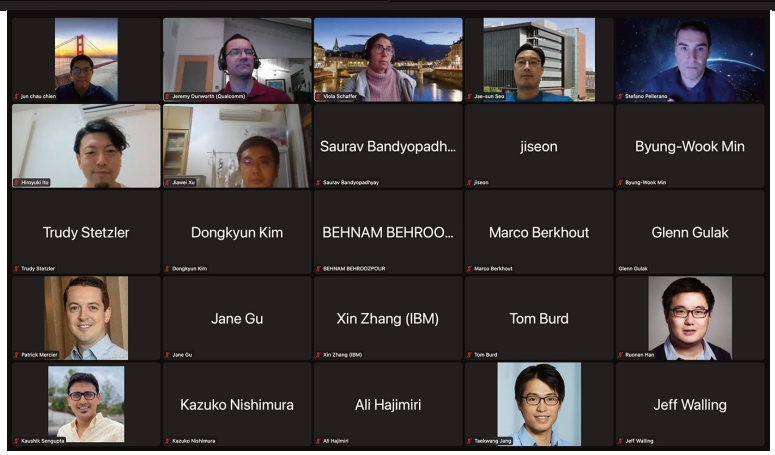
ISSCC 2017

ISSCC 2019 volunteer graduate students from ECE, University of Toronto

ISSCC 2020 Plenary

ISSCC 2023 Paper Selection Meetings



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