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WELCOME



Welcome to the special ISSCC 2013 Commemorative Supplement celebrating the 60th Anniversary of the International Solid-State Circuits Conference. While this celebration of 60 years of technological change at ISSCC focusses primarily on the past decade, many of the articles recollect earlier times, even to the beginning of the Conference.

This Supplement comes together with a DVD which contains a complete electronic copy of this text along with supplemental material including copies of the 1993 40th Anniversary Commemorative issues and the 2003 50th Anniversary Commemorative issue. These two additions are intended to help fill in the missing historical time preceding this Supplement, as well as providing additional historical photographs. To set the tone for this 60th Anniversary package, we have included the ISSCC 1954 Advance Program on the DVD. The DVD also includes copies of all papers referenced in the Subcommittee Overview in subject order with links from the article.



Following in the theme of providing historical context, the DVD also includes a full-length version of “ISSCC: The Early Pioneers”, a video recording produced to commemorate the 50th Anniversary, which was shown at the 2003 50th Anniversary Conference. This video includes interviews with five of the early Conference organizers, including John Linvill, the very first Technical Chair in 1954; Richard Baker, who was the Technical Chair in 1958 and 1967; Arthur Stern, who was the Technical Chair in 1959 and General Chair in 1960; Jerry Suran, who was the Technical Chair in 1961 and the General Chair in 1962; and Murlin Corrington, who was responsible for finances for many years. (Of these, only Jerry Suran survives.) Excerpts of this video are also available on the ISSCC website, currently located at http://isscc.org/videos/2002_pioneers.html.

Returning to the Supplement itself, it also includes an update of the ISSCC Author Honor Roll which was initiated on the occasion of the 50th Anniversary. In addition to this 60-year overview, there will be, as well, a snapshot of contributions over the past decade.

Also included in this Supplement are tables identifying the Conference leadership from North America, Europe, and the Far East, over the years. A new summary table not previously available shows for the past 60 years the number of Executive Committee members, the number of subcommittee specialties, and the number of committee members from each geographic area. Another table and associated graphs document the accepted papers by region over the history of ISSCC.

Yet another addition to this Anniversary Supplement, is an upgrade to what was first introduced for 2012 and presented then in the IEEE SSCS Magazine, “Through the Looking Glass: Trend Tracking for ISSCC 2012” [1]. As well, the 2013 version of ISSCC trends is included in this Supplement.

Finally, the Supplement contains a new article relating the history of “The Saratoga Group”. This group is composed largely of graduate students from ECE, University of Toronto, who volunteer each year to help with speaker registration, presentation-slide corrections, and operate the projection computers during the Conference amongst other tasks. The Saratoga Group began in 1990 with 8 members (all non students), and has evolved to be dominated by student volunteers to a number which is currently 25, including 17 students.

As at ISSCC 2003, ISSCC 2013 includes some celebratory events: the top contributors from the 60-year and 10-year Honor Rolls will be recognized during the Plenary Session; an anniversary cake will be unveiled and served at the Monday Social Hour; a special Monday Evening Panel will look at the past, present, and future of IC design; and each attendee will receive a 60th Anniversary thermos mug.

In closing, we would like to thank all of those who contributed to this Supplement, whose names can be found in association with their contributed articles. Thanks are also due to the members of the 60th Anniversary Committee, which besides ourselves includes Anantha Chandraskasan, Bryant Griffin, K.C. Smith, Alice Wang, and Melissa Widerkehr. Our special thanks go to Dave Pricer for his historical overview article. Dave, himself, is an ISSCC pioneer having been Program Chair in 1975, Conference Chair for many years, and has subsequently served in other Executive Committee roles.

We hope you will enjoy this compilation of 60 years of excellence at ISSCC!

John Trnka

Laura Fujino

ISSCC: SIXTY YEARS OF INNOVATIVE EVOLUTION

W. David Pricer, Charlotte, VT



The Early Years:

The pioneering organizers of what would become the International Solid-State Circuits Conference did not know they were laying the foundation for an international conference, or even an annual event. Founding Program Chair, John Linvill, wrote that future conferences of this kind might be “useful”, “from time-to-time”.

The first planning meeting in August of 1953 was held just six months before the inaugural 1954 Conference. John Brainerd of the University of Pennsylvania along with Linvill and H. J. Carlin of the IRE Circuit Theory Group were major instigators. The early participants came largely from the IRE Subcommittee of Transistor Circuits (the “4.10 Committee”), and the local Philadelphia chapters of both the IRE and the AIEE. (AIEE and IRE would later merge to become the present-day IEEE.)

Some of the pioneers remember the motivation underlying the first Conference somewhat differently: Linvill envisioned the Conference as an extension of the informal discussions within the IRE 4.10 Committee of which he was then Chairman; Merlin Corrington, the 1954 Treasurer, saw it more as a covert way to acquire teaching material for some very lucrative short courses taught by the local IRE chapter; Others simply thought “the time had come”.

The Program Committee in the earliest years was largely drawn from that same 4.10 Committee which had a somewhat “buccaneer” reputation. It was allegedly the only “Standards Committee” with no intention of ever writing a “standard”. It was also constituted with no more than one member from any one company. This, it was said, was to protect participants from being fired by their employers for what they offered to the discussion!

The first Conference in February of 1954 consisted of papers from just six organizations: Bell Telephone Laboratories, General Electric, RCA, Philco, MIT, and the University of Pennsylvania. There was no equivalent of today’s Digest of Technical Papers: Rather, attendees received a booklet of abstracts. A few authors were thoughtful enough to bring along a few hardcopies of their papers. Naturally, the limited supply of hardcopies quickly ran out! Locally based Program Committee members supplied the projection equipment and screens.

Moreover, the financial arrangements now seem quaint: The organizers had borrowed \$200 dollars each from the IRE and AIEE to fund pre-conference costs. Registration was four dollars (\$3 if paid before February 13th)! The registration price was based on a projected attendance of 400. Startlingly, 601 people registered, requiring a relocation of the presentation venue at the University of Pennsylvania.

The international presence at the first Conference consisted of a few attendees from Canada, and one attendee each from England and Japan. These proportions changed rapidly in the first few years of succeeding conferences. The first presentation from overseas appeared in 1958.

The name of the 1954 Conference appears in various publications and documents as: “The Transistor Conference”, “The Conference on Transistor Circuits”, “The Philadelphia Conference”, or “The National Conference on Transistor Circuits”. Whatever the name, everybody seemed to know what it was!

In 1960, after experimenting with almost-yearly title changes, the organizers settled on the present name: “International Solid-State Circuits Conference” (ISSCC).

While the Conference name stabilized within a few years, the definition of just what was “solid-state” took longer to evolve. Early “solid-state” technologies, as reported at the Conference, included: magnetic circuits, cryogenics, and pneumatic circuits. “Solid-state”, it seems, was anything without a vacuum tube! Eventually these competing technologies would succumb to the economies of integrated transistor circuits.

Converting regional birth to international breadth also took time! As late as 1961, four northeast-region American companies (BTL, GE, IBM, and RCA) contributed over 50% of the papers. The first overseas Program Committee members appeared in 1960. These were of necessity, corresponding members. Overseas air-travel was still considered expensive and a major hurdle to Conference participation. But, by 1965, the number of overseas program committee members had increased to 8, and, by 1968, the overseas papers were considered to be on par with those from North America.

In 1970, the overseas membership was greatly expanded and began meeting separately in both Europe and Japan under of the leadership of Jan Van Vessel and Takuo Sugano, respectively. Selected members of these regional program committees were dispatched to the final program meeting in America with the results of their local deliberations.

Evolution of the Technical Program Committee:

Very early, the Program Committee adopted the practice of rotating membership, such that each year 30 percent of the members would “retire”, and be replaced by “new” members. In the formative years, the Program Committee would reorganize itself yearly into new subcommittees in order to grapple with an ever-changing menu of new paper topics. In an era unconstrained by the demands of integration, a very broad range of technologies found their way into the “solid-state tent”. A few of these technologies, such as tunnel diodes, had a very short life time.

By 1968, the list of subcommittees had stabilized to become: Digital, Analog (linear), Microwave, and Other. The rather non-descript “Other” referred to a brave band of committee members prepared to review many examples of one-of-a-kind papers. By the mid-sixties the enormous economic power of circuit integration had marginalized many competing solid-state technologies, particularly magnetics, as well as semiconductor devices requiring unique diffusion profiles. Solid-state came to mean integrated semiconductor circuits. The subcommittee organization would remain stable for the next fifteen years

1984 was the last year of the Microwave Subcommittee. The microwave program had become a conference within the Conference, exhibiting little overlap with the wider attendee interest. “Microwave” was thereafter dropped from the program. Diversification in integrated circuit application rapidly filled the gap.

In 1985, Digital split into Digital and Memory; and in 1987 Signal Processing joined the committee roster. In 1992, the proliferation of subcommittee disciplines resumed with the launching of Emerging Technologies. This was the first subcommittee chartered to seek out solid-state applications which had not already found a home in ISSCC. Both the subcommittee title and charter were eventually expanded to Technology Directions. Papers reviewed by this Subcommittee have become one of the most highly-rated features of the Conference.

In recent years, steady growth in submitted papers and application diversity has further forced the multiplication of subcommittees. Today, these consist of: Analog; Data Converters; Energy Efficient Digital; High-Performance Digital; Imagers, MEMs, Medical, and Displays; Memory; RF; Technology Directions; Wireless; and Wireline. The Program Committee, which once met separately by region, now meets as one, and is the “International Technical Program Committee” (ITPC).

The Move from Philadelphia

ISSCC was founded in Philadelphia. In the formative years, ISSCC garnered broad support from established electronics firms in the American northeast. Many of these firms were within easy driving distance of the Conference’s home at the campus of the University of Pennsylvania. However, by the mid-1960s the center of semiconductor development in the United States was shifting west, and the international nature of the Conference was coming into sharper focus. Western attendees gradually became more vocal about moving the Conference to San Francisco. Unsurprisingly, the founders preferred their Philadelphia home. They had an effective if perverse-sounding argument: “When an engineer says he wants to attend a conference in Philadelphia in

February, management just *knows* he is sincere". Steady attendance, even in weak economic years seemed to validate this view.

A campaign by western attendees orchestrated by David Hodges, in time, convinced the sponsors to try San Francisco in 1978. The Conference then continued to alternate coasts, with New York soon substituting for Philadelphia. After a decade of consistently higher attendance, San Francisco became the Conference's permanent home in 1990.

The Role of the Executive Committee:

Although ISSCC is strictly a non-profit organization, continuity and financial sobriety requires it to be run like a business. In the formative years, the business committee was called the National Committee. The name was changed to the Executive Committee once the Conference firmly gained international stature.

The Executive Committee's structure has changed considerably over the years. From the formative years through 1980 the post of Conference (and Executive Committee) Chair was usually filled by last year's Program Chair. In roughly these same years, the continuity of business acumen was provided by Treasurer Bob Mayer, Digest Editor Lew Winner, Local Arrangements Chair Henry Sparks, and Sponsors Committee Chair Murlin Corrington. In the 1980s all four of these pioneers would retire or die. To provide the needed continuity, starting in 1980, the term of Executive Chair was extended to at least five years. Since then, there have been just five Chairs: Jack Raper, David Pricer, John Trnka, Tim Tredwell, and Anantha Chandrakasan.

The Lew Winner Years:

Lew Winner began his career as a magazine technical writer and New York City radio commentator. In 1956, he was recruited to help edit what was then called the "Technical Addendum to the Program Booklet" (of Abstracts). This would eventually become the "Digest of Technical Papers", but initially it looked more like today's Visuals Supplement. Lew and Editorial Chair Jack Raper, assisted by Lew's wife Beatrice maintained a standard of editing excellence for decades.

Lew's early association with ISSCC was tenuous. He did not even put his name on the first "Digest". Formal arrangements stipulated that he would be paid, but only after the Conference first showed a surplus. His title was Public Relations, which he kept to the end and well beyond the point when it was anywhere-near-descriptive of his duties.

By the mid-1970s, Lew was effectively the general manager of the Conference. As many of the pioneers retired in the 1980s, he further assumed some of their duties. He worked Herculean hours for a modest fee. His ability to resist sleep deprivation was storied. For fifty weeks each year his life *was* the ISSCC. Then for two weeks each year he would take a hotel room in Fort Lauderdale, sit on the beach and compile the Conference statistics. That was Lew's *vacation!*

In his later years, he came to enjoy playing the irascible curmudgeon. He demanded excellence, and delivered blistering scorn when he thought it was not immediately forthcoming. He could be fearless in making potential enemies, always safe in the assumption that Conference Chair Jack Raper would somehow negotiate peace afterwards.

The Expansive Years:

In the first thirty-five years the Conference Technical Program grew from 18 papers to about 90. The format, however, remained relatively constant year after year. There would be two and a half days of technical papers presented in three parallel sessions. The evening hours were filled with panel discussions, the more controversial the better. But, over the next twenty-five years, ISSCC would gradually add new features.

The Visuals Supplement (originally the Slide Supplement) first appeared in 1990. Speakers typically used about twenty 35mm slides during their paper presentation. Only some of these slides were captured in the "Digest". Speakers frequently inserted additional slides to their presentation at the last minute. The Supplement captured all 35mm images actually used in the presentation; and was mailed to all attendees shortly after the Conference.

The Supplement also provided one entirely unexpected benefit. During the previous thirty-six years the most consistent complaints of attendees were directed at papers that did not use good readable slide composition. The Conference had, for years, provided all speakers with slide preparation instructions.

While most speakers followed these instructions, some did not, with disastrous results. Speakers came to be required to submit their 35mm slides to Editor Laura Fujino before paper presentation. The most deficient images could be detected and hastily corrected before presentation. The advent of electronic projection made this image enhancement process better, faster, and more complete. Today, she and a small band of volunteer students and helpers intercept, and correct all poorly-organized or marginally-readable images before the attendees see them.

The Short Course was introduced in 1993. It is primarily directed toward engineers facing significant new knowledge demands. The subject changes each year, but the instructors are always recognized experts in rapidly moving fields. Over the following years, the handout materials have been enriched and expanded. Color printing is now the norm. As well, a DVD with audio and transcription, including all course images and copies of many relevant background papers, is available for purchase.

Short Papers also first appeared in 1993. Previously, the Program Committee had to choose between "technical-benchmark papers", and those with simple but "really neat" circuit ideas. The inclusion of Short Papers allows the Conference the capacity to accommodate both. Today, there are some 200 papers both, regular and short, presented.

The Tutorials were introduced in 1995. Their purpose is radically different from the Short Course. The tutorials are positioned before the presentation of regular papers in the Conference program, and are intended to provide "instant background" for attendees contemplating the exploration of areas outside their own. Repetition of tutorial presentations allow attendees to attend up to three such tutorials in one day. As well, a DVD with audio and transcription for all 9 tutorials, including all tutorial images and copies of many relevant background papers, is available for purchase.

In 1996, ISSCC finally broke with its austere past, and sponsored a social hour. Attendees took this opportunity to "network".

Also starting in 1996, ISSCC began to provide all attendees with a post-Conference DVD. This DVD allows electronic search of all information in the Digest and Visuals Supplement.

In 2001, ISSCC went all-electronic for projection. Because ISSCC uses the best-available high-intensity projectors, attendees can now take notes in near-normal ambient room light. ISSCC also added WEB registration which provides instant confirmation of successful registration. WEB registration has now become almost a necessity driven by the complexity of scheduling many Conference offerings, some of which have conflicting times and limited seating.

By 2001, ISSCC had evolved to a five-day format with up to five simultaneous events. The old two and a half-day three-event format was long gone!

Continuing the Evolution:

The pioneers who founded ISSCC deliberately excluded commercial application booths from the Conference venue. Their concern was rooted in the then too common experience wherein a conference technical program becomes subservient to its commercial aspects.

Times change and so do perspectives. Modern integrated circuit electronics allow for some fascinating demonstrations that would not have been possible in earlier years. The Program Committee has in the past three years invited a small set of accepted-paper authors to bring demonstrations of what their integrated circuit hardware can achieve. The attendee response has been quite positive. There are now two such evening features, one for academic, and another for industrial authors.

The Conference now also includes a Book Display. Participation is limited to publishers of engineering books, texts, periodicals, and courses.



Not all experiments succeed or succeed uniformly. In this mode, ISSCC has experimented with the electronic capture of the technical program for redistribution at more than one remote location. However, while technical success has been demonstrated, the Conference has not yet found a good general business plan for remote presentation of the full technical program. As a compromise, the Plenary Session, and demonstration sessions are posted on the ISSCC WEB site, as a standard ISSCC feature. Likewise, electronic capture of some of the ISSCC educational events has extended both the use and the audience of this activity.

In the early days, the Conference was always preceded by a Workshop sponsored by the original 4.10 Committee, and later by the “consolidated” Solid-State Circuits and Technology Committee. Their IEEE “workshop” format called for a very limited attendance of experts in the chosen-topic field, and dissemination of NO published material. The object was to encourage informal and uninhibited discussion. However, as the solid-state technology matured, the format evolved. Wider attendance and some limited publication seemed warranted. Sponsorship became under the direct control of ISSCC,

and has been expanded to six such events per Conference. The name has been changed to “Forums” designating a break with the more-insular “workshop” format.

For almost all of its history, ISSCC required all paper submissions to fit a single submission template. In 2009, the Conference recognized a different kind of paper with a distinctive audience. Students at many engineering universities had gained access to state-of-the-art semiconductor fabrication. In many cases they had found innovative applications. This work was interesting and stimulating but not necessarily ready for formal publication. The Student Research Preview allows students to showcase the direction of their work, and exchange experiences while retaining their opportunity for a formal publication at a future date. The Student Research Preview has its own Program Committee.

At 60 years of age, ISSCC continues to experiment. The Conference thrives!



ISSCC 2012 Women's Reception: Terri Fiez, organizer, and others.



ISSCC 2010 Coffee Break.

A DECADE OF CHANGE FOR THE INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

Trudy Stetzler, Houston, TX



Preamble:

The International Technical Program Committee (ITPC) performs a vital role for ISSCC. The ITPC is responsible for reviewing hundreds of paper submissions and selecting the highest quality ones for presentation, as well as organizing various evening events, tutorials, and forums.

From the beginning of the Conference in 1954 to 2003, the Technical Program Committee evolved significantly in both the number of subcommittees and committee members,

with the first overseas members beginning to participate in 1960 [1]. Over the past decade, this process has accelerated with the International Technical Program Committee rapidly evolving to reflect the changing technical environment, and the continuing international growth of the Conference.

Ten Years Ago:

Ten years ago, there were two regionally-based committees: the European Program Committee and the Far East Program Committee. The overall Program Committee was comprised of members from North America and representatives from these two regional committees. There were seven subject-area subcommittees for the paper review process: Analog; Digital; Memory; Signal Processing; Wireless and RF Communications; Wireline Communications; and Imagers, Displays, and MEMs. An eighth special subcommittee, Technology Directions, was charged with finding advanced technology and circuits techniques; It was comprised of a steering team with representatives from the seven other subcommittees [1].

The 2004 Program Committee included 112 members: 74 directly from North America, 35 representatives in total from the Far East and Europe, along with the Program Chair, Program Vice-Chair, and Program Secretary. This Program Committee was responsible for planning the Conference events and selecting papers for presentation.

The two full regional committees having 51 members in the Far East and 33 members in Europe held separate planning meetings to encourage the submission of papers from their regions, and to identify potential plenary speakers.

The Recent Decade:

Realizing the growing international importance of the Conference, and the increased submissions from around the world, in 2005 the Program Committee was organized into a single International Technical Program Committee (ITPC), including all members from all regions participating together in the planning and paper-selection meetings. This merger reduced the combined size of the technical program committee from 161 to 146 members: 64 from North America, 46 from the Far East, and 36 from Europe. The regional balance in the Technical Program Committee and subcommittees was maintained using a 3-year running average of the papers accepted from each of the three regions.

Since the committee was now a single International Technical Program Committee, there was an effort to make the June planning meeting more efficient for all members. Thus, in 2010, the June planning meeting was replaced with a mini-meeting of the Subcommittee Chairs to plan the Tutorials, Evening Sessions, and Forums. In 2011, this meeting split into two virtual meetings to accommodate the global time zones. The first meeting reviewed the previous ISSCC and plans for the next year's conference including evening sessions, forums, and tutorials. The second meeting finalized the evening sessions and discussed the IDS/ADS plans, Press Kit, ISSCC guest editor requirements, and strategic changes for the Conference.

Also in 2005, in recognition of the importance of emerging technologies and circuit techniques, Technology Directions became a separate subcommittee. The charter for this new subcommittee was to identify leading-edge developments of potential interest to our attendees, ones that were five to ten years away, but which would not normally be presented at ISSCC [1].

These selections were far ranging: from ones whose topic lay in the realm of a traditional subcommittee, but which lacked implementation details, to others whose subject area was outside that of usual ISSCC submissions. From time to time, several of the topics identified by the Technology Directions Subcommittee have become mainstream and have been included in a traditional subcommittee. As well, as the Technology Directions Subcommittee became more established, it evolved from actively soliciting papers to emphasize the review of papers that were submitted as part of the normal review process. The unique appeal of the Technology Directions sessions is evident by their high attendance.

Fueled by new standards and advances in technology and system architectures, there has been continued growth of submissions in communications and wireless technology. To address this growth in new areas, the Technical Program Committee was restructured in 2006 into nine subcommittees: The Wireless and RF Communications Subcommittee was charged to focus on Wireless communications, and RF circuit techniques were merged into the Analog and RF Subcommittee. A new subcommittee, Data Converters, was born from the Analog Subcommittee as a result of the increasing submissions in analog-to-digital converters for communication systems. As the explosive growth in paper submissions in the wireless area continued, the number of subcommittees was increased to ten with separate Analog and RF Subcommittees in 2007.

As the decade advanced, the continued march of Moore's Law drove a split in the digital design world. One direction was to focus on the highest speed and performance possible from microprocessors; the second direction was to focus on energy efficiency for low-power applications, such as in cell phones and wireless networks. Thus, in 2008, the subcommittees evolved to reflect this change in design technique, and the old subcommittees of Digital and Signal Processing were replaced with two new subcommittees High-Performance Digital and Low-Power Digital bringing the total number of subcommittees to ten. To more accurately reflect the nature of paper submissions, the Low-Power Digital Subcommittee would be renamed as the Energy-Efficient Digital Subcommittee in 2011.

Today:

For ISSCC 2013, there are ten technical subcommittees: Analog; Data Converters; Energy-Efficient Digital; High-Performance Digital; Imagers, MEMs, Medical, and Displays; Memory; RF; Technology Directions; Wireless; Wireline. The International Technical Program Committee (ITPC) consists of 161 members, plus the Program Chair and Program Vice-Chair. There are 60 North American members, 54 Far East members, and 47 European members representing 23 countries. These individuals are from a mix of industry, academia, and research institutes. Together they reviewed 629 submitted papers and organized the Evening Events (5), Tutorials (9), and Forums (6) to create the ISSCC2013 Program.

Reference:

[1] "ISSCC – The Latter Years", W. David Pricer, ISSCC 50th Anniversary Supplement 1954-2003, p S8.





60 YEARS OF ISSCC TECHNICAL AND GENERAL CHAIRS

Year	Technical Chair	Affiliation	City	State	General Chair	Affiliation	City	State
1954	J. G. Linvill	Bell Labs			I. Wolf	RCA		
1955	H. E. Tompkins	Burroughs Corp			D. Fink	Philco		
1956	H. Woll	RCA Labs	Princeton	NJ	G. L. Haller	General Electric	Syracuse	NY
1957	G. Royer	IBM	Poughkeepsie	NY	A. L. Samuel	IBM		
1958	R. Baker	MIT Lincoln Labs	Lexington	MA	J. H. Mulligan, Jr	New York University	New York	NY
1959	A. P. Stern	General Electric	Syracuse	NY	J. Morton	Bell Labs	Murray Hill	NJ
1960	T. R. Finch	Bell Labs	Murray Hill	NJ	A. P. Stern	General Electric	Syracuse	NY
1961	J. J. Suran	General Electric	Syracuse	NY	T. R. Finch	Bell Labs	Murray Hill	NJ
1962	R. B. Adler	MIT	Cambridge	MA	J. J. Suran	General Electric	Syracuse	NY
1963	S. K. Ghandhi	Philco Scientific Lab	Blue Bell	PA	F. H. Blecher	Bell Labs	Murray Hill	NJ
1964	P. B. Myers	Marietta Corp	Baltimore	MD	E. O. Johnson	RCA	Somerville	NJ
1965	G. B. Herzog	RCA Labs	Princeton	NJ	J. B. Angell	Stanford Univ.	Stanford	CA
1966	G. B. Herzog	RCA Labs	Princeton	NJ	J. D. Meindl	US Army Electronics Cmd.	Fort Monmouth	NJ
1967	R. H. Baker	MIT	Cambridge	MA	J. S. Mayo	Bell Labs	Holmdel	NJ
1968	R. L. Petritz	Texas Instruments	Dallas	TX	J. S. Mayo	Bell Labs	Whippany	NJ
1969	R. S. Engelbrecht	Bell Labs	Murray Hill	NS	J. D. Meindl	Stanford Univ.	Stanford	CA
1970	T. E. Bray	General Electric	Syracuse	NY	R. S. Engelbrecht	Bell Labs	Holmdel	NJ
1971	R. R. Webster	Texas Instruments	Dallas	TX	J. A. Raper	General Electric	Syracuse	NY
1972	S. Triebwasser	IBM Research	Yorktown Heights	NY	R. R. Webster	Texas Instruments	Dallas	TX
1973	V. I. Johannes	Bell Labs	Holmdel	NJ	S. Triebwasser	IBM Research	Yorktown Heights	NY
1974	H. Sobol	Collins Radio	Dallas	TX	V. I. Johannes	Bell Labs	Holmdel	NJ
1975	W. D. Pricer	IBM	Essex Junction	VT	H. Sobol	Collins Radio	Dallas	TX
1976	J. H. Wuorinen	Bell Labs	Whippany	NJ	W. D. Pricer	IBM	Essex Junction	VT
1977	D. A. Hodges	Univ. of California	Berkeley	CA	J. H. Wuorinen	Bell Labs	Whippany	NJ
1978	J. D. Heightley	Sandia Labs	Albuquerque	NM	D. A. Hodges	Univ. of California	Berkeley	CA
1979	W. S. Kosonocky	RCA Labs	Princeton	NJ	J. D. Heightley	Sandia Labs	Albuquerque	NM
1980	J. D. Plummer	Stanford Univ.	Stanford	CA	J. A. Raper	General Electric	Syracuse	NY
1981	B. A. Wooley	Bell Labs	Holmdel	NJ	J. A. Raper	General Electric	Syracuse	NY
1982	P. R. Gray	Univ. of California	Berkeley	CA	J. A. Raper	General Electric	Syracuse	NY
1983	L. M. Terman	IBM Research	Yorktown Heights	NY	J. A. Raper	General Electric	Syracuse	NY
1984	P. W. Verhofstadt	Fairchild uProc. Div.	Mountain View	CA	J. A. Raper	General Electric	Syracuse	NY
1985	H. J. Boll	Bell Labs	Murray Hill	NJ	J. A. Raper	General Electric	Syracuse	NY
1986	A. Grebene	Micro Linear Corp	San Jose	CA	J. A. Raper	General Electric	Syracuse	NY
1987	R. Baertsch	General Electric	Schenectady	NY	J. A. Raper	General Electric	Syracuse	NY
1988	W. Herndon	Fairchild Research Ctr.	Palo Alto	CA	W. D. Pricer	IBM	Essex Junction	VT
1989	H. E. Mussman	AT&T Bell Labs	Naperville	IL	W. D. Pricer	IBM	Essex Junction	VT
1990	C. W. Gwyn	Sandia Labs	Albuquerque	NM	W. D. Pricer	IBM	Essex Junction	VT
1991	J. T. Trnka	IBM	Rochester	MN	W. D. Pricer	IBM	Essex Junction	VT
1992	A. R. Shah	Texas Instruments	Dallas	TX	W. D. Pricer	IBM	Essex Junction	VT
1993	R. C. Jaeger	Auburn Univ.	Auburn	AL	W. D. Pricer	IBM	Essex Junction	VT
1994	D. Monticelli	National Semiconductor	Santa Clara	CA	W. D. Pricer	IBM	Essex Junction	VT
1995	T. Tredwell	Eastman Kodak	Rochester	NY	W. D. Pricer	IBM	Essex Junction	VT
1996	F. W. Hewlett	Sandia Labs	Albuquerque	NM	W. D. Pricer	IBM	Essex Junction	VT
1997	R. K. Hester	Texas Instruments	Dallas	TX	J. T. Trnka	IBM	Rochester	MN
1998	J. Cressler	Auburn Univ.	Auburn	AL	J. T. Trnka	IBM	Rochester	MN
1999	S. S. Taylor	Triquent Semiconductor	Hillsboro	OR	J. T. Trnka	IBM	Rochester	MN
2000	R. Crisp	Rambus, Inc.	Mountain View	CA	J. T. Trnka	IBM	Rochester	MN
2001	G. Gulak	Univ. of Toronto	Toronto	Canada	J. T. Trnka	IBM	Rochester	MN
2002	W. Sansen	Katholieke Univ.	Leuven	Belgium	T. Tredwell	Eastman Kodak	Rochester	NY
2003	A. Chandrakasan	MIT	Cambridge	MA	T. Tredwell	Eastman Kodak	Rochester	NY
2004	A. Kanuma	Toshiba	Kawasaki	Japan	T. Tredwell	Eastman Kodak	Rochester	NY
2005	I. Young	Intel	Hillsboro	OR	T. Tredwell	Eastman Kodak	Rochester	NY
2006	J. Sevenhans	Consultant	Brasschaat	Belgium	T. Tredwell	Eastman Kodak	Rochester	NY
2007	J. Van der Spiegel	Univ. of Pennsylvania	Philadelphia	PA	T. Tredwell	Eastman Kodak	Rochester	NY
2008	Y. Hagihara	Sony	Atsugi City	Japan	T. Tredwell	Carestream Health	Rochester	NY
2009	W. Bowhill	Intel	Hudson	MA	T. Tredwell	Carestream Health	Rochester	NY
2010	A. Theuwissen	Harvest Imaging/Delft U.	Bree/Delft	Belgium	A. Chandrakasan	MIT	Cambridge	MA
2011	W. Gass	Texas Instruments	Dallas	TX	A. Chandrakasan	MIT	Cambridge	MA
2012	H. Hidaka	Renesas Electronics	Itami	Japan	A. Chandrakasan	MIT	Cambridge	MA
2013	B. Nauta	Univ. of Twente	Enschede	The Netherlands	A. Chandrakasan	MIT	Cambridge	MA

60TH ANNIVERSARY

A FAR-EAST PERSPECTIVE ON 60 YEARS AT ISSCC

Makoto Ikeda, University of Tokyo, Tokyo, Japan



Preamble:

As the Transistor Conference of 1954 evolved and expanded to become ISSCC, distinctly international contributions began to appear: Thus, in 1960, the first paper was presented from Japan [1], followed by growing numbers of others, 3 in 1961[2]-[4]. Then, in 1989, the first paper was presented from Korea [5], and in 1996, the first from Taiwan. [6]. Later, other contributions appeared from Hong Kong, China, Singapore, Australia, and India.

Along with the increasing paper submissions from the Far East, there began a corresponding participation by Japanese in the Program Committee: two in 1967 and three in 1970. Ultimately, a formal Far-East Program Committee was established for ISSCC 1971, consisting of 10 members including 7 Japanese, 1 Korean, 1 Taiwanese, 1 Australian.

In 1989, the first Plenary address from the Far East (Japan) was presented by H. Nakajima of Sony [7]. This was followed by a Plenary address given by S. Hiroe from Toshiba in 1991. Since 1993, annually, one of the Plenary speakers has been selected from the Far East. The first Plenary speaker from Korea was C.G. Hwang of Samsung [8] in 2002, and the first Plenary speaker from Taiwan was N. Lu of Etron [9] in 2004. In 2003, the first Program Vice-Chair from the Far East, Akira Kanuma, was chosen; he continued as the first Program Chair from the Far East for ISSCC 2004. Subsequently, these roles have been filled by two others from the Far East.

Far-East Paper Contributions:

For the past decade, the number of papers accepted from the Far-East region represent roughly one third of the total presented. As the decade proceeded, an increasing fraction of these came from outside Japan: for example, in 2004, 35% of FE papers came from countries other than Japan; and correspondingly, 65% in 2012, the number of papers from Korea exceeded that from Japan, with KAIST (Korea Advanced Institute of Science and Technology) being the largest contributor from the Far East. At ISSCC 2013, 40% of the total accepted papers are from the Far East, with KAIST providing the largest number of papers in the entire Conference!

Far-East Specialized Technical Contributions:

For the past decade, the Far East has led in several areas, notably memory, most particularly in NAND Flash scaling: from a 90nm 4Gb memory (Samsung) in 2004 [10], to a 19nm128Gb memory (Sandisk, Toshiba) in 2012 [11], maintaining a 3 \times annual capacity increase. At ISSCC 2013, world leading memory techniques will be presented from the Far East, including the world's largest ReRAM (32Gb), from Sandisk/Toshiba [16]; the world's smallest SRAM cell (0.081 μm^2), from TSMC [17]; and the world's fastest DRAM interface (10Gb/s/pin), from Korea University [18].

The Far East has also led in improvement of image sensors, including the first Back-Side Illuminated (BSI) CMOS image sensor which was presented in 2006 by Sony [12]. Meanwhile, the pixel size of CMOS image sensors shrunk from 2.25 μm in 2004 (Matsushita) [13] to 1.4 μm in 2011 (Samsung) [14]. As well, the frame rate of CMOS image sensors was improved with 20Mfps being achieved in 2012 (Tohoku University) [15]. At ISSCC 2013, two 3-D stacked image sensors will be presented, one for ultra-high parasitic light sensitivity, from Olympus [19], and a BSI image sensor bonded on the signal processor through TSV to create smaller camera modules for mobile devices, from SONY [20].

Amongst other important contributions from the Far East, ISSCC 2013 includes the world's first fully integrated 60GHz CMOS transceiver chipset for WiGig, from Panasonic [21].

Program Chairs from the Far East:

For ISSCC 2003, Akira Kanuma (Toshiba) was selected as Program Vice-Chair; for 2004, he became Program Chair He was followed by the selection of Yoshiaki Hagiwara (Sony) for Program Vice-Chair of ISSCC 2007; he became Program Chair for 2008. Then, for ISSCC 2011 Hideto Hidaka (Renesas) was selected as Program Vice-Chair; he became Program Chair for 2012).

Far-East Contributions to Paper/Attendee Promotion:

The Far East Committee continues to encourage paper submission and attendance at ISSCC from its region through a variety of means: Press Conferences have been held in Tokyo, Seoul, Taipei, alternately Beijing or Shanghai, once in Bangalore and this year, for the first time, in Singapore; as well, other regional meetings and events have been held, including some which featured a talk on "How to Write a Paper for ISSCC", first presented by Jan Van der Spiegel at A-SSCC 2006

<https://submissions.miracrd.com/isscc2013/PDF/WritingISSCCpaperJVdS_Nov06b.pdf>

Far-East Initiative:

In 2007, the Far-East Committee initiated the Silkroad Award: this is presented annually at ISSCC to a student speaker from the Far-East region for his or her first ISSCC presentation. It is intended to encourage students, especially from emerging countries to submit their best ideas to ISSCC.

Conclusion:

Over the past decade, the Far-East Committee has continued with many of the traditions begun in earlier decades, while extending and expanding its efforts in promotion of participation by the Far-East circuits community in the diverse activities at ISSCC.

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FAR-EAST CHAIRS AND SECRETARIES

Year	Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country	Asst. Sec.	Affiliation	City	Country
1971	T. Sugano	Univ. of Tokyo	Tokyo	Japan								
1972	T. Sugano	Univ. of Tokyo	Tokyo	Japan	S. Hamada	NTT	Tokyo	Japan				
1973	S. Hamada	NTT	Tokyo	Japan	H. Mukai	NTT	Tokyo	Japan				
1974	S. Hamada	NTT	Tokyo	Japan	K. Kataoka	NTT	Tokyo	Japan				
1975-1976	Y. Tanii	Electrotechnical Lab	Tokyo	Japan	T. Sekigawa	Electrotechnical Lab	Tokyo	Japan				
1977-1978	M. Uenohara	Nippon Elect Co	Kawasaki	Japan	K. Ayaki	Nippon Elect Co	Kawasaki	Japan				
1979	M. Watanabe	NTT	Tokyo	Japan	K. Kataoka	NTT	Tokyo	Japan				
1980	M. Watanabe	NTT	Tokyo	Japan	K. Kurumada	NTT	Tokyo	Japan				
1981-1982	K. Kurokawa	Fujitsu	Kawasaki	Japan	H. Ishikawa	Fujitsu	Tokyo	Japan				
1983-1984	M. Nagata	Hitachi CRL	Tokyo	Japan	M. Kubo	Hitachi CRL	Tokyo	Japan				
1985-1986	Y. Takeishi	Toshiba	Kawasaki	Japan	Y. Nishi	Toshiba	Kawasaki	Japan				
1987-1988	H. Sasaki	NEC	Kawasaki	Japan	A. Morino	NEC	Kawasaki	Japan				
1989-1990	T. Sudo	NTT	Atsugi	Japan	S. Horiguchi	NTT	Atsugi	Japan	T. Wakimoto	NTT	Atsugi	Japan
1991-1992	T. Nakano	Mitsubishi	Itami	Japan	O. Tomisawa	Mitsubishi	Itami	Japan	K. Okada	Mitsubishi	Itami	Japan
1993-1994	H. Ishikawa	Fujitsu	Atsugi	Japan	S. Hijiya	Fujitsu	Atsugi	Japan	K. Yamashita	Fujitsu	Atsugi	Japan
1995-1996	G. Kano	Matsushita	Osaka	Japan	T. Baba	Matsushita	Osaka	Japan	S. Katsu	Matsushita	Osaka	Japan
1997-1998	M. Kubo	Hitachi	Tokyo	Japan	K. Shimohigashi	Hitachi CRL	Tokyo	Japan	K. Kimura	Hitachi	Tokyo	Japan
1999-2000	Y. Unno	Toshiba	Yokohama-City	Japan	A. Kanuma	Toshiba	Kawasaki	Japan	Y. Miyazawa	Toshiba	Kawasaki	Japan
2001-2002	H. Watanabe	NEC	Kawasaki	Japan	T. Arai	NEC	Kawasaki	Japan	M. Yamashina	NEC	Sagamihara	Japan
2003	Y. Hagiwara	Sony	Atsugi	Japan	M. Kataura	Sony	Atsugi	Japan	T. Yamazaki	Sony Electronics	San Jose	CA-USA
Year	Chair	Affiliation	City	Country	Vice Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country
2004	Y. Hagiwara	Sony	Tokyo	Japan	K. Iizuka	Sharp	Nara	Japan	J. Chung	Pohang Univ of Science & Tech	Pohang	Korea
2005-2006	K. Iizuka	Sharp	Nara	Japan	J. Chung	Pohang Univ of Science & Tech	Pohang	Korea	T. Kawahara	Hitachi	Tokyo	Japan
2007	J. Chung	Pohang Univ of Science & Tech	Pohang	Korea	T. Kawahara	Hitachi	Tokyo	Japan	S. Park	Samsung	Yongin	Korea
2008	J. Chung	Pohang Univ of Science & Tech	Pohang	Korea	T. Kawahara	Hitachi	Tokyo	Japan	H-J Yoo	KAIST	Daejeon	Korea
2009-2010	T. Kawahara	Hitachi	Tokyo	Japan	H-J Yoo	KAIST	Daejeon	Korea	M. Ikeda	Univ of Tokyo	Tokyo	Japan
2011	H-J Yoo	KAIST	Daejeon	Korea	M. Ikeda	Univ of Tokyo	Tokyo	Japan	M. Hamada	Toshiba	Kawasaki	Japan
2012	H-J Yoo	KAIST	Daejeon	Korea	M. Ikeda	Univ of Tokyo	Tokyo	Japan	K. Arimoto	Renesas Elect	Itami	Japan
2013	M. Ikeda	Univ of Tokyo	Tokyo	Japan	K. Arimoto	Okayama Pref Univ.	Okayama	Japan	J-Y Lee	Samsung	Yongin	Korea

60 YEARS OF ISSCC IN EUROPE

Willy Sansen, Katholieke Universiteit Leuven, Leuven, Belgium



Continuing globalization has transformed ISSCC into a truly international event. This is demonstrably the case with paper acceptance. About one third of accepted papers originate from Europe. Several countries such as The Netherlands, France, Germany, Belgium, and many more, each contribute routinely more than a dozen papers to the Conference annually.

European strengths in circuit innovation are especially evident in Analog, Mixed-Signal/Data Converters, and RF design, but also in application-focused areas such as Wireless and IMMD. Technology Directions has also attracted many European contributions, enhancing the visionary part of the Conference.

Since the regional distribution of membership in the Program Committee depends on the regional paper acceptance, the number of European Program Committee members has grown from around 30 to 47 in the past decade. Correspondingly, Europeans are increasingly participating as Subcommittee Chairs: Franz Dielacher (Infineon) was the first European Subcommittee Chair for Wireline from 2004 to 2011; Bill Redman-White (University of Southampton) for Analog from 2006 to the present; John Long (T.U. Delft) for RF from 2009 to 2010; Roland Thewes (T.U. Berlin) for Imagers, MEMS, Medical, and Displays from 2011 to the present; and Andrea Cathelin (ST Microelectronics) for RF from 2012 to the present.

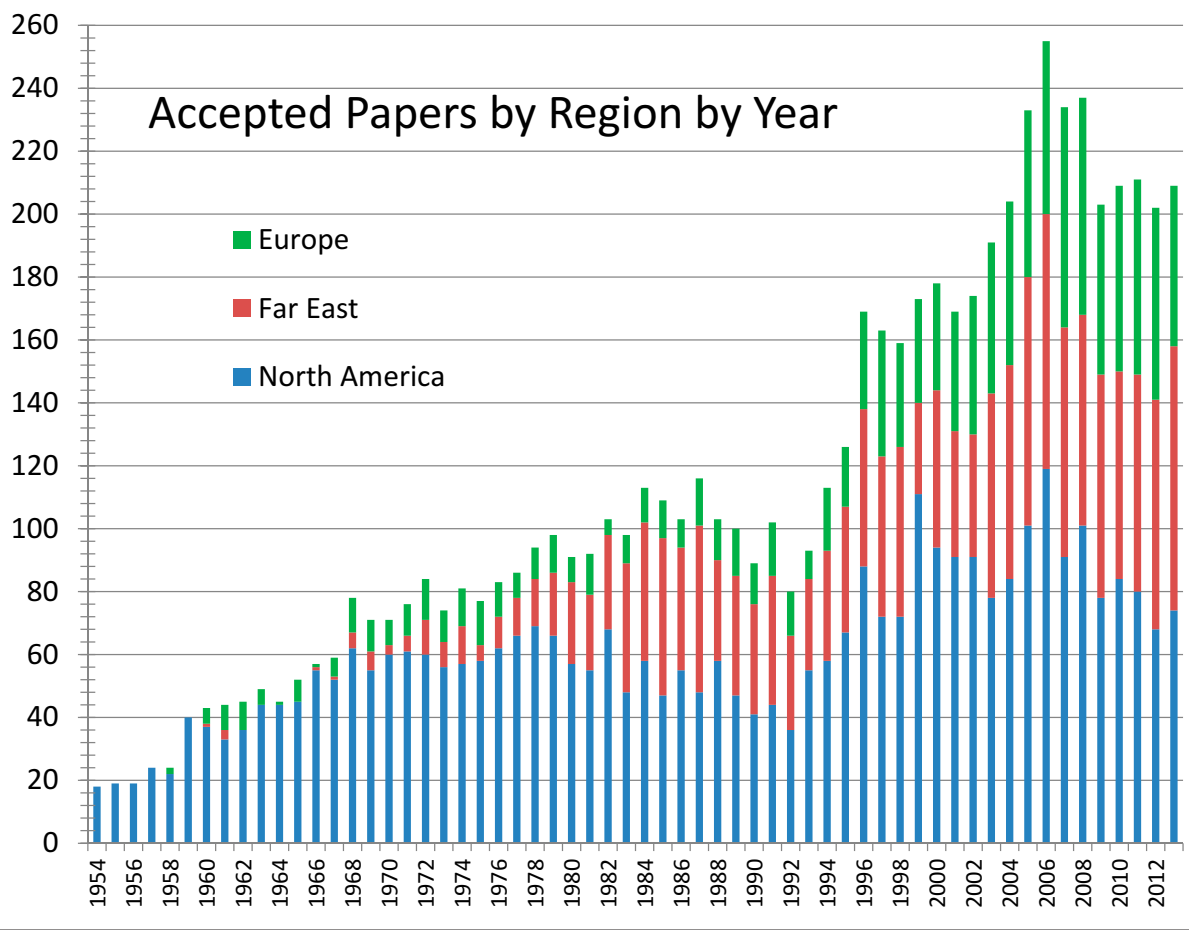
Also several Program Chairs have come from the European region: The first one was Willy Sansen (KU Leuven) in 2002; Jan Sevenhans (Alcatel) in 2006; Albert Theuwissen (T.U. Delft) in 2010; and Bram Nauta (University of Twente) in 2013.

The most important change in the operation of the European organization has been the creation of a succession format for chair/secretary selection. Then, in 2002, this was extended to provide a three member representation on the ISSCC Executive Committee: a Chair, a Vice-Chair, and a Secretary. Every second year, the Vice-Chair becomes Chair and the Secretary Vice-Chair, with a new Secretary chosen by the European organization. This rolling scheme provides the advantage that all three officers have ample time and opportunity to learn about ISSCC operations. Moreover, if one of them cannot attend a meeting, the two others are likely to be present. This arrangement began in 2003 with Jan Sevenhans as the first European Chair. The complete roster is listed in the table below. More recently, for ISSCC 2012, the change interval has been reduced from two years to one.

In conclusion, as seen from Europe, the success of internationalization of the Conference is a direct result of the leadership of its past and current Executive Chairs: Dave Pricer, John Trnka, Timothy Tredwell, and Anantha Chandrakasan. I wish to acknowledge the help of past European Chairs, Bram Nauta and Aarno Pärssinen in the preparation of this retrospective.

EUROPEAN CHAIRS AND SECRETARIES

Year	Chair	Affiliation	City	Country	Vice Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country
1971-1972	J. C. van Vessel	Philips	Nijmegen	The Netherlands					O. Folberth	IBM	Boeblingen	Germany
1973-1974	J. C. van Vessel	Philips	Nijmegen	The Netherlands					H. Ruechardt	Siemens	Munich	Germany
1975	O. Folberth	IBM	Boeblingen	Germany					H. Ruechardt	Siemens	Munich	Germany
1976	O. Folberth	IBM	Boeblingen	Germany					O. W. Memelink	Tech. Hogeschool Twente	Enschede	The Netherlands
1977-1978	N. C. de Troye	Philips Research	Eindhoven	The Netherlands					S. S. Roy	Inter. Computers, Ltd	Manchester	England
1979	N. C. de Troye	Philips Research	Eindhoven	The Netherlands					W. Engl	Tech. Hochschule Aachen	Aachen	Germany
1980-1983	H. H. Berger	IBM	Boeblingen	Germany					P. Jespers	Katholieke Univ.	Louvain	Belgium
1984-1985	J. Borel	Thomson EFCIS	Grenoble	France					P. Schouter	Thomson-CSF	St. Egreve	France
1986-1988	J. Lohstroh	Philips Research	Eindhoven	The Netherlands					J. Darneels	Bell Telephone	Antwerp	Belgium
1989-1994	K. Hoffman	Univ. der Bundeswehr	Neuburg	Germany					R. van de Plassche	Philips Research	Eindhoven	The Netherlands
1995-1996	R. van de Plassche	Philips Research	Eindhoven	The Netherlands					M. Degrauwe	CSEM	Neuchatel	Switzerland
1997-2000	R. van de Plassche	Philips Research	Eindhoven	The Netherlands					W. Sansen	Katholieke Univ.	Leuven	Belgium
2001	R. van de Plassche	Philips Research	Eindhoven	The Netherlands					J. Sevenhans	Alcatel	Antwerpen	Belgium
2002	R. van de Plassche	Philips Research	Eindhoven	The Netherlands	J. Sevenhans	Alcatel	Antwerpen	Belgium	A. Theuwissen	Philips Semicond.	Eindhoven	The Netherlands
2003	J. Sevenhans	Alcatel	Antwerpen	Belgium	A. Theuwissen	Philips Semicond.	Eindhoven	The Netherlands	R. Koch	Infineon Technologies	Munich	Germany
2004	J. Sevenhans	LEAsics of Broadband	Antwerpen	Belgium	A. Theuwissen	DALSA BV	Eindhoven	The Netherlands	R. Koch	Infineon Technologies	Munich	Germany
2005-2006	A. Theuwissen	DALSA BV	Eindhoven	The Netherlands	R. Koch	Infineon Technologies	Munich	Germany	Q. Huang	ETH Zurich	Zurich	Switzerland
2007-2008	R. Koch	Infineon Technologies	Munich	Germany	Q. Huang	ETH Zurich	Zurich	Switzerland	B. Nauta	Univ. Twente	Twente	The Netherlands
2009	Q. Huang	ETH Zurich	Zurich	Switzerland	B. Nauta	Univ. Twente	Twente	The Netherlands	A. Baschrotto	Univ. of Milan-Bicocca	Milano	Italy
2010	Q. Huang	ETH Zurich	Zurich	Switzerland	B. Nauta	Univ. Twente	Twente	The Netherlands	A. Pärssinen	Nokia	Helsinki	Finland
2011	B. Nauta	Univ. Twente	Twente	The Netherlands	A. Pärssinen	Nokia	Helsinki	Finland	E. Cantatore	Eindhoven Univ. of Tech.	Eindhoven	The Netherlands
2012-2013	A. Pärssinen	Renesas Mobile	Helsinki	Finland	E. Cantatore	Eindhoven Univ. of Tech.	Eindhoven	The Netherlands	A. Burdett	Toumaz Technology	Abingdon	United Kingdom



60 Years of Paper History by Region

Year	America	Far East	Europe	Year	America	Far East	Europe	Year	America	Far East	Europe
1954	18	0	0	1974	57	12	12	1994	58	35	20
1955	19	0	0	1975	58	5	14	1995	67	40	19
1956	19	0	0	1976	62	10	11	1996	88	50	31
1957	24	0	0	1977	66	12	8	1997	72	51	40
1958	22	0	2	1978	69	15	10	1998	72	54	33
1959	40	0	0	1979	66	20	12	1999	111	29	33
1960	37	1	5	1980	57	26	8	2000	94	50	34
1961	33	3	8	1981	55	24	13	2001	91	40	38
1962	36	0	9	1982	68	30	5	2002	91	39	44
1963	44	0	5	1983	48	41	9	2003	78	65	48
1964	44	0	1	1984	58	44	11	2004	84	68	52
1965	45	0	7	1985	47	50	12	2005	101	79	53
1966	55	1	1	1986	55	39	9	2006	119	81	55
1967	52	1	6	1987	48	53	15	2007	91	73	70
1968	62	5	11	1988	58	32	13	2008	101	67	69
1969	55	6	10	1989	47	38	15	2009	78	71	54
1970	60	3	8	1990	41	35	13	2010	84	66	59
1971	61	5	10	1991	44	41	17	2011	80	69	62
1972	60	11	13	1992	36	30	14	2012	68	73	61
1973	56	8	10	1993	55	29	9	2013	74	84	51

Data Compiled by: John Trnka

HIGHLIGHTS OF PRESS/PUBLICITY ACTIVITY OVER THE PAST DECADE AT ISSCC

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Preamble:

This article is meant to be an extension of my previous one which appeared in the ISSCC 2003 50th Anniversary Supplement [1].

While the obvious explicit role of Press-Relations activity at ISSCC has been to interest and inform members of the Press, who in turn would inform the technical and general public, there is some explicit sense that it was also intended as a means to less-direct other ends. Certainly, these days and for the past twenty years, the strategy has been to target less-technical management through the influence of the financial Press. For it is such upper management who exert financial control over the essential life-line to the success of ISSCC – the participation of volunteers, of authors, and of attendees – all of which depends on a positive corporate (financial) attitude. Thus, our goal has been to convince management that, even in hard times, ISSCC is where the action is, will be foretold, and will be demonstrated; In short, if informed early action leads to success, then ISSCC is where to invest!

Overview:

Press-material preparation resulting in the “Press Kit”, a booklet of some 180 pages or so, continued for ISSCC 2004 until 2009, in much the same way that had been defined earlier at its inception for ISSCC 1994.

The Far-East Press Conferences were expanded: the Tokyo meeting which began in 1995 continued; the Seoul meeting which began in 2003 continued; a Taipei meeting was initiated in 2005, and continues; a Beijing meeting was initiated in 2005, and continues with alternation between Beijing and Shanghai; a one-time-only meeting was held in Bangalore in 2006; this year, for the first time, a Press meeting was held in Singapore. For all the Far-East meetings, early Press Kit versions have been provided to the Far-East Regional Chairs for suitable translation.

In an effort to extend the emphasis on Press Meetings to Europe, there have been several attempts to replicate the Far-East experience in Europe: The first of these was for ISSCC 2004 when K.C. Smith, Laura Fujino, and Rudolf Koch held a press reception at Electronica 2004, in Munich, Germany; another was for ISSCC 2004 when Jan Sevenhans prepared an extensive European Press Release, emphasizing the European contribution to ISSCC past and present; and more recently for ISSCC 2012 the European Regional Chairs have issued a Press Release with a European flavor; this has been continued for ISSCC 2013.

For ISSCC 2010, in response to the need to handle what was perceived as an increasing load of the press-preparation process, Jim Goodman was added to the Press team as the Press Coordinator, with the role of easing the burden of press-material preparation faced by the Subcommittees at the October Paper-Selection meetings. For the first time, prior to the paper deadline in September 2009, a Press Poster/Flyer was created and mailed to Conference attendees from the previous two years. This poster/flyer included information on the Conference Theme, Plenary Speakers, Educational Events, and Evening Sessions.

As well, to assist in collection and final checking, a Press Committee was formed consisting of K.C. Smith, Jim Goodman, Makoto Ikeda, C.K. Wang, Eugenio Cantatore, and Ann O'Neill. Under Jim's direction, the process of Press-Kit preparation was simplified and a tighter Press Kit was prepared in October 2009, emphasizing a succinct two-sentence structure highlighting selected papers. While Press Copy (intended to provide well-formed articles which were originally intended for direct use by the relatively-non-technical Press) was retained, the earlier preparation by the Subcommittees of Featured-Paper pages (intended to assist the Technical Press, and Press Copy preparation) was eliminated. The Press Kit continued to be edited by a group consisting of K.C. Smith, Laura Fujino, Vincent Gaudet, James Haslett, Shahriar Mirabbasi, and Kostas Pagiamtzis.

For ISSCC 2012, Alice Wang replaced Jim Goodman. To attempt to further streamline the Press-Kit-preparation process, a small ad-hoc committee was struck to identify strengths and weaknesses of past processes, and identify future directions. As a result, the Press Kit format for ISSCC 2012 was further streamlined: In each Subcommittee, Press Designates were assigned to lead the Subcommittee Press effort; Press Copy was eliminated; Trend Charts and Essays which appeared occasionally in earlier versions were now emphasized as the major contribution from the Subcommittee, in addition to the usual Subcommittee Overview; Session Overviews (which are intended to appear later in the Conference Digest) were expanded to accommodate the removal of Abstracts in the Advance Program and Digest; Finally the format of the highlighted paper descriptions were provided in bullet form. The Press Kit continued to be edited by a group consisting of K.C. Smith, Laura Fujino, Jason Anderson, Vincent Gaudet, Glenn Gulak, James Haslett, and Kostas Pagiamtzis.

For general use, particularly by attendees at ISSCC 2012, an edited compilation of the Trend materials from the 2012 Press Kit was published in the IEEE Solid-State Circuits Magazine [2].

For ISSCC 2013, the Press Kit process initiated in 2012 continues. A trends-related overview article was again prepared for publication in the IEEE SSCS Magazine, this time, to appear in two installments.

Press-Directed Outreach in the Past Decade

(with timescale set by reference to the associated Conference year):

2004 to 2013: The annual Tokyo Press Conference continues.

2004: Second Seoul Press Conference (the first was for ISSCC 2003); Tim Tredwell gave an informative address on “50 Years of Integrated Circuit Technology: As Chronicled at the International Solid-State Circuits Conference”; European Press Release.

2005: First Taipei Press Conference, continuing annually; and an informal Beijing Preview Meeting.

2006: First Beijing Press Conference, continuing on alternate years; and a one-time-only Bangalore Press Conference.

2007: First Shanghai Press Conference, continuing on alternate years; and Far-East Regional Chairs attended the VLSI Conference in Bangalore.

2009: The policy which began in the 1990s of having the Conference Chair, the Press-Relations Chair and Publications Chair attend Far-East Press Conferences was discontinued.

2010: Jim Goodman joins the Press team; Press Flyer is first introduced; Press-preparation process was refined.

2012: Alice Wang replaced Jim Goodman as Coordinator; the Press-preparation process was further streamlined; European Press Release; Trends Article appeared in IEEE SSCS Magazine.

2013: First Singapore Press Conference; European Press Release continues; Trends Article appears in two installments in the IEEE SSCS Magazine [3].

A Paean to the Press:

On a more personal note, I feel a need to acknowledge the community of Press with whom I have interacted over the decades at ISSCC. They are an unusual group of people, from diverse backgrounds, often not narrowly technical, but equally often possessed of a great many insights into the technical world that surrounds ISSCC. By and large, they are a relatively social group, part of an extended community of individuals that we are fortunate to sample annually at ISSCC. In support of this view, ISSCC has a decades old policy of providing a special communal space in which the Press can interact amongst themselves and others, as they see fit. It is there that some of the excitement that they sense and share is available early in a pre-public forum. While the numbers of individuals who have passed through this space is enormous being more than 50 per year for decades, there are a great many stalwarts who con-



tinue to return in support of ISSCC. Of those many, a few include: Peggy Aycinena, Steve Bush, Dave Burskey, Peter Clarke, Mike Demler, Brian Fuller, Jim Handy, Tets Maniwa, Rick Merritt, Nic Mokhoff, Steve Ohr, and many others. To these and countless unidentified colleagues go our heartfelt appreciation of a job well and truly done for their awareness, enthusiasm, and vision of our joint future.

Final Reflection of 60 Years:

The Press have been, and continue to be, an important part of the Conference's success. Their influence has certainly contributed positively to the universal feeling of the importance of ISSCC to the solid-state industry, and the cognate creativity it supports. Without the influence of the Press, a great many important individuals, both technical and financial, would be far less informed! As one of them most recently observed: "As the granddaddy of all solid state conferences, it's the place where some of the most historic

circuit design announcements have been made over the years. Everybody wants to be there, and this past Monday (Editor's note: Presidents Day) nobody appeared to regret not having the day off – particularly during the plenary session when the cavernous hall was filled with thousands of people sitting in countless tidy rows, stretching off into the darkness. Even the keynote speakers commented on the impact of looking out across that sea of people. Yeah, ISSCC is really something". [4]

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- [4] Peggy Aycinena, <http://www10.edacafe.com/blogs/whatwouldjoedo/2012/02/22/people-isscc-mobs-flash-and-dash/>



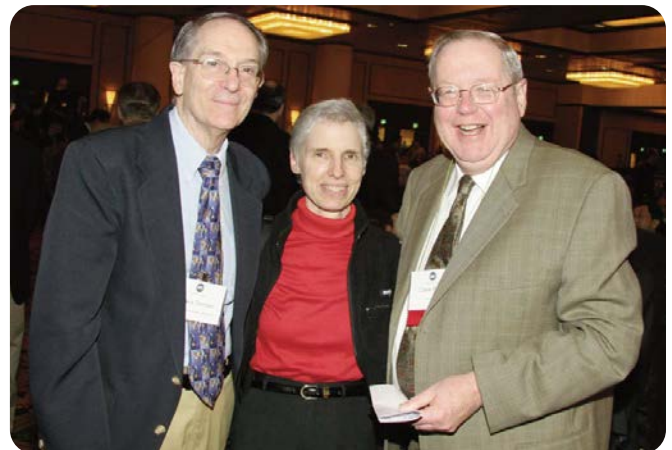
ISSCC 2003: Past Director of Conference Operations Diane Melton taking a well deserved rest.



ISSCC 2003 Behind the Scenes: AV Producer Mark Brazil with head audio technician William (Snoopy) Fuquay.



ISSCC 2006: Attendees collecting their Digests.



ISSCC 2006: Past IEEE President, Lewis Terman and his wife, Bobbie, with Past ISSCC General Chair, Dave Pricer.

THE SIXTH DECADE OF ANALOG AT ISSCC

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Introduction:

In many ways, trawling through the annals of ISSCC reveals a continuous history of the discipline of analog design, since analog techniques formed the core from the very beginning of ISSCC. In this short summary, we aim to focus on the recent advances, and provide a review the analog papers from the past decade.

While the years from 2003 to 2013 have seen tremendous turmoil in the semiconductor markets, the analog sector has shown remarkable resilience. The more jaundiced might say that this is because “it’s the analog guys who make the money, and the digital guys who spend it.” More diplomatically, analog remains an area where innovative design is at least as important as having the latest IC technology. As witness to this idea, excellent analog papers are being submitted to ISSCC in ever-larger numbers, and the analog sessions remain among the best-attended.



Thus, it is both difficult and unfair to try to select a few papers as being particularly meri-

torious; rather, we will seek to highlight those papers which exemplify the trends in design and applications that are driving progress in analog technology. At the beginning of the past decade, data conversion had come to dominate the “analog” sessions, but since then, far from being overtaken by events and technology, the burgeoning scope of the papers submitted reflects something of a renaissance in traditional analog design.



Amplifiers:

Despite being perhaps the most basic of electronic functional blocks, amplifiers continue to show innovation, both for large and small signals. For precision instrumentation and signal conditioning, clever chopping and ripple reduction techniques mean that CMOS is now a mainstream contender, yielding impressive noise and offset figures [1], as well as high input common-mode ranges [2]. At the other end of the scale, audio output stages have shown significant advances in the face of very different technology and application pressures. Portable applications now demand audio outputs in fine-geometry CMOS which give high efficiency and direct battery connection capability. New techniques have evolved using cascode structures that can reliably operate beyond the breakdown of a single nanometre-scale MOS device, and these can be seen in commercial Class-G and Class-D designs [3][4]. Integrated supply boosting is also evident to allow higher output power levels from fixed battery supplies [5]. When using high-voltage IC technologies, the increased efficiency of Class-D architectures also allows the complete integration of very-high-power audio output stages in a single die [6].

Very-high-bandwidth output drivers are also appearing on the boundary between conventional audio amplifiers and power-management applications to allow fast supply modulation in broadband output stages [7].

Power Management:

At the beginning of this decade, there were no power management papers being submitted, but it is now the single largest category in analog, and shows increasing levels of innovation and diversity as the dawn of the portable age has brought new imperatives of cost, size, and efficiency, to the requirements for power supplies.

Many papers have addressed the needs for supply conditioning for mobile applications, where a single Lithium-Ion battery supplies several required

domains at different voltage and current levels. In addition to the need to use mainstream IC technology, there has been a strong economic push to generate several independently regulated supplies, while using only a single external inductor [8]. There has also been a realization that in most applications good efficiency must be maintained over the entire load range, leading to new switching-mode and frequency-selection strategies [9], approaches increasingly facilitated by digital-controller implementations in nanometre technologies [10].

In the SoC world, the increasing demand for different supply domains within the same IC has created a need for locally regulated supplies with high efficiency, so as not to negate the power saving from supply-voltage scaling of digital subsystems. To date, integrated inductive converters have had little impact, but with the increase in the available capacitance per-unit-area, there is a growing trend to use fully integrated switched-capacitor converters with selectable ratios [11]. To match the needs of operation in nanometre technologies at low supply voltages, voltage reference designs also continue to advance [12].

In many applications, very-fast regulation response is needed, and in some, the supply must be modulated while retaining high conversion efficiency. To meet these challenges, hybrid combinations of linear and switched-mode supplies have appeared, trading the advantages of both approaches [13].

There is also a growing diversity in the power levels of the systems being addressed. Energy harvesting is seen as essential for many remote sensor systems, but it poses a range of challenges for their power management circuits. Recognizing that some transducers begin operation at very low voltages, designs have appeared that can self-start at impressively low input levels, and still deliver an output sufficient for conventional application circuits [14]. In the solar arena, maximum-power-point issues are well known, but there is an increasing need for floating regulators in a distributed structure to maximize the overall output of a solar array [15]. Going in the other direction, wireless charging applications are appearing, requiring high efficiency moderate power rectifiers able to operate with loose coupling at high frequencies [16]. LED-lighting control is also a rapidly growing area. New designs presented are capable of direct connection to the AC line voltage, while providing well-controlled power factor and harmonic loads to meet utility supply restrictions [17].

PLLs and Oscillators:

Frequency references and clocks in general are a nearly universal requirement, stimulating a steady stream of innovative designs. With the ubiquity of low-power applications, there is a growing need for extremely low-power reference oscillators to keep time while the host is in a standby or sleep mode, ready to respond to a wake-up input [18]. The pressure to eliminate the usual quartz crystal has also led to exploiting intrinsic thermal time constants to control a reference [19].

The fractional-N PLL with a $\Delta\Sigma$ controller has become the architecture of choice in many communications systems. In addition to further reducing spurious tones [20], there remains the challenge of reducing the residual in-band noise due to phase-quantization errors, and many novel techniques have been presented to address this issue [21].

Filters:

While filters have traditionally featured strongly in analog, there is less emphasis on them these days, as many established low-frequency applications can be handled more efficiently by a combination of ADC and DSP blocks. Nonetheless, where the power and dynamic range constraints are not achievable in this way, analog filter designs continue to develop into previously unexplored areas. In the communications arena, there is usually a trade-off between the degree of bandwidth reduction performed in the analog domain versus the power needed to perform digitization over a matching bandwidth,

be it baseband or RF. The goal posts continue to move with advances in technology, but as new higher-frequency and higher-bandwidth applications appear, these trade-offs must still be made, and tunable analog filters can now reach up to 10GHz bandwidth [22]. In a practical system, there is often the need for filters with high spurious-free dynamic range and low power consumption. One can exploit the changing signal dynamics in most channels by switching active elements into the circuit only when needed for the linearity and noise demands of the signal amplitude present, and disable these otherwise, with significant power saving [23]. The linearity performance of novel N-path filters means that they are now to be seriously considered as replacements for SAW filters in receiver architectures [24].

At the low-power end of the scale, 0.5V operation has been achieved in standard CMOS technology [25], while radical new ideas have emerged to completely change the variables in the signal-processing flow, and replace conventional op-amp or gm-C integrators with variable oscillators [26].

Conclusions:

Far from being sidelined by the march of digital, analog at ISSCC has seen a great expansion in scope, both in terms of the breadth of application areas and in the range of technologies used. Innovation in the analog IC design world is clearly in excellent health, and over the next decade we can look forward to advances in an even-wider range of applications!

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ISSCC 2010: Speaker and Committee Registration in the Nob Hill Room.



ISSCC 2010 : Alice Wang, current ISSCC Press Coordinator, with other attendees between sessions.

ISSCC DATA CONVERTER TRENDS 2004-2013

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**Introduction:**

In the early 2000s, skeptics argued that most data converter architectures had matured, and may begin to suffer from power inefficiency as we scale into deep sub-micron CMOS. The past decade of innovation in data converters has clearly knocked such arguments out of the ball park, and has shown how clever circuit and architecture design can in fact draw benefits from further process scaling. This is clearly seen in Figure 1, which highlights the continuing trend toward lower energy per Nyquist sample for recently published A/D converters.

**ADCs:**

An interesting consequence of the creativity and improvements seen over the past decades is the increasing competition among ADC architectures. While it was relatively straightforward to make architectural decisions in 2003, today's ADC designer is confronted with an overlapping design space that offers multiple solutions that are difficult to differentiate in their suitability. For example, the design space for pipelined architectures has been encroached by oversampling converters with

ever-increasing bandwidths, as well as by time-interleaved converters using Successive Approximation Register (SAR) sub-ADCs (see the detailed discussion below).

Nyquist ADCs:

One of the most significant developments in Nyquist-rate A/D conversion has been the dramatic revival of the SAR architecture, triggered in part by Draxelmayr's ISSCC 2004 paper [1]. Against the common wisdom at the time, this work showed that a time-interleaved SAR array can achieve flash-like speeds with low energy consumption, leveraging the high density and fast switching speeds of nano-scale CMOS. Following this presentation, a slew of papers on successive approximation converters appeared at ISSCC (see Figure 2). Indeed, one entire session at ISSCC 2010 was dedicated to this topic. Most impressively, it was shown that the time-interleaved SAR architecture can deliver an aggregate speed of 40GS/s at 6 bits [2] for optical communication, or it can digitize the entire cable TV spectrum at 2.6GS/s at 10-bit resolution [3]. Today, innovation in SAR ADC design is still alive and continues to harvest the benefits from further process scaling. This is evidenced by an ISSCC 2013 paper that describes a 1.2GS/s design in 32nm technology [4]; this is the fastest single-channel 8-bit SAR ADC reported to date.

Challenged by the impressive energy efficiency and scaling robustness of SAR converters, the designers of pipelined ADCs continued their search for "opamp-less" amplification techniques. Following the proposals of open-loop and low-loop-gain approaches [5][6][7], comparator-based [8], fully-dynamic [9], and ring-amplifier-based [10] approaches helped in keeping the power dissipation of pipelined ADCs competitive. In the context of high-end wireless applications, the pipelined architecture has seen less competition, and has proven to be the only contender that can deliver 250MS/s at a resolution of up to 16 bits [11]. With time-interleaving and proper calibration, we have seen that the pipelined architecture can even be pushed to 1GS/s at 12 bits [12]; a performance level that is hard to reach with any other topology.

Oversampling ADCs:

Over the past decade, the advances in performance parameters of delta-sigma modulators have been primarily driven by the increasing data rates of modern communication systems. This was supported by opportunities provided by advanced CMOS technologies to improve bandwidth and digital signal processing capabilities. The proliferation of various cellular standards has resulted in the design of extremely versatile delta-sigma modulators with band-

widths scalable over several orders of magnitude [14]. The trend towards smaller feature size of CMOS technologies has enabled sampling frequencies to increase from several hundreds of MHz up to 4-to-6GHz in recent work [15][16][18]. Signal bandwidth has gone hand-in-hand, exceeding the 100MHz barrier [15][16]. This has been made possible by key architectural and circuit innovations, such as excess loop delay compensation [13], continuous-time filter implementations [13] to [19], and multi-bit topologies [13][15][16][17] employing digital calibration [17] or dynamic element-matching techniques. While the bandwidth of delta-sigma modulators has been pushed from the kHz to the MHz range, state-of-the-art power efficiency figures have been demonstrated under 100fJ/conversion-step [13][19], and as low as 28fJ/conversion-step, recently [21]. Lately, a revival of the bandpass delta-sigma converter concept targets RF-domain applications [16][20], moving the delta-sigma modulator closer to the input of the receiver chain.

DACs:

In the area of D/A conversion, the work of the past decade delivered speeds of several GS/s in high-resolution parts optimized for data-communication applications [22][23][24]. The onslaught of these developments was especially visible in the 2004-2005 timeframe, when one dozen high-speed DACs were published at ISSCC. Equally impressive were the developments in oversampling audio DACs, which now achieve distortion levels of -100 to -120dB in processes down to 45nm [25].

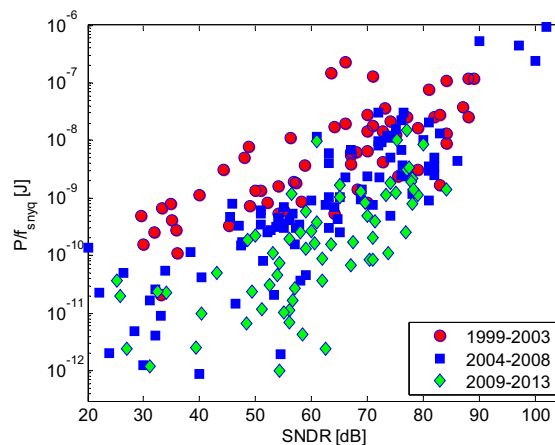


Figure 1: Energy per A/D conversion of ADCs published at ISSCC.

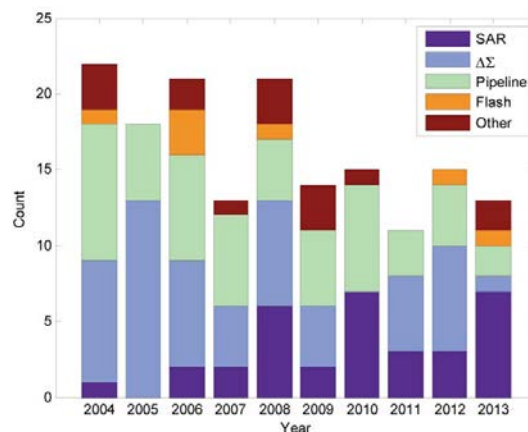


Figure 2: Underlying architectures of ADCs published at ISSCC.

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ISSCC 2003: ISSCC Pioneers, Arthur Stern and Jerry Suran, at the ISSCC 50th Anniversary Luncheon.



ISSCC 2003: Charlie Sodini, Bruce Wooley, Anantha Chandrakasan, and Ian Young with Gordon Moore.



ISSCC 2010: Breaking for lunch.

60TH ANNIVERSARY

DIGITAL CIRCUITS – A TEN YEAR RETROSPECTIVE WITH A GLIMPSE OF THE FUTURE

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**Introduction:**

The past ten years can be characterized as a transitional decade, where classical-CMOS-device scaling has given way to a new era of scaling [1], characterized by the integration of new materials and structures to improve device performance, reduce power, and enable continued scaling. Digital transistors continued to improve in performance, with the addition of strained silicon at the 90nm technology node in 2003 [2]. The next step was to address the need to scale the gate oxide thickness. The 45nm technology in 2007 saw the first high- κ hafnium-based dielectric with metal-gate transistors for improved performance and reduced leakage [3]. Tri-Gate transistors were introduced at the 22nm technology node in 2011, providing a steeper sub-threshold slope compared to traditional planar MOSFETs that improves their ability to operate at lower voltages to reduce active power [4]. The number of copper interconnect layers continues to grow, with 15 reported this year in high-end server processors [5].

As scaling proceeds, variability continues to increase [6]. Correspondingly, more analog

functions are being replaced by equivalent digital circuits, while SRAM 6-transistor cells are typically designed to function with “assist” circuits [7][8], or have been fully replaced with dual-port 8-transistor cells [9]. For clock generation, all-digital Phase-Locked Loops (PLLs) and delay-locked loops (DLLs) provide lower jitter and better frequency control than the well-known analog self-biased PLLs, at much lower power and area [10].

Digital Processor Directions:

Single-chip-microprocessor transistor count blew past the 1 billion mark in 2005, with most recent server processors exceeding 3 billion devices. While high-end server processors continue to push frequency (with a 5.5GHz processor [5] reported at ISSCC-2013), mainstream processor frequencies peaked early in the decade, as limited by power constraints. Consequently, performance increases have been obtained with improved micro-architectural techniques and multi-threading. Dual- and quad-core processors are the norm for everyday computing devices. However, specialized processors have incorporated hundreds of cores on a single die. The trend toward higher integration continues with graphics and networking units being absorbed into the main processor die to enable higher performance and lower power. Gaming systems [11] and Graphics-Processing Units (GPUs) [12][13] have augmented general-purpose processors with SIMD units to provide substantially higher peak performance for targeted applications. Essentially, all modern micro-processor designs have become System-on-Chip (SoC) heterogeneous constructs that integrate compute, graphics, audio, video, and communications units into a single monolithic die.

Focus on Power:

Power consumption continues to be the primary design constraint in all digital circuits, and is a limiter to overall peak performance. While some desktop client processors can exceed 100W, mobility and battery life requirements are pushing laptop, tablet, and phone processors toward lower and lower power targets, as consumer devices evolve to meet the demands of the steadily increasing wireless data bandwidth. Server processor power is also decreasing to support increased parallelism at the expense of single-thread performance in thermally-constrained systems. In the past decade, we witnessed a “back-to-the-future” trend with the introduction of “cloud”-computing server systems to allow monetization of centralized computing resources through the Internet. In addition to lower-power targets, smaller transistor geometries and reliability have driven operating voltages lower. Power-gating devices have

become ubiquitous in order to manage leakage, with nearly a dozen voltage domains reported on a single die [14], while power-management systems have been incorporated on the SoC to manage the trade-off of performance and power consumption based on application demands. Near-Threshold Voltage (NTV) circuits enable very low power operation. To operate at such low voltage levels, standard-cell libraries must be re-designed to eliminate gates which would have extreme delay variations, such as complex gates with four or more stacked transistors or transmission-gate multiplexers with four or more inputs [15]. Heterogeneous processors [16] have been made that combine a high-performance core and an energy-efficient core to maximize the battery life while supporting bursts of computationally intensive tasks.

Future Directions:

A key trend going forward is 3D integration of processors and memories using Through-Silicon Vias (TSVs). While power delivery and thermal effects are important challenges, 3D-stacked circuits provide impressive density improvements with very high bandwidth to memory [17]. As well, heterogeneous processors are mixing serial-thread-optimized general-purpose cores with throughput-optimized SIMD cores to provide better power efficiency and higher system performance. Security is becoming a key requirement for digital computing, with Physically Unclonable Functions (PUFs) used for secret-key generation and along with hardware random number generators. High-performance computing is increasingly bandwidth limited. Optical interconnects are beginning to address this bandwidth bottleneck as photonic technology integration becomes cost effective.

In today’s power-constrained designs, self-adapting circuits are used to minimize voltage and frequency margins and avoid over-design.

Optimal designs require accurate sensing mechanisms to control processor metrics by detecting various variations: device, supply noise, operating temperature, and activity. Future processors will incorporate adaptive and dynamic power systems, temperature and voltage management systems, as well as integrated voltage conversion. Sensors will be integrated within compute cores to make them aware of the user and the surrounding environment. Correspondingly, broad collaboration across multiple disciplines, including architecture, circuits, graphics, process technology, packaging technology, platform and system design, energy efficiency, drivers and application software, will be required for continued integration and performance growth.

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IMAGERS MEMS AND SENSORS, MEDICAL DEVICES AND DISPLAYS – A DYNAMIC DECADE

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The common thread that unites the constituents of IMMD is a concern for interfaces with the physical world - both the human body and its environment. Conventionally, we consider this broad area in terms of both tool and task: imagers, MEMS and sensors, medical, and displays, as discussed in the following subsections:

Imagers:

Following the first CCD and CMOS imager papers that appeared at ISSCC in the 1970s and 1980s [1], commercial production volume

and related market size, pixel count, numbers of applications, and image quality have all dramatically increased. Now, for consumer-electronics products such as cell phones, tablets, and laptops, the integrated camera has become a standard feature with photodiode-array diameters down to the mm range [2]. At the same time, high-end chips with array diagonals up to several centimeters are available for semi-professional and professional photography [3], moreover wafer-level cameras for scientific applications [4], and devices specifically optimized for high-speed imaging purposes [5].

Although a higher pixel count does not necessarily translate into better images, the pixel race is still ongoing: Whereas smart phones already use around 5 to 10 Mpixels, in the high-end domain, the 100 Mpixel hurdle was overcome some years ago [6]. Rather, currently, a major contribution to image quality in cameras is based on the addition of digital signal processing techniques: While earlier CMOS- and CCD-based imagers consisted solely of an array of photosensitive devices and an analog signal-transmission chain [1], evolving advanced devices combine the analog frontend with A/D conversion, along with digital circuitry and memory for massive image post-processing, all on a single chip [2]-[6]. Moreover, non-pixel-count-related advances in manufacturing technology have established more-efficient light-harvesting through Wafer-Level Optics (WLO) and BackSide-Illuminated (BSI) operation [7]-[10].

Last, but not least, a number of medical and scientific imaging applications (for example, single-photon counting, time-of-flight detection, 3D and ultra low-light application) have been enabled through integration of Single-Photon Avalanche Diodes (SPADs) within arrays on CMOS chips equipped with appropriate readout circuitry [11]-[13]. The most recent achievements include 3D vision by using techniques such as on-chip lenticular lenses and buried sub-wavelength optics [14].

MEMS:

MEMS have very successfully impacted the consumer area [15]-[17]: Accelerometers and gyroscopes are now a natural part of computers, mobile, and gaming devices. Moreover, MEMS devices are important components in automotive and industrial applications [18]. Digital light projection using micro-mirror arrays has become a standard in image-projecting systems, such as table-top projectors, TVs, cinema projectors, and portable handheld devices [19]. Also integrated microphones and pressure sensing devices in general have become important in many commercial applications [20].

MEMS are increasingly found in many other areas: In the RF domain, MEMS have established themselves as switches and filters; MEMS-based frequency references have shown outstanding performance at reasonable cost, and thus enjoy successful commercial exploitation [21][22]. Other MEMS developments are occurring in emerging fields including biomedical, chemical, and microfluidic applications [23].

Sensors:

The enhanced performance of smart sensors has been achieved by the integration of basic sensing elements with frontend and signal processing circuitry, compensating for errors, artifacts, and noise. As well, these additions allow for more efficient trimming and calibration procedures (such as one-point vs. two-points), translating into significant cost advantages [24].

Temperature sensors based on the well-known bandgap topology have continuously developed towards increased resolution and lower power consumption [25][26]. Moreover, recent publications at ISSCC have shown that this principle is still successfully applicable to most advanced CMOS technologies used in microprocessors [27]. Besides this, high-accuracy temperature sensing has also been demonstrated based on the phenomenon of heat diffusion in Silicon and SiO₂, allowing for temperature ranges up to 200°C [28].

Medical Devices:

In the biomedical domain, significant progress has been reported: Although, a commercial breakthrough has not yet been achieved, electronic microarrays for bio-molecule detection have proven feasible based on various principles [29]-[31]. Recently, devices for DNA sequencing have been suggested whose goal is to make the sequencing process much faster at lower cost compared to today's standard techniques [32].

Cell handling, manipulation, and sorting, have been demonstrated with a spatial resolution on the order of tens of microns. This is accomplished on CMOS chips using arrays of buried electrodes to apply dielectrophoretic forces [33]. In-vitro neural tissue interfacing with cultivated cells or brain slices has been demonstrated using arrays of tens of thousands of interfacing sites on a few mm² with spatial resolution in the 10µm range [34][36]. They allow the recording of both maps and movies of neural activity, providing stimulation of the tissue.

Brain machine interfaces with around one hundred channels have been used extensively in research concerned with *in-vivo* neural tissue monitoring [37]. In view of the restriction of mW power dissipation or below in live tissue, and the specific goals of these studies, such systems are specifically tailored for the best tradeoff between power, noise, and spatiotemporal resolution [38][39].

Major improvements have been reported in the area of prosthetic and implantable devices: "Classical" devices such as pace makers have become increasingly smart through intelligent co-operation with sensor systems monitoring human body parameters and implementing related algorithms [40]. Cochlear implants have benefited from technology development through increasing the number of sites and improved computational power per chip area and power dissipation [41][42]. Retinal prostheses with up to a thousand stimulation sites are in clinical trials worldwide, and successful results to restore basic vision capability have been reported by various groups [43][44]. Devices for deep-brain stimulation were approved for therapies applied to humans in 2009, and have been demonstrated to help Parkinson and chronic-pain patients to significantly reduce their symptoms [40][45]. Further developments are directed at closed-loop epileptic-seizure control [46] Recently, optogenetic approaches have proven that opto-electrical interfacing with the brain may open the way to new horizons for research and prosthetic applications [47].

In other directions, such as in the areas of EEG, ECG, or EMG measurements, ICs help to simplify patient monitoring, and make it more convenient for patients and physicians [48], or enable individuals with severe physical disabilities to control and interact with their environment by means of free-tongue motion [49].

Displays:

During the past decade, flat panel TVs and many mobile applications have seen a transition to the use of 10b driver ICs. The related DACs and driver ICs must consider a wide variety of boundary conditions, including: Speed, area, layout aspect-ratio, and degradation compensation circuitry (for AMOLED screens). Frequently, segmented and hybrid topologies are used to meet these needs [50]-[52]. Moreover, the marked increase in mobile applications has driven the development of high-performance low-power touch-screen controllers and drivers [53][54]. As well, near-to-eye applications have added further functionality to the display world by introducing eye-tracking as a new feature in bi-directional devices [55].

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ISSCC 2003 Plenary Session: Gordon Moore presenting at the 50th Anniversary

60 YEARS OF MEMORIES AT ISSCC

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Introduction:

Solid-state memories have experienced tremendous growth over recent decades, benefiting from Moore's Law of technology scaling. The total annual revenue of semiconductor memory now exceeds 50 U.S. billion dollars. Throughout this rapid growth, ISSCC has served as the premier forum in which industry and academia share the latest advancements in memory. A major chronicle of memory publication at ISSCC was well presented by Jagdish Pathak in the 50th Anniversary Commemorative Digest [1]. As we now com-

memorate the 60th year of ISSCC, I will focus on the key new developments in major areas of memory at ISSCC over the past decade.

Mainstream memory technologies continue to be SRAM, DRAM, and floating-gate-based Flash for increasingly broad applications. Memory density has been growing at a rate of 2 \times per one-to-two-year span across the various technologies, driven by strong demands for higher performance and lower cost. However, as the geometry of storage cells shrinks well below the 100nm regime, continuous scaling has started to face many challenges on multiple technical fronts, often requiring advanced solutions from device technologies, new circuits, and system-level optimization. Meanwhile, emerging memory technologies have made significant strides toward real product applications, which could very well lead to viable alternatives to conventional memories in the future.

SRAM:

Embedded SRAM continues to serve as the work-horse for embedded applications due to its superior performance and full-compatibility with logic process technologies. SRAM scaling has followed logic-gate density scaling over the decades, which has spurred a wide range of applications from high-performance computing to low-power hand-held devices. While transistor variations pose a big challenge to maintain adequate read-write margin in the ever-shrinking 6-transistor bitcell, the demand for low-voltage operation for battery-powered applications has added a new dimension in SRAM scaling challenges. A number of SRAM papers at ISSCC in recent years have focused on advanced circuit techniques to help improve design margins for low-voltage operations [2] to [4]. Many of these circuit techniques have centered on two fronts: the use of different voltage levels to mitigate the read-write conflict, and the adoption of dynamic adaptive design to minimize the impact of process variations. Meanwhile, the introduction of new transistor technologies such as hi-k metal gate and 3D tri-gate transistors have also proven to be very effective in overcoming the scaling challenges to achieve excellent density, performance, and power. A recent SRAM publication at ISSCC demonstrates, for the first time, a large SRAM array design with the bitcell area below 0.1 μm^2 in a 22nm tri-gate CMOS technology [5]. The future of SRAM scaling will largely depend on continuous innovations in both underlying transistor technology and advanced circuit design.

NAND Flash Memory:

NAND overtook NOR in nonvolatile solid-state memory at the turn of this century, and has clearly become the story of Flash memory over the past decade [6]. The explosive growth in NAND has been driven largely by various mobile consumer-electronic developments, such as the MP3 player, digital camera, and USB drive. The most recent frontier for NAND application is providing large storage memory in mobile systems that have been dominated by Hard-Disk-Drives (HDD). The rapid reduction in cost-per-bit derived from technology scaling has enabled NAND to gain rapid traction in this new area, which in turn is fueling continuous growth in NAND-technology scaling. Due to its highly-regular array geometries, NAND has outpaced the density scaling of all other memory in the past decade with about 2 \times capacity increase every year. This trend likely will continue in the foreseeable future through innovations in both array design and technology scaling. A recent NAND publication has bro-

ken the 20nm barrier in technology feature size and demonstrated a capacity of 128Gb/die with a 3-bit/cell architecture [7] [8].

But, relentless technology scaling in NAND is pushing the fundamental limits in current NAND cell technology and circuit design, including tunneling leakage of the memory cell and coupling-induced signal loss. These challenges are further compounded by the desire to store multiple bits per cell as was introduced in the mid-1990s [9] to increase effective memory density. More-advanced cell-programming algorithms, along with comprehensive system-level error management will play increasingly important roles as NAND technology scaling moves beyond the 20nm generation [10][11].

DRAM and High-Speed Memory Interface:

DRAM has always played a critical role in closing the gap between high-performing compute engines (such as CPUs), and storage memory. The demand for high-bandwidth memory has experienced rapid growth over the past decade due to many new applications in visual computing, including high-resolution graphics and displays for consumer electronics. While DRAM capacity continues to grow at about 2 \times every other year, much of the recent technical focus has been on the memory interface in order to achieve high memory bandwidth. This trend is clearly reflected at ISSCC with a large number of publications in recent years concentrating on DRAM interface design. A recent publication at ISSCC revealed a design of 4Gb DDR4 SDRAM with 3.2Gb/s/pin for high-performance application [12]. The new design is based on a 30nm DRAM technology with stacked capacitor. For ultra-high-bandwidth needs in graphics, a GDDR interface has been developed and is able to achieve up to 7Gb/s/pin performance with advanced I/O circuit techniques [13]. While DDR4 along with GDDR are leading the way for high-performance applications, a low-power DRAM interface has also become increasingly important for a wide range of mobile applications. Voltage scaling remains as a key to reducing I/O power. A recently reported industry-leading 4Gb LPDDR3 r achieves up to 1.6Gb/s/pinat 1.2V through the use of various advanced interface circuits in 30nm technology [14].

Recent technology innovations in Through-Silicon Via (TSV) has opened up a new class of memory-interface design for achieving high-bandwidths at much lower power levels [15]. TSV enables connection with a very large number of pins between memory and memory, and memory and logic. A more recent ISSCC publication reported 800Mb/s/pin bandwidth with only 283 μW power consumption [16]. As conventional DRAM technology faces more and more challenges from technology scaling, TSV and other advanced 3D interfaces can pave the way for more effective 3D IC integration in addressing future demands in density and bandwidth requirements.

Emerging Memories:

The pursuit of advanced memory beyond conventional charge-based technologies can be traced back to the very early days in ISSCC history [17]. Various new forms of memories, often referred to as "emerging memories", have attracted intense efforts from industry and academia in recent years, as conventional technologies face more and more difficulties in scaling: Phase-Change-Memory (PRAM) is leading the way in achieving the highest level of integration to date. An 8Gb PRAM design recently revealed at ISSCC has achieved up to 40MB/s program bandwidth [18]. The high-bit-density nature of PRAM has made it a strong candidate to potentially replace floating-gate Flash memory. Magnetic Memory (MRAM) has long been an interest for random-access memory due to its fast access time and excellent endurance [19]. Most recently, Spin-Transfer-Torque (STT)-based MRAM has received the most attention, as it overcomes the power and density scaling challenges in conventional MRAM [20]. More-advanced circuit and architecture techniques have driven the MRAM density up to 32Mb in 90nm technology [21]. Resistive RAM (ReRAM) is the latest to join the long list of emerging memories for future applications [22] [23]. In spite of the significant progress with new memory developments, there are many technological hurdles remaining before any of these new memories can be deployed in real products. The intensity of the race against conventional memories will certainly grow stronger as the lucrative market for flexible non-volatile memory dramatically expands.

Overall:

In summary, ISSCC has remained true to its founding spirit for 60 years in providing the global forum for experts to share the latest knowledge and progress in solid-state memory. Given the challenges and new opportunities facing the memory industry, ISSCC will, without doubt, continue to play a critical role in advancing memory developments in the future.

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WIRELESS AND RF: THE RECENT YEARS

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Introduction:

The wireless-communication industry has experienced explosive growth since the 1990s, with an increased acceleration in the past 10 years. This has been propelled primarily by higher integration, lower cost, and new technology developments. The key enabler for mobile handheld devices is the wireless-connectivity capability; without this, these devices can only be used as a handheld "computing" or "storage" device. With high-speed wireless links, users have instant access to unlimited information/data on the Internet; hundreds and thousands of "killer" apps have since been developed on these devices to provide even greater services to the end users.



If you tear down a modern day smartphone, you will find devices that provide wireless connectivity in the following three categories: Wireless WAN, Wireless LAN, and Wireless PAN. WWAN (usually referred to as 2G/3G/4G cellular standards), provides wide-area network and voice access at speeds of several Mb/s over an area of several miles radius. WLAN (also known as IEEE 802.11) has become the de facto wireless standard which

is capable of 10 to 1000Mb/s access speed covering distances up to hundreds of meters. WPAN (such as Bluetooth) has been used as a low-power, short-distance wireless connectivity method to allow ~1Mb/s of data with very-low power consumption. Together, these provide users with a seamless wireless access experience virtually everywhere in the world.

In the past decade, amazing progress has been made on popular commercial standards (such as cellular, WLAN, and Bluetooth). This is a direct consequence of increasing levels of circuit integration: not only of building blocks such as LNAs, mixers, filters, and so on, but also multiple standards, all within a single-chip SoC. Many examples will be shown in the next section. In addition, new standards, such as UWB and WiGig have evolved from university research into commercial applications. Since high carrier frequencies and extremely wide bandwidth have been used in these developments to achieve high data rates, new circuit topologies have been required. As well, new trends in ultra-low-power wireless devices and health applications have seen increased popularities, new techniques for wake-up radio and battery-less operation have been proposed with promising results. All these advancements will be covered in this article.

Commercial Standards:

The advent of low-cost deep-submicron CMOS technologies has made possible the realizations of complex SoCs for multi-standard transceivers, which integrate both the MAC and PHY layers on the same die including the radio, thus reducing the number of external components, power dissipation, and ultimately the cost. While exploring some of these realizations, it is also interesting to see the evolution of the building blocks, and RX/TX architectures that have dominated the ISSCC RF and Wireless sessions over the past two decades, as they merged into the large SoCs of today.

For example, a quad-band GSM/GPRS SoC is presented [1]. On one chip, it integrates RF (ZIF RX and direct-modulation TX, with a $\Delta\Sigma$ fractional-N PLL), all the mixed-signal and digital functionalities, including an application processor, RAM/ROM and audio; leaving only PAs, filters, switches, and PMIC, as external components. A similar trend can be seen in the WLAN area: In 2005, one of the first complete SoCs for 802.11g (again including the entire baseband, MAC and PHY layers), was integrated in 0.18 μ m CMOS [2]. This radio exploits the sliding-IF dual-conversion architecture both for RX and TX. But, the complexity of such systems has grown further, while the multi-band capability is becoming important. In 2011, a 90nm CMOS transceiver was designed

to support 4 EDGE and 9 WCDMA bands [3]; also in 2011, a transceiver with an embedded quad-band GSM/GPRS/EDGE and 3 WCDMA bands, which included both digital and multimedia processing, in 65nm CMOS, was presented [4].

The emphasis on large systems-on-chip cannot overshadow new design solutions for basic RF building blocks. Thus, the drive to implement fully-integrated radios has fueled many new ideas: The translational loop concept made possible the implementation of a GSM front-end capable of filtering the blockers, without external SAW filter, one of the last elements which had "resisted" integration [5]. A new receiver design explores the elimination of the LNA, resulting in a mixer-first approach [6]; the receiver allows impedance matching at the antenna and achieves excellent linearity to manage large blockers [7]. More recently, translational loop has been implemented together with a noise canceling structure [8], and both single-ended and differential input saw-less receivers adopt transformer-coupled LNA [9]. Even in the widely-explored area of CMOS oscillators, novel topology with a Class-C VCO improves the noise-power trade-off [10]. In the long-standing area of PLLs, new techniques have been introduced to reduce in-band spurs in wide-band fractional-N synthesizer [11]. Many of these concepts have been applied to SoCs, producing for example, a quad-band GSM transceiver including a SAW-less receiver, integrated in 65nm CMOS [12].

A quad-band GSM/GPRS CMOS PA is an example of CMOS integration that was once considered impossible [13]: Using a Distributed Active Transformer (DAT), this PA achieved +35dBm of output power with PAE of 51%. Another development has been a fully-integrated CMOS differential PA for GSM/EDGE applications [14] which exploited the concept of the Doherty amplifier, an idea that originates from microwave circuits. The problem of efficiency enhancement of power backed-off in PAs, which seriously impact the battery lifetime, has been recently tackled using a dual-mode fully-integrated CMOS PA, for WCDMA applications [15].

The developments of integrated transmitters, has involved far more than the design of PA output stages: Modern communication standards employ non-constant envelope modulation techniques, such as OFDM, whose large peak-to-average-power ratios severely impacts PA efficiency. Various transmitter architectures, such as LINC and polar, have been attempted to address this issue [16]-[21].

An important concept developed in the past few years has been the realization of digitally-intensive RF transceivers. In such systems, the digital baseband data is directly converted to and from RF, without relying on classical mixer architectures. The digital receiver idea was popularized by the pioneering work on a Bluetooth receiver, in which the RF signal is first sampled-and-held and processed in discrete-time. This concept was later extended to GSM/EDGE transmitters based on a digital PLL [22] [23].

While the efficacy of the entire digitally-intensive approach, which is still in its infancy, is not assured, the introduction of the digital PLL has shown several advantages over its analog counterpart, such as design portability, simple noise cancellation, and power efficiency [24]-[28].

Digitally-intensive and SAW-less transceivers are important contributions to truly functional Software-Defined Radio (SDR), whose goal is not simply a multi-mode terminal, but a fully reconfigurable radio that can operate efficiently over all different standards [29]. An example of a digital circuit that solves classical RF problems, such as harmonic rejection, uses LMS-based adaptive cancellation in the digital domain to achieve 80dB of rejection [29]. The challenges of SDRs have also been investigated using external MEMS switches, suggesting future implementations that will exploit integrated RF MEMS [31].

New Standards and New Bands:

Thus far, we have described designs targeting the WLAN and 2G/3G cellular arena. However, in the past decade, we have witnessed the development of circuits for new standards, sometimes operating in frequency bands that were not possible for silicon just a decade ago.

In addition to basic telephony, 4G standard, WiMAX, and LTE, are devoted to mobile wide-band Internet access and multimedia features. WiMAX transceivers, appeared rather quickly, even adopting new architectures in a discrete-time receiver [32], while other SoC developments exploited the MIMO approach [33] [34]. However, the stringent requirements of LTE, including out-of-band noise, wide bandwidth channels, and FDD operations, severely challenge designers. A SAW-less modulator for LTE employed the voltage-sampling concept to achieve -162dBc/Hz noise in all bands [35].

Short-range wireless is another rapidly growing field: the typical requirement of high-efficiency has sustained the development of UWB transceivers [36]; and the first commercial realization of the TransferJet protocol allows for a 357Mb/s rate [37].

Beginning in 2000, research in the field of millimeter wave (mmW) silicon design has quickly made available ICs for new bands and new applications. The driving force to operate silicon in the 60GHz band was twofold: Technology scaling improved performance (in particular f_T and f_{max}), for both SiGe and CMOS technologies, which in turn makes silicon a viable alternative to III-V technologies. The need for wireless connectivity over very short distances (1 meter) at high-data-rate transfer (multi-Gigabit/s) has created new markets. The 60GHz band is much-less-crowded than the 1-to-5GHz band. Moreover, the high propagation losses at this frequency should ensure the isolation of the network with respect to interference. A SiGe fully-integrated transceiver at 60GHz was presented by IBM in 2004 [38], while the transceiver module, presented in 2011 [39], also embedded glass-substrate antennas. A WiGig-compliant 60GHz CMOS-transceiver chipset was introduced in 2013 [40].

Automotive radar (at 24GHz and 77GHz) is another important application developed in this decade that took advantage of the improvement of f_T and f_{max} performance: The spread-spectrum technique was presented in 2007 [41], while an example of frequency-modulated CW was presented in 2010 [42]. The high path loss at these frequencies represents a serious limit that cannot be overcome with only a simple highly-directional antenna in a portable system. For this reason, there has been a push toward silicon integration of phased arrays, capable of beamforming. (Interestingly, Gordon Moore predicted this application in his famous 1965 paper.) A fully-integrated 8-element 24GHz phased-array receiver SiGe was presented in 2004 [43], followed in 2005 by a CMOS 4-element transmitter [44]. In 2006, the same research group pushed the frequency to 77GHz using SiGe technology. Beamforming was also exploited in the 52GHz receiver implemented in standard CMOS in 2008 [45].

At ISSCC 2007, circuits operating above 100GHz were demonstrated, which enabled even higher data rates [46]: An oscillator and an amplifier at 104GHz were implemented in 90nm CMOS technology; such circuits have found application also in the growing field of imaging, as a 144GHz radar attests [47].

Today, silicon ICs are pushing toward 1THz, the borderline for RF circuits. A clear application of these (almost-THz) circuits is in the field of imaging. Although this field of research is very new, a 1k pixel THz camera [48], and the first CMOS broadband radiation source at 260 GHz [49] have been developed. However, market prospects for these applications remain unclear. Thus, it is difficult, and perhaps premature, to put such developments into a historical context.

New Trends:

In recent years, new trends in wireless communication have emerged to address ultra-low-power and health-care applications. Ultra-Low-Power (ULP) covers quite a large area of applications, mostly in sensor networks and electronic tag devices. To conserve energy as much as possible, these devices often include a wake-up radio which activates the device only when it is necessary. In the situation where energy storage is not available, energy needs to be extracted from the incident waves that also serves as a wake-up signal. In health-care applications, many low-power techniques have been explored over the past decade, and the WBAN (Wireless Body Area Network) 802.15.6 standard was finalized in 2012.

To achieve overall-low-power consumption, the wireless device must remain in idle mode most of the time, and be activated only occasionally by a wake-up RX. This RX can be awakened by detecting a signal in the air; however, false triggers are quite common if filters are not used for the wake-up signal frequency. At ISSCC 2012, a method was proposed that dramatically reduces false triggers by using a coded wake-up signal to trigger the wake-up RX [50], thereby allowing a more robust implementation of an ultra-low-power wireless device.

However, a low-power device has a finite lifetime because of its limited energy storage. As well, some applications requiring tiny wireless sensor nodes may not have space for a battery. Thus, energy harvesting becomes necessary. There are several sources of "free" energy: the most common, which has been used commercially, is Power-by-Field. In this mode, an initiator (or tag reader) sends a signal to the sensor node; if the received signal is sufficiently strong, energy can be extracted and stored in a holding capacitor; at the same time, the same signal can be used to wake up the device. Commercial examples of these are Electronic Toll Collection (ETC) and Near Field Communication (NFC). The most notable usage of this technology is in the eWallet. By 2016 when all new wireless handheld devices are expected to be equipped with this technology, eWallet will likely become the most popular payment method.

As well, lots of advancements have been made in the areas of healthcare. One of these is the creation of the WBAN standard that has just been finalized; (Note that a typical WBAN device consumes $<5\text{mW}$, and is capable of transferring at 10-to-100kb/s data rate; these devices typically operate around 400MHz, 900MHz, and 2.4GHz.) Earlier in the past decade, Super-Regenerative RX (SR-RX) was selected for low-power low-data rate for biomedical applications [51]. The high-Q passive component originally used in the SR-RX has been eliminated by using an auto-calibration technique on the quench waveform [52][53]. Because SR-RX can be used only with OOK modulation, other approaches are being investigated. For ULP, passive RX FE and passive mixers have been proposed to reduce the RX power consumption [54]; however, this approach suffers from higher NF due to lack of RF FE gain. An alternative for wireless communication in healthcare is to use the human body itself as the data-communication medium, in a process called Body-Channel Communication (BCC).

Recently, there have been three related developments in the area of Body Sensor Network (BSN), and Medical Implantable Communication Services (MICSs) [55]-[57]. Various architectural and circuit techniques have been created to meet healthcare standard requirements. Two notable ideas for power reduction are: an LNA-Mixer-VCO structure that shares a single bias current [58]; a multiphase injection-locked ring oscillator and sub-harmonic passive mixer to eliminate the need of high frequency LO [59]. Finally, the first device that meets WBAN standard was published in 2012 [60]. This transceiver uses sliding-IF RX and polar TX; to achieve the WBAN power consumption specification of $<5\text{mW}$.

Conclusion/Prediction:

As wireless handheld devices proliferate, and their sales volume surpasses that of traditional wired-networked devices (such as PC/notebooks), the entire ecosystem has now changed to provide applications and services wirelessly. In the coming few years, the data rate for wireless communication will increase by several times with the migration from the 3G to the 4G network; meanwhile, wireless-network coverage will become more seamless and robust, assisted by the availability of free hotspots in metropolitan areas. Moreover, more sensor devices will make use of Bluetooth or BLE (Bluetooth Low Energy) to provide more data and services. With the newer technologies, ultra-high-speed wireless links will provide instant download of movies and videos with very-low energy consumption, while NFC will completely change the way people conduct transactions.

With continuous research and development in wireless chips that support lower cost, lower power, and smaller form factors (higher integration), advancement in wireless handheld devices will continue. As a result, more applications and services will support these wireless devices to make them an essential part of everyone's life.



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TECHNOLOGY DIRECTIONS - AN EVOLUTION

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The Technology Directions Subcommittee within ISSCC covers emerging trends in solid-state circuits, ranging from innovative technologies and devices to new application areas. This technical category first appeared at the 1990 Conference with a single session under the heading “Emerging Circuit Technologies”. Papers in this session were chosen by the “General” Subcommittee, with the purpose of highlighting developments considered to be of importance to the solid-state circuits community, though not yet established as mainstream technologies. This first Emerging

Technologies session proved to be very popular, and so was continued in the following years, but this time with a specific “Emerging Technologies” Subcommittee comprised initially of three Program-Committee members (Frank Hewlett, Ron Jerdonek, Jan Van der Spiegel). In 1993, the 40th Anniversary of ISSCC, the Emerging Technologies Subcommittee was expanded to five members (Frank Hewlett, Ron Jerdonek, K.C. Smith, Jan Van der Spiegel) with John Trnka as the Chair. The Conference Chair, Dave Pricer, commissioned the Subcommittee with the task of growing the Conference in new topic areas, as submitted papers and attendance had been declining for several years. Pricer felt that the existing subcommittees tended to accept papers in established topics while frequently rejecting new subjects, so he specifically gave the Emerging Technologies Subcommittee the power to accept papers over the objections of the other subcommittees; of course, this led to some confrontational events in the Program Committee meetings!

In 1994, the Subcommittee was renamed Technology Directions (TD), and delivered three sessions to the Conference. This arrangement remained in place until ISSCC 2000, when the TD Subcommittee was expanded to include a member from each of the other subcommittees. This was done to improve acceptance from the other subcommittees, and over time, relations between TD and the other subcommittees improved significantly. Later, in 2005, the TD Subcommittee was re-organized to once again have its own set of members, and arrangements have remained stable since then.

Predicting the Future:

The task of the TD Subcommittee is to identify emerging technologies of possible importance to the evolution of ISSCC, perhaps as much as five to ten years from their commercialization. Thus, it is inevitable that TD sessions have championed both successes (technologies and innovations which go onto become mainstream), as well as failures (those which are superseded by other, better techniques).

In the early years of TD, the failure rate was perhaps higher than the success rate. Technology areas which were championed in the early years of TD – but which failed to gain a place in the mainstream conference – include analog and digital neural network implementations [1] to [4]; logic circuits using exotic devices such as resonant tunnelling devices, Josephson junctions, electron-gas CCDs, and superconductive technology [5] to [8]; and memory technologies such as para-electric films, multi-valued associative RAM using floating gates, and cell-capacitor memory arrays [9] to [11].

With the formation of a dedicated Subcommittee, the success rate improved. Areas first highlighted during TD sessions, and which are now widespread among the Solid-State Circuits community include:

MEMS:

A TD session at ISSCC 1993 entitled “Scaling, Sensing, Micro-Optics” presented a number of papers describing the challenges and prospects provided by the merger of micromechanical and microelectronic elements, including a paper from the Fraunhofer Institute describing the design of a CMOS piezoresistive pressure sensor with integrated programming and calibration circuitry [12]. Two years later, another TD session included a paper from Texas Instruments reporting on a micro (electromechanical) system that integrated

digital micro-mirror devices with CMOS circuits [13] – such Digital Light Projector (DLP) technology is now widespread in projection display systems. MEMS circuits and applications within ISSCC have matured and are now handled by the Imagers, MEMS, Medical, and Displays (IMMD) Subcommittee.

Low-Power Digital:

The first TD session to focus on advances in low-power technology, particularly for digital circuits, was in 1994. Contributions included a paper by Chandrakasan (UC Berkeley) describing a fully-configured wireless terminal operating from only a 1.1V supply [14], while Stanford described functional digital circuits using zero-threshold CMOS transistors operating at supply voltages as low as 200mV [15]. Further low-power/low-voltage digital papers emerged in TD sessions in the following years, including the use of a variable substrate bias to enable standby-power reduction [16], and techniques to control power consumption of individual sub-blocks without requiring multiple-thresholds or triple-well [17]. Such low-power/low-voltage digital techniques now reside within the Energy-Efficient Digital (EED) Subcommittee.

RF Techniques:

Advanced RF techniques have often arrived at ISSCC via TD before they become established technologies within the RF/Wireless Subcommittees. Examples include: Abidi (UCLA) projected that the direct conversion transceiver would be a major competing architecture for integrated wireless communications [18]; IBM researchers showed that the integration of spiral inductors on VLSI silicon was feasible with Qs of up to 40 [19]; and in 1998, Samavati (Stanford) proposed the use of both vertical and lateral electric fields to increase capacitance per unit area [20].

Increasing RF Frequencies:

Continued CMOS scaling has driven integrated RF circuits to higher and higher frequencies. At ISSCC 2000, a TD session entitled “High Frequency Wireless” presented a paper from Bell Labs describing a 5GHz CMOS radio-front-end chipset [21]. In 2004, at a similar TD session, researchers from UC Berkeley presented RF CMOS circuits operating at 60 GHz [22], while

more recently, CMOS circuits approaching Terahertz operation have appeared [23].

Technology Developments:

TD is the traditional forum in which technology and process developments are introduced to ISSCC. Recent years have seen the emergence of FinFETs [24], FBAR technology [25], Magnetoresistive RAM [26], and above-IC Bulk Acoustic Wave (BAW) integration [27].

RFID:

Circuit techniques for RFID applications were first presented at ISSCC in 1997 [28][29]. More recent developments presented at TD show reduced circuit area and cost, extending the potential application fields to barcode replacement [30] and individual recognition [31].

Packaging and 3D Integration

TD has also championed advances in packaging and integration density. In 1990, the state-of-the-art in high-density packaging was presented by Fujitsu as a pin-grid array with a 636µm pin pitch [32]. In 1996 researchers from Matsushita presented a flip-chip technology allowing single-chip antenna integration for mm-wave circuits [33]; in 2004, IMEC presented options for 3D interconnection and packaging [34]; while in 2005, Keio University described 3D-stacked die using inductive wireless coupling for data interconnect [35]. These advances in packaging and integration density continue with IMEC presenting issues and considerations for Through-Silicon Via (TSV) technology at ISSCC 2010 [36].

Energy Harvesting:

Circuits supporting energy-harvesting for battery-less applications first featured within TD sessions, before transitioning to the IMMD Subcommittee. One of the first papers in 2003 from MIT describes two MEMS-based power sources generating electrical power from heat and rotation, respectively [37].



Papers appearing regularly in future years have shown increasing miniaturization and conversion efficiency, such as a thermoelectric-energy-harvesting interface circuit presented by MIT which enables operation from input voltages as low as 35mV [38].

Launching the Future:

Today, the TD Subcommittee continues to champion technologies and application areas which are likely to have a significant impact over the coming decade. Reviewing recent TD sessions at ISSCC, one sees key technology innovations that are likely to form the basis of products in years ahead, including:

Future Medical Applications:

Although the IMMD Subcommittee is responsible for the biomedical-applications area within ISSCC, more innovative or experimental circuits are often presented first in TD. Such applications include: retinal implants for restoring vision [39]; the control of insect flight via electrical muscle stimulation [40]; and implants for optical modulation of neurons in the brain – a technique known as optogenetics [41]. Another emerging area within the biomedical field is Wireless Body-Area Networks (WBAN), and recent ISSCC papers include body-sensor nodes which can be embedded within adhesive bandages [42], or miniature patch sensors for continuous sleep monitoring [43].

Flexible and Printable Circuits:

The performance and complexity of organic electronics continues to increase, opening up new possibilities for future flexible and printable products. Recent TD papers in this field include: a flexible, large area pressure sensor for artificial skin [44]; organic RFID tags [45]; and even an organic 8-bit microprocessor implemented on a flexible, plastic foil [46].

Imaging:

Increasing CMOS operating frequencies and lower intrinsic device noise enables new imaging techniques to become feasible using bulk silicon technologies. Recent examples include terahertz imaging for security and medical applications [47], and miniaturized solutions for Nuclear-Magnetic-Resonance (NMR) imaging [48].

Next-Generation Sensors:

Further miniaturization of sensors, particularly for biomedical applications, remains an active area for TD. Examples from recent years include: interfacing of semiconductors and living neuronal cells [49]; microfluidic systems fabricated directly on top of a sensing and control IC [50]; Nano-ElectroMechanical Sensors (NEMS) integrated with CMOS circuits [51]; and sensors for miniaturization of DNA analysis [52].

ISSCC 2013:

Papers accepted for this year's TD sessions at ISSCC build on the themes identified above. Medical applications presented this year include an iontophoresis controller IC for transdermal drug delivery integrated into a patch-type form factor [53], and an ultra-low-power SoC which detects EEG signals, and classifies them using a non-linear support vector machine for early detection of seizures in conditions such as epilepsy [54]. Applications for large area electronics also continue to develop, and this year, we see presented an organic sensor sheet for EMG measurement [55], as well as a transponder array on a flexible sheet for powering and communicating with battery-less sensors [56]. In the field of imaging, a Single-Photon Avalanche Diode (SPAD) line sensor for time-resolved laser Raman spectroscopy is presented, designed for space and rover-based planetary exploration [57]. Contributions to next-generation sensor applications include an integrated microsystem for neural sensing applications, where the neural probes and CMOS circuitry are directly connected using Through-Silicon Vias (TSVs) [58], and a fully-digital capacitive sensor interface implemented entirely using carbon nanotube FETs [59]. Moreover, in what may prove to be a new TD direction, two papers describe non-volatile digital-processing systems whereby memory elements are embedded within logic gates, enabling systems with zero standby power consumption [60], as well as robust operation even when the digital supply voltage is frequently interrupted [61].

In Summary:

Clearly, such a brief review as this can only touch on the number and diversity of papers which have appeared at ISSCC under the "Technology Directions" umbrella, and the limited space available, means that inevitably some important papers and topics could not be included. However, what is important to note is that, as technologies arrive in TD, and mature, becoming part of the mainstream Conference, they continue to be replaced by new and exciting developments, ensuring that ISSCC remains the premier forum in which state-of-the-art results in solid-state technologies are reported.

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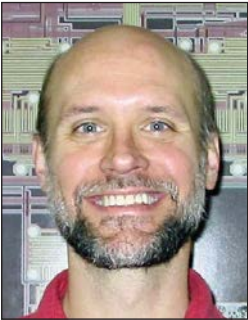
ISSCC 2003 Attendees awaiting the start of the Plenary Session.

ISSCC 2002 Book Displays.



TEN YEARS OF WIRELINE CIRCUITS AT ISSCC

John T. Stonick, Synopsys, Hillsboro, OR



Introduction:

During the past 10 years, advances have been made in many aspects of optical and electrical interconnects, Wireline, for short. CMOS implementations supporting serial data rates up to 40Gb/s have been reported, along with advanced equalizers operating beyond 65Gb/s. As well, novel solutions have been presented to overcome the challenges associated with pushing data rates to ever-increasing speeds, over lossy electrical channels with strongly frequency-dependent characteristics. The trend to technologies which effectively lower

the cost of incorporating digital signal processing within wireline receivers has also enabled an expanded role for digital equalization solutions. Finally, wireline design effort has been shaped dramatically by the rising importance of system-driven power constraints, resulting in extraordinary advances in link power efficiency.

Electrical Interconnects:

The advances in electrical interconnects can be categorized by four parameters: speed, efficiency, equalization performance, and system innovation. In what follows, we will walk through each of these in an effort to present a comprehensive framework in which to understand the developments of the past ten years, and to provide some insight into the future of wireline circuits.

Speed: The trend in raw speed over the past ten years can be seen in Figure 1. This trend is important because it shows the achievable state-of-the-art which can be extrapolated to provide a glimpse of the future.

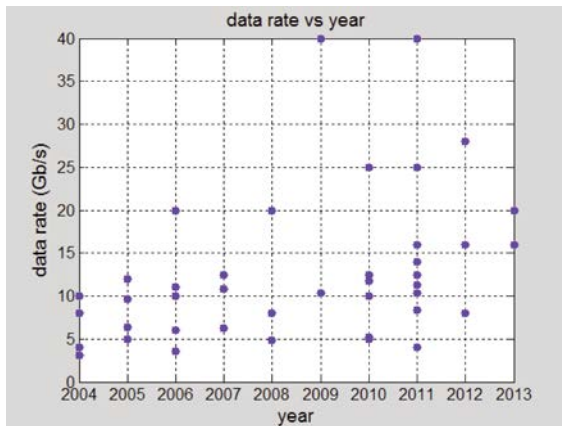


Figure 1: Data Rate vs Year [1]

In Figure 1, we can see that there has been a gradual upward trend in the top data rate of electrical transceivers, the top data rate increasing by a factor of four over the ten-year period. The highest reported speed for an electrical transceiver, 40Gb/s, occurred in 2009 [2] and again in 2011 [3]. This is a remarkable accomplishment for CMOS technology. While the chart in Figure 1 is for full transceivers, it is notable that this year, Lu and Alon describe a 66Gb/s 3-tap DFE receiver in a 65nm GP CMOS process[4]. As optical standards and 100GbE standards progress, they will continue to apply pressure to develop faster electrical transceivers to the pipes full.

Efficiency: An area in which significant progress has been made over the past ten years, is that of efficiency. Efficiency is usually reported in mW per Gb/s; However, when reviewing a large collection of data on a single plot, inverting this metric to Gb/s per mW, serves to highlight the best work.

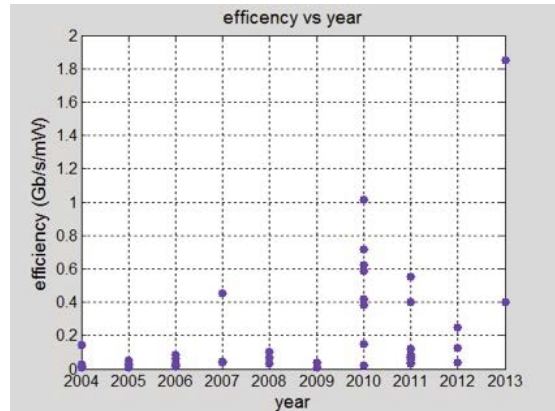


Figure 2: Efficiency vs Year [1]

As we see in Figure 2, with one exception in 2007, efficiency was not a major part of the design effort from 2004 to 2009. However, that single exception represented a breakthrough paper, "A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communications" [5], by Palmer et al that combined both known and novel circuit-design techniques to minimize energy consumption in a chip-to-chip transceiver. It took three years to eclipse the efficiency demonstrated in that paper. Then, in 2010, efficiency became a hot topic, with many highly-efficient transceivers being presented, including the best-in-class paper by Fukuda et al, "A 12.3mW 12.5Gb/s Complete Transceiver in 65nm CMOS" [6], in which they demonstrated a peak efficiency of more than 1Gb/s per mW (or equivalently less than 1mW per Gb/s). This year, at ISSCC 2013, the peak efficiency was again pushed forward in a die-to-die link from Poulton et al, "A 0.54pJ/b 20Gb/s Ground-Referenced Single-Ended Short-Haul Serial Link in 28nm CMOS for Advanced Packaging Applications" [7]. This performance, while impressive, is difficult to directly compare to previous works which were chip-to-chip transceivers.

An additional aspect, from which we can glean some understanding, is how the efficiency trend over the past ten years is related to process feature size as shown in Figure 3.

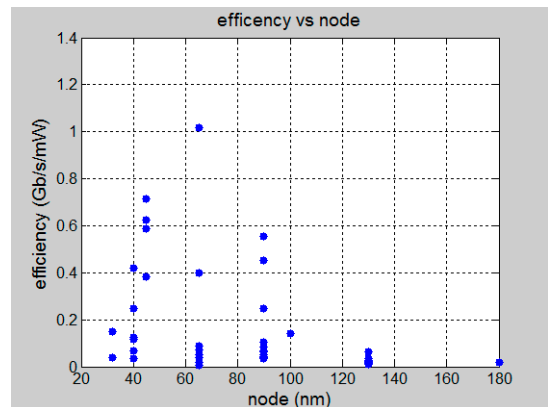


Figure 3: Efficiency vs Feature Size [1]

Here, we see an interesting trend: It would appear that the "sweet spot" for efficiency occurs for feature sizes in the range from 45nm to 90nm. One explanation is that the reduced headroom in finer geometries leads to inefficiency in high speed I/O design, nulling out the advantage of higher f_T transistors. For larger geometries, the larger parasitics, lower f_T , and higher supply voltages, limit efficiency at today's data rates. Note that the extremely-high efficiency exhibited at 28nm was for a package-to-package link from Nvidia.

Performance: While both data rate and efficiency are important, they only partially characterize the advances made in electrical transceivers over the past ten years. A remaining important aspect is the area of capability, the combination of speed of operation, along with the ability to compensate for loss. In 2012, Bulzacchelli et al presented “A 28Gb/s 4-Tap FFE/15-Tap DFE Serial Transceiver in 32nm SOI CMOS Technology” [8], that was shown to compensate for 35dB of loss, and is arguably the most-capable transceiver published to date.

System Innovation: Perhaps the most innovative paper presented over the past 10 years was “A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital RX Equalization and Clock Recovery” [9], presented by Harwood et al, in 2007. In their work, they replaced the analog equalizer and binary slicer found in a traditional binary receiver with an ADC, moving the equalization purely into the digital domain. The novelty of this work is evidenced by the fact that it sparked an evening session in 2009, “Will ADCs Overtake Binary Frontends in Backplane Signaling?” While there was no consensus in 2009, it is now clear that ADC-based receivers do offer promise as a candidate architecture for the transceivers of tomorrow.

A second major innovation that had immediate impact was the voltage-mode or SST transmitter presented in 2007, “A 16Gb/s Source-Series Terminated Transmitter in 65nm CMOS SOI” by Menolfi et al [10]. This presentation launched the present trend toward using voltage-mode drivers, as opposed to the traditional CML drivers, in high-speed electrical transceivers.

Optical Interconnects Introduction: At the same time that progress was being made in electrical-transceiver design, the state-of-the-art of optical transceivers was also advancing. To better understand the trends and advancements in optical transceivers, we will consider developments in three application areas: Silicon photonics (such as intra-board level optics), access-network transceivers to support PON-type applications, and transceivers for long-haul optical networks.

Silicon Photonics and Optical-Electrical Interface Circuits: Integrating electronics and photonics is one of the keys that will someday enable optical backplanes as an economically viable alternative to electrical backplanes. In this regard, a huge step forward was made in 2006 when Huang et al published, “A 10Gb/s Photonic Modulator and WDM MUX/DEMUX Integrated with Electronics in 0.13 μ m SOI CMOS” [10]. This startling achievement was followed in 2007 when Narasimha et al, published, “A Fully Integrated 4x10Gb/s DWDM Optoelectronic Transceiver in a Standard 0.13 μ m CMOS SOI” [11]. Today’s state-of-the-art in this area was presented by Proesel, et al in 2012, “25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-Based Optical Links in 90nm CMOS” [13]. As well, a glimpse into the future of silicon photonics was given by the presenters of a 2012 Evening Session, “Optical PCB Interconnects, Niche or Mainstream?”. The general consensus of the session was that system-level high-volume manufacturing challenges still must be overcome before silicon photonics can be widely adopted.

Passive Optical Networks (PONs): While silicon photonics are still a futuristic application for optical transceivers, the rollout of Passive Optical Networks (PONs) over the past ten years, such as Verizon’s FIOS network, have been enabled by the burst-mode-transceiver work presented at ISSCC: Enabling technologies for PONs began with a “Burst-Mode Receiver for 1.25Gb/s Ethernet PON with AGC and Internally Created Reset Signal”, published by Le, et al in 2004 [14]. The state-of-the-art was advanced in 2007 by a pair of papers: Lee and Liu’s paper, “A 20Gb/s Burst-Mode CDR Circuit Using Injection-Locking Technique” [15], presented a CDR that could lock within a single bit time. Cho, et al, pushed the speed-of-operation limits for burst-mode operation with “A 33.6-to-33.8Gb/s Burst-Mode CDR in 90nm CMOS” [16].

Long-Haul Networks: While optical for backplanes is a future market, and optical for access networks is an emerging market, optical has been dominant in long-haul networks for quite a while. This has been due in large part to the optical-transceiver work that has been and continues to be presented at ISSCC. The trend over the past ten years in this area has been the replacement of SiGe transceivers by CMOS transceivers: In 2004, Werker et al, set the bar

for power and performance in “A 10Gb/s SONET-Compliant CMOS Transceiver with Low Cross-Talk and Intrinsic Jitter” [17], by publishing an OC-192-compliant transceiver that consumed less than 1W. The trend from SiGe to CMOS continued in 2009, when Amamiya, et al, showed that it was possible to achieve OC-768 performance in CMOS when they published, “A 40Gb/s Multi-Data-Rate CMOS Transceiver Chipset with SFI-5 Interface for Optical Transmission Systems” [2].

The Future:

Where do we go from here? The past ten years have borne witness to a combination of innovation and evolution in the fields of electrical and optical transceivers. Over the next ten years, I expect that the demand for higher bandwidths over copper channels will push backplane electrical transceivers to multi-level signaling, just as has already occurred in twisted pair Ethernet and disk-drive read channels. This will blur the distinction between traditional and ADC-based receivers. Additionally, I expect that within ten years, silicon photonics will no longer be a technology of the future, but rather will have a significant market share in high-end server applications, and will have begun working its way down into consumer applications.

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THROUGH THE LOOKING GLASS II – TREND TRACKING FOR ISSCC 2013

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At the IEEE International Solid-State Circuits Conference (ISSCC), there is a long tradition of striving to extend the Conference's role as the foremost global forum for the presentation of advances in solid-state circuits and systems-on-a-chip (SoCs). But, this implies a great deal of effort on the part of many people. One of the most important elements of this effort is the structuring and organization of the Program Committee, including its subdivision into ten subcommittees, each focusing on diverse technical areas, and their dynamic growth and adaptation through the selection of world-renowned specialists. One of the many techniques used by each Subcommittee to remain at the forefront of evolving technology is the identification and maintenance of trend information, on the basis of which new developments become startlingly clear.

The intent of the present article is to share with members of the IEEE Solid-State Circuits Society (SSCS), a sampling of the views held by the diverse group of experts represented within the Program Committee, which for ISSCC 2013 is composed of 161 members, including 10 Subcommittee Chairs. These members are divided into ten Subcommittees whose size ranges from 12 to 18 people. This year, the Subcommittees are focusing on the following areas: analog; data converters; energy-efficient digital; high-performance digital; imagers, MicroElectroMechanical Systems (MEMS), medical, and displays; memory; radio frequency; technology directions; wireless; and wireline. What follows is a sampling of recent analyses and predictions from each of the ten subcommittees:

Analog

Analog techniques continue to have a critical role in evolving modern electronics: The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy must fundamentally be performed with analog systems. As a result, the key technologies for power management are predominantly analog. For example, currently there is much interest in wireless power transmission for battery charging applications, such as for mobile handsets and for medical implants. Increased efficiency in wireless power transmission is enabling faster charging over longer distances. As well, there is an explosion of technologies that permit energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers. Here, the significant focus is on analog circuits which harvest sub-microwatt power levels from energy sources at tens of millivolts, providing autonomy for remote sensors or supplementing conventional battery supplies in mobile devices. To achieve this, extremely low power must be consumed by the attendant analog circuits so that some energy remains to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation

amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of such low power systems. Fast power-up and power-down are also required of these circuits to permit high energy efficiency during intermittent operation. In combination, these analog power-management technologies will permit devices to be powered indefinitely from sustainable sources, opening the door to many evolving applications, including ubiquitous sensing, environmental monitoring, and medical instrumentation.

Analog circuits also serve as bridges between two worlds – the digital computational, and the analog real. Just like road bridges, analog-circuit bridges are often bottlenecks, and their design is critical to overall performance, efficiency, and robustness of the system they support. Nevertheless, digital circuits such as microprocessors drive the semiconductor market; thus, semiconductor technology has been optimized relentlessly for the past 40 years to reduce the size, cost, and power consumption of digital circuits. Correspondingly, analog circuitry has proven increasingly difficult to implement using these optimized-for-digital IC technologies. For example, as the size of transistors reduced, the range of analog voltages they can handle decreased, and the variation observed in their analog performance increased. These aspects of semiconductor technology explain two key divergent trends in analog circuits. One is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency-lighting applications. But, other applications dictate full integration of both analog and digital circuits in the smallest-feature-sized modern digital technologies. One important example is microprocessors where multiple cores are able to reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are represented in Figure 1 by movement towards the top-right.

Thus, we see analog techniques continuing to thrive while expanding in support of new demands for power efficiency driven by digital developments.

Data Converters

Data converters serve as key building blocks in almost all known applications that bridge the analog physical world with the digital circuits that dominate modern integrated circuits. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be key drivers for innovation, as evidenced by the data converters presented at ISSCC 2013.



ISSCC 2013: Paper Session Assignment at the October Paper-Selection Meeting.

Figure 2 shows energy efficiency expressed as power dissipated relative to the effective Nyquist sample rate (P/f_{snrq}) as a function of the ADCs Signal-to-Noise Ratio (SNDR). For low- to medium-resolution converters, energy is primarily expended to quantize the signal; the efficiency of this operation can be measured as the energy consumed per conversion step (the so-called Walden Figure of Merit). The dotted trend line in Figure 2 represents the benchmark of 10fJ/conv-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of the signal-to-noise ratio, as shown by the solid line. For ISSCC 2013, contributions are indicated by the colored dots representing various converter architectures, with previous years denoted by the smaller dots. (Note that a lower P/f_{snrq} metric represents a more efficient circuit.) Several new SAR-based converters at various SNDR design points continue to extend the limits of energy efficiency, and push into previously uncharted territory.

Figure 3 shows energy per conversion step versus the effective sample rate. This figure elucidates the difficulties of high-speed operation for a given technology. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the spectrum of conversion rates.

Finally, Figure 4 shows achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nevertheless, at ISSCC 2013, we see many examples that set new records in this metric, utilizing several different converter architectures.

Converters continue to evolve in support of the increasing demands of new applications motivated by the availability of faster decreasing-cost digital circuits.

Energy-Efficient Digital

The energy efficiency of digital circuits becomes increasingly important as larger and larger numbers of transistors are integrated on a single chip: Demand for ubiquitous mobile functionality for enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive technological innovation toward energy- and cost-efficient implementations. While the performance of embedded processors has increased to meet the rising demands of general-purpose computation, dedicated multimedia accelerators provide dramatic improvements in performance and energy efficiency for specific applications.

Energy harvesting is another area of growing importance, leading to technologies that leverage non-volatile logic-based SoCs for applications that do not have a constant power source, or for handheld devices with very-limited battery capacity.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as reducing the area required to implement specific functions. Correspondingly, at ISSCC 2013, processors unveiled are built on a variety of technologies, with best-in-class results as measured by integration scale, performance/watt, and integration functionality. These include a few industry-first implementations demonstrated in various technologies ranging from 0.13 μm down to 28nm bulk and SOI CMOS technologies.

Emerging medical applications require a significant reduction in standby power, compared to state-of-the-art commercial processors. This has driven the exploration of new leakage-reduction techniques in both logic and on-chip memories, targeting orders-of-magnitude reduction in leakage currents. Fast wake-up time requirements drive the need for rapidly saving and restoring the processor state.

Figure 5 illustrates the main trends of energy relevant aspects of feature phones and smart phones. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300MHz in the early 2000s, there was a sudden spurt towards 1GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and recent smart phones incorporate dual- and even quad-core processors, running up to 2GHz. Battery capacity, mostly driven by

the required form factor, as well as thermal limits, imply a power budget of roughly 3W for a smartphone. From this power budget, the RF power amplifier (for cellular communication) and the display are major drains. Overall, digital power consumption ranges from 2W (peak) to 1W (sustained). Thus, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth). For video and image processing, the trend has been toward dedicated optimized hardware solutions. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, and computational imaging. For all digital circuits, the limited power budget leads to the use of more-fine-grained clock gating, various forms of adaptive voltage-frequency scaling, a variety of body-bias schemes, and elaborate power-management strategies.

Figure 6 shows the evolution of bit rates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links, consistently show a 10 \times increase in bit rate every five years, with no sign of abatement. Thus, with essentially-constant power and thermal budgets, energy efficiency has become a central theme in designing the digital circuits involved in signal processing. Historically, CMOS feature sizes have halved every five years. For a brief period in the 1990s, CMOS scaling (a.k.a. Dennard scaling) provided a 2³ (α^3) increase in energy efficiency every five years, almost matching the required 10 \times power reduction. But, during the past decade, CMOS scaling offers only a roughly 3 \times improvement in energy efficiency every five years. The resulting ever-widening gap has led to alternative approaches to improving energy efficiency, namely, new standards, smarter algorithms, more-efficient digital signal processors, highly-optimized accelerators, smarter hardware-software partitioning, as well as the power-management techniques mentioned previously.

Thus, we see a potential for a host of new applications of lower-and-lower-power technology created in response to the recognition of the universal importance of efficient local processing of signals in diverse omnipresent areas.

High-Performance Digital

The relentless march of process technology brings more integration and performance to digital systems each year: At ISSCC 2013, for example, IBM's System z processor leads the charge with a 2.75B transistor chip, operating at 5.7GHz.

The chip complexity chart in Figure 7 shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration mark was achieved some years ago, we now commonly see processors with beyond 2B transistors on a single die.

Leveraging sophisticated strategies to lower leakage and manage voltage, variability, and aging, has bolstered the continuing reduction in total power dissipation. These strategies are helping rein in the increase in energy demands from PCs, servers, and similar systems. As power reduction becomes mandatory in every application, the trend towards maintaining near-constant clock frequencies also continues as shown in the frequency trends plot in Figure 8. This will yield solutions with lower cost and lower cooling demands, resulting in greener products for the future.

As well, processor designers are choosing to trade off performance by lowering supply voltage. The performance loss of reduced voltage and clock frequency is compensated by further increased parallelism. Processors with more than 8 cores are now commonplace. This year, at ISSCC 2013, a 24-core processor will be presented as noted in the core-count trend chart in Figure 9.

In addition to the trend toward integrating more cores on a single chip, single packages with multiple die are appearing: At ISSCC 2013, IBM will present a multi-chip module with six CPUs and two embedded DRAM cache chips. As well, dedicated co-processing units for graphics and communications are now commonly integrated on these complex Systems-in-Package (SiP). Design of these SoCs and SiPs requires broad collaboration across multiple disciplines including circuits, architecture, graphics, process technology, package, system design, energy efficiency, and software. New performance- and power-efficient computing techniques continue to be introduced for targeted critical applications, such as floating point and SIMD.



As technology continues to scale to finer dimensions, large caches are being integrated within microprocessor die. Figure 10 shows the general trend of large cache integration.

Methods for communication within and between die are becoming increasingly important. These are being driven by two trends: (1) 3D integration is increasingly common; and (2) interconnect delay becomes more dominant as processes scaled down. Designs emphasizing on-die inter-chip transport constitute a recent trend (see also Wireline).

At ISSCC 2013, another trend in evidence is the continued emergence of all-digital phase-locked loops and delay-locked loops which better exploit nanometer-feature-size scaling while reducing power and area costs. Due to the application of highly innovative architectural and circuit design techniques, the features of these “all-digital” PLLs and DLLs have improved significantly over the recent past. Figure 11 shows the jitter performance vs energy cost for PLLs and MDLLs.

Overall, digital processors continue to grow in complexity, while more circuits are implemented using digital techniques to cope with variability, and ease scaling to finer geometries.

Imagers, MEMS, Medical, and Displays (IMMD)

The common thread that unites the constituents of IMMD is a concern for interfaces with the physical world – both the human body and its environment. Conventionally, we consider this broad area in terms of both tool and task: imagers, MEMS, medical, and displays, as discussed in the following subsections:

Imagers:

Since 2010 there has been growth beyond expectations in the adoption of mobile devices, such as smart phones and tablets, which has induced larger volumes of CMOS image sensor chips. Both the resolution and miniaturization races are ongoing, and performance metrics are becoming more stringent. In addition to conventional pixel shrinkage, a “more than Moore” trend is increasingly evident: Resolution of over 20Mpixels is commercially available for mobile devices employing enhanced small-size pixels. As a consequence of innovative readout and ADC architectures embedded at the column and chip levels, data rates approaching 50Gb/s, and a noise floor below single electron, have been demonstrated. In addition to conventional applications, ultra-low-power vision sensors, 3D, high-speed, and multispectral imaging, are front-running emerging technologies.

Back-Side Illumination (BSI) is now the mainstream technology for high-volume high-performance mobile applications. While 1.12 μ m BSI pixels are currently available, the industry is potentially moving towards 0.9 μ m pixel pitch and below. Additional innovative technologies outside of traditional scaling include advanced 3D stacking of a specialized image-sensor layer on top of deep-submicron digital CMOS (65nm 1P7M) using Through-Silicon Vias (TSVs) and micro-bumps.

The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts is a trend throughout the image-sensor industry toward higher levels of integration to reduce system costs.

Ultra-low-power vision sensors are being reported in which more programmability and computation is performed at the pixel level in order to extract scene information, such as object features and motion.

Lightfield/plenoptic commercial cameras, which have been available since 2010, are now gaining popularity and are being marketed for 3D imaging and/or all-in-focus 2D imaging. On-chip stereoscopic vision has been demonstrated through Digital Micro Lenses (DMLs), paving the way to next-generation passive 3D imaging for mobile and entertainment applications, such as through gesture-control user interfaces.

Significant R&D effort is being spent on active-3D-imaging Time-Of-Flight (TOF) applications to support requirements from autonomous driving, gaming, and industrial applications, addressing open challenges, such as background light immunity, higher spatial resolution, and longer distance range.

Deep-submicron CMOS Single-Photon Avalanche Diodes (SPADs) have been developed by several groups in various submicron technologies. They are now capable of meeting the requirements for high resolution and high timing accuracy by employing highly parallel Time-to-Digital Converters (TDCs) and small pixel pitch with better fill factor.

Ultra-high-speed image sensors for scientific imaging applications having up to 20Mfps acquisition speed have been demonstrated.

Multispectral imaging is gaining a lot of interest from the image-sensor community: several research groups have demonstrated fully-CMOS room-temperature THz image sensors, and a hybrid sensor capable of simultaneous visible, IR, and THz detection has been reported.

The share of the market for CCDs in machine vision, compact DSCs for security applications continues to shrink. Only for high-end digital cameras for astronomy and medical imaging, do CCDs still maintain a significant market share.

MEMS and Sensors:

MEMS inertial sensors are finding widespread use in consumer applications to provide enhanced user interfaces, localization, and image stabilization. Accelerometers and gyroscopes are being combined with 3D magnetic-field sensors to form nine-degree-of-freedom devices, and pressure sensors will eventually add a 10th degree. The power consumption of such devices is becoming sufficiently low for the sensor to operate continuously, enhancing indoor navigation. There have been further advances in heterogeneous integration of MEMS with interface circuits to support increased performance, larger sensor arrays, reduced noise sensitivity, reduced size, and lower costs.

To address the stringent requirements of automotive, industrial, mobile, and scientific applications, MEMS inertial sensors, pressure sensors, and microphones are becoming more robust against Electro Magnetic Interference (EMI), packaging parasitics, Process-Voltage-Temperature (PVT) variations, humidity, and vibration.

Sensor interfaces achieve increasingly high resolution and dynamic range while maintaining or improving power or energy efficiency. This is achieved through techniques such as zooming, non-uniform quantization, and compensation for baseline values.

New calibration approaches, such as voltage calibration, are being adopted for BJT-based temperature sensors to reduce cost. In addition to thermal-management applications (prevention of overheating in microprocessors and SoCs), temperature sensors are also increasingly co-integrated with other sensors (such as humidity, pressure, and current sensors), and MEMS resonators for cross-sensitivity compensation. Alternative temperature-sensing concepts find their way into applications with specific requirements not easily addressed by BJTs: Thermal diffusivity-based sensing for high-temperature applications; thermistor-based and Q-based concepts for *in-situ* temperature sensing of MEMS devices and for ultra-low-voltage operation.

MEMS oscillators continue to improve: Phase noise is now low enough for demanding RF applications (12kHz-to-20MHz integrated jitter is now below 0.5ps); and frequency accuracy is now better than 0.5ppm. Consumer applications are adopting such new low-power and low-cost oscillators.

Biomedical:

There have been continuous achievements in the area of ICs for neural and bio-potential interfacing technologies. Spatial resolution of neural monitoring devices is being reduced utilizing the benefits of CMOS technology. IC providers are increasing their component offerings towards miniaturization of portable medical devices.

Telemedicine and remote-monitoring applications are expanding with support from IC manufacturing companies. Moreover, the applications of such systems are not limited to services targeted for elderly or chronically ill patients; for example, there are several technologies developed to enhance the way clinical trials are conducted by monitoring patient adherence and by improving data collection. Low-power WiFi, and Bluetooth-low-energy is emerging as a standard wireless connection between portable communication services and wearable technology.

Smart bio-molecular sensing is another major trend that marries the solid-state and biochemical worlds together with the ultimate goal of enabling a more predictive and preventative medical care. With the help of the accuracy

and parallelism enabled by CMOS technology, time, cost, and error rate of DNA sequencing may be significantly improved. Direct electronic readout may relax the need for complex biochemical assays. Similar trends are becoming increasingly evident in proteomics and sample preparation.

Even for medical imaging, there is a shift from hospital imaging toward point-of-care and portable devices. A key example is in portable high-resolution ultrasounds in which larger scientific imaging setups are being integrated onto the sensor through process technologies (such as integrated spectral filters, CMUT). Another example is in molecular imaging. The advent of Silicon Photo Multipliers (SiPM) which provide a solid-state alternative to PMTs, enable the realization of PET scanners compatible with MRI, opening the way to new frontiers in the field of cancer diagnostics. More recently, SiPMs realized within deep-submicron CMOS technologies have allowed the integration at pixel- and chip-level extra features, such as multiple timestamp extraction, allowing a dramatic reduction of the system cost.

Displays:

The desire to put much higher-resolution and higher-definition displays into mobile applications is one of the display-technology trends, that is now opening a Full HD smartphone era. 440ppi high-definition displays are expected, even for 5-inch display sizes. Low-Temperature Poly Silicon (LTPS) technology seems to have more merit than amorphous-Silicon Thin-Film-Transistors (a-Si TFTs) technology. But a-Si TFT and oxide TFT technologies supported by compensating driver systems are beginning to compete with it. Very-large-size LCD TVs over 84 inches, with UD (3840×2160) resolution are now the leading entertainment systems. 55-inch AMOLED TVs with Full HD resolution are also opening new opportunities in consumer applications.

As touch-screen displays for mobile devices become increasingly thin, capacitive touch sensors move closer to the display. But, the resulting in-cell touch displays come with reduced signal levels due to increased parasitics, and increased interference from the display and switched-mode chargers. Noise immunity is improved by adopting noise filtering and new signal-modulation approaches.

Thus, overall, we see expansion of diverse techniques evolving in aid of the most important role of modern technology – to serve mankind.

Memory

Development in mainstream memory technologies continues unabated: We see progressive sustained scaling in embedded SRAM, DRAM, and floating-gate-based Flash, for very broad applications. However, due to the major scaling challenges in all mainstream memory technologies, we see a continued increase in the use of smart algorithms and error-correction techniques to compensate for increased device variability. In further response to these challenges, we see logic processes adopting FinFET devices along with read- and write-assist circuits in SRAMs. Meanwhile, emerging memory technologies are making steady progress towards product introduction, including PGRAM and ReRAM, while STT-MRAM is beginning to become a strong candidate for both standalone and embedded applications.

SRAM:

Embedded SRAM continues to be a critical technology enabler for a wide range of applications from high-performance computing to mobile utilization. The key challenges for SRAM include V_{CCmin} , leakage and dynamic power reduction while relentlessly following Moore's Law to shrink the area by 2× for every technology generation. As the transistor feature size has marched to below 30nm, device variation has made it very difficult to shrink the bit-cell size at the 2× rate, while maintaining or lowering V_{CCmin} between generations. Starting at 45nm, the introduction of high- κ metal-gate technology reduces the V_t mismatch and further enables device scaling by significantly reducing the equivalent oxide thickness. Starting at 22nm and beyond, new transistors such as FinFETs and fully-depleted SOI are key to enabling the continuous scaling of bit-cell area and low-voltage performance. Design solutions such as read/write-assist circuitry have been used to improve SRAM V_{CCmin} performance starting at 32nm. New SRAM bit cells with more than 6 transistors have also been proposed to minimize operating voltage. For example, 8T register file cells have been reported in recent products requiring low V_{CCmin} . Dual-rail SRAM design emerges as an effective solution to enable Dynamic Voltage-Frequency Scaling (DVFS), by decoupling the logic supply rail from the SRAM

array, thus allowing a much wider operating window. It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope for succeeding feature-size reductions. Sleep transistors, fine-grain clock gating, and clock-less SRAM designs have been proposed to reduce leakage and dynamic power. Redundancy and ECC protection are also keys to ensure yield and reliability when embedded SRAM products go into production. Figure 12 shows the trend in SRAM-bit-cell scaling on the left axis, and the trend in SRAM supply-voltage scaling on the right axis, using data from major semiconductor manufacturers.

High-Speed I/O for DRAM:

In order to reduce the bandwidth gap between main memory and processor frequencies, external data rates continue to increase as conventional high-speed wired interface schemes (such as DDRx and GDDRx for DRAM) evolve, as shown in Figure 13. Currently, GDDR5 and DDR4 memory I/Os operate around 7Gb/s/pin and 3Gb/s/pin, respectively. To achieve higher data-transfer rates, signal-integrity techniques (such as crosstalk, noise and skew cancellation), and speed enhancement techniques (such as equalizers and pre-emphasis) have been developed. These advanced techniques have pushed I/O speeds towards 10Gb/s/pin. Lower power consumption for data-center and mobile applications has also been pursued. A near-ground signaling method, termination impedance optimization, decision feedback equalization, and clock-feathering slew-rate control technologies have been demonstrated to reduce the power dissipation of memory interfaces significantly, while achieving high bandwidth.

NonVolatile Memories:

In the past decade, significant focus has been put on the search for emerging memories to provide a possible alternative to floating-gate NonVolatile Memory (NVM). The emerging NVMs, such as Phase-Change Memory (PRAM), Ferroelectric RAM (FeRAM), Spin-Torque-Transfer Magnetic RAM (STT-MRAM), and Resistive Memory (ReRAM), are showing the potential to achieve high-cycling capability (operational lifetime), and lower power per bit for both read and write operations. Some commercial applications, such as cellular phones, have recently begun to use PRAM, demonstrating that reliability and cost competitiveness of emerging memories is becoming a reality. Fast write speed and low read-access time are being achieved in many of these emerging memory schemes. At ISSCC 2013, a 32Gb ReRAM cross-point array is demonstrated in 24nm technology. Figures 14 and 15 provide a summary of the scaling trends for both bandwidth and density of emerging memories.

NAND Flash Memory:

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with Solid-State Disks (SSDs). The use of multiple bits per cell has proven to be effective in increasing the density. Figure 16 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 18 years. With scaling, device variability and error rates increase, requiring system designers to develop sophisticated control algorithms to compensate. Some of these algorithms are implemented outside the NAND silicon, in the system memory controller (in particular, the ECC and data management methods), for improved overall reliability. Possible future scenarios include 3D-stacked NAND vertical gates as a solution to further increase overall NAND-memory density.

Current state-of-the-art results from ISSCC 2013 include:

- 32Gb ReRAM test chip developed in 24nm CMOS
- The first ever 128Gb 3b/cell NAND Flash design in 20nm planar-cell CMOS
- A 45nm 6b/cell charge-trapping Flash memory using LDPC-based ECC demonstrates 10-year error free operation.
- A highly efficient 6.4Gb/s near-ground single-ended low-common mode transceiver for memory interface
- A highly efficient SRAM operating at 0.6V used statistically-gated sense amplifiers

Radio Frequency (RF)

Across the broad spectrum of RF applications in all frequency bands, this year ISSCC 2013 provides evidence of increasing integration and technical maturity, while at the same time, innovation proliferates. What follows, outlines emerging RF trends to be revealed there.



There is an ongoing drive toward increasing levels of integration in all areas of RF design, from mm-Wave, to cellular, to imaging, to wireless sensors. In mm-Wave designs, higher system complexity (including front-end, synthesizer, and baseband) is increasingly being integrated onto a single die. In cellular, the push for integration has led to a strong trend toward architectures allowing better linearity and co-existence of these multiple bands and standards. A related trend has been increasing research directed toward removing costly and bulky SAW filters and duplexers; Some of these efforts include the creation of highly linear blocker-tolerant receivers, mixer-first receivers, feedback blocker cancellation, feed-forward blocker cancellation, N-path filters, and electrically balanced hybrid transformers. Strong effort continues toward integration of CMOS PAs, while delivering viable power-efficiency performance. Overall, this year at ISSCC 2013, there has been a marked appearance of a significant number of chips in 65nm CMOS as opposed to other technologies. This observation can be noted across all frequency ranges and all circuit topologies. It is evident from ISSCC 2013 that RF devices will continue to see larger levels of integration at the chip- and package-level for years to come.

Over the past decade, the papers submitted to ISSCC have indicated a clear trend toward higher frequencies of operation in CMOS and BiCMOS. This year, this continues for oscillators, mm-Wave amplifiers, and PAs. Another trend is toward the increasing complexity of systems operating in the 60-to-200GHz range; this push to ever-higher frequencies is being pursued by both industry and academia for various applications, such as high-data-rate communication. With the low-GHz frequency spectrum already overcrowded, researchers are continuing to target frequencies above 60GHz. Other applications for products operating in these frequency bands include imaging and radar; these frequencies are desirable for such products due to their high spatial resolution, and facilitation of small antenna dimensions, allowing efficient beam-forming arrays; this integration of mm-Wave antennas into silicon substrates is another increasingly visible trend.

As a consequence of the trends to increase integration and to higher frequencies, a new class of fully-integrated application-driven systems have emerged: The availability of many RF and mm-Wave building blocks in CMOS and BiCMOS is motivating fully-integrated solutions for specific emerging applications in the RF and mm ranges: Single-chip radars in RF and mm-Wave frequencies with improved resolution, improved efficiency, showing increasing levels of integration, are appearing. Similarly, new systems are being developed for ultra-wideband radar and mm-Wave wireless sensing. Developments in the biomedical field are clearly moving from the simple measurement of electrical parameters towards the measurement of real medical properties in realistic environments through the use of Systems-in-Package (SiP).

Complexity and Maturity in the mm-Wave and sub-mm-Wave Ranges:

The high cutoff frequency of bipolar transistors and highly downscaled MOS transistors has enabled the realization of circuits and systems operating in the mm-Wave range. In the past few years, high-data-rate communication in the 60GHz band and car radar around 77GHz have garnered much attention. While the integration level in these domains is already quite high, we see an improvement in performance of various building blocks (such as output power of PAs, and spectral purity and tuning range of VCOs).

The 100GHz barrier for operation of silicon circuits was breached a few years ago. Whereas initially elementary building blocks such as VCOs and amplifiers operating above 100GHz have been realized, we now witness the trend of increasing complexity in circuits operating there. Meanwhile, the electrical performance at the building-block level has improved: As shown in Figures 17 and 18, the output power of mm-Wave and sub-mm-Wave sources and PAs has increased; as well, VCOs are operating at ever-increasing frequencies with a higher tuning range.

Co-Existence and Efficiency for Cellular Applications:

RX and TX Linearization: In the past few years there has been an increasing interest in techniques for improvement in the linearity of transmitters and receivers. Improved linearity of receivers will ease the requirements on RF filtering of out-of-band blockers, requiring, for example, only the use of a programmable notch filter in the RF path. Transmitter linearity improvements will benefit performance parameters such as Error-Vector Magnitude (EVM), ACLR, and spectral purity.

PA Efficiency: PA efficiency improvements demonstrated this year at ISSCC 2013 will directly impact the battery life in portable applications. These efficiency-improvement techniques include analog and digital pre-distortion, dynamic biasing, and envelope tracking.

Digitally-Assisted RF: The trend towards digitally-assisted RF continues and is increasingly applied in mm-Wave chips. More digitally-assisted calibration techniques are being demonstrated in order to improve the overall performance of transceivers by reducing the impact of analog impairments at the system level. These techniques include: spur cancelation/reduction, IIP2 improvements, and digital pre-distortion.

VCOs: There is a continuing trend toward improvements in phase-noise Figure-of-Merit (FOM) and power consumption through circuit techniques used in Class-C and Class-D VCOs. Figure 19 shows trends in VCO FOM performance of some of the most significant VCOs published over the past decade. As can be seen, ISSCC 2013 demonstrates clear contributions to this field.

Thus, overall, we see both the improvement of sustaining RF techniques, and the dramatic extension and growth of RF toward new areas of application at ever-higher frequencies.

Technology Directions (TD)

The role of the Technology-Directions Subcommittee is to identify and encourage developments of potential importance in the ongoing evolution of ISSCC. Characteristically, a wide variety of topics are covered, some new and some continuing, with success achieved by the transference of the emerging technique to one of the evolving mainstream Subcommittees. This year, at ISSCC 2013, two strong emerging trend directions are visible: in flexible electronics; and in nonvolatile memory.

Large-Area Flexible Electronics:

In the field of flexible large-area electronics fabricated at low-temperatures, the current focus is now on lowering the cost-per-unit-area, rather than on increasing the number of functions-per-unit-area that is the focus of crystalline silicon technology, following Moore's Law.

A clear breakthrough in research for large-area electronics in the past decade has been the development of Thin-Film-Transistor (TFT) processes with an extremely low temperature budget (<150°C), enabling manufacturing on flexible and inexpensive substrates such as plastic films and paper.

For some time, the materials used for these developments have been carbon-based organic molecules such as pentacene, with properties of p-type semiconductors. More recently, air-stable organic n-type semiconductors and amorphous metal oxides, which are also n-type semiconductors, have emerged. The most popular metal-oxide semiconductor is amorphous Indium Gallium Zinc Oxide (IGZO), but variants exist (Zinc Oxide, Zinc Tin Oxide, and so on). The mobility of n- and p-type organic semiconductors has reached values exceeding 10cm²/Vs, which is already at par or exceeding the performance of that using amorphous silicon. Amorphous metal-oxide transistors have typical charge carrier mobility of 10-to-20cm²/Vs. Moreover, operational stability of all organic semiconductor materials has greatly improved to a level sufficient to enable commercial applications, especially in combination with large-area compatible barrier layers to seal the transistor stack.

In the present state-of-the-art, p-type only, n-type only, and complementary technologies are available. For the latter, all-organic implementations are available, but also we see hybrid solutions, featuring the integration of p-type organic with n-type oxide TFTs. At present, most TFTs are still manufactured with technologies from display-lines, using subtractive methods based on lithography. However, there is a clear emphasis on the development of additive technologies that could provide higher production throughput, based on different approaches borrowed from the graphic printing world, such as screen and inkjet printing. The feature sizes and spread of characteristics of printed TFT technologies are still larger than those made by lithography, but there is clear progress toward size reduction.

The primary applications for such TFT systems are as backplanes in active-matrix displays, particularly flexible ones. Organic TFTs are well-suited for electronic-paper-type displays, whereas oxide TFTs are targeting OLED displays. Furthermore, TFTs on foil are well-suited for integration with temperature or chemical sensors, to create pressure-sensitive foils, photodiode arrays, antennas, sheets capable of distributing RF power to appliances, energy scav-

enging devices, and so on, in hybrid integrated systems on foil. Early demonstrations include smart labels, smart shop shelves, smart medical patches, and so on. These are enabled by continuous progress in the complexity of analog TFT circuits targeting the interface with sensors and actuators, to modulate, to amplify, and to convert analog signals, as well as progress in digital TFT circuits and nonvolatile memory for signal processing and storage.

Nonvolatile Memory in Logic:

With continuing technology scaling, advances in energy-efficient computation will become even more important. Correspondingly, at ISSCC 2013, a new trend can be seen: It involves the integration of nonvolatile memory with logic for ultra-fast power-down/power-up while maintaining the state of the computation. Such technologies will impact future mobile platforms and industrial applications, making mobile computing truly ubiquitous.

Thus, we see two examples of the many new directions in which the electronics industry are likely to flow, as continuously uncovered by technology directions at ISSCC.

Wireless

Data rates for modern wireless standards are increasing rapidly. This is evident from the pace of the introduction of cellular standards shown in Figure 20. Note that the data rate has increased 100x over the last decade, and another 10-fold increase is projected for the next five years. This trend is partly supported by the use of more-complex modulations (such as using Orthogonal Frequency Division Multiplexing (OFDM) for better spectral efficiency) at the cost of Digital Signal Processing (DSP). In addition, the expansion of channel bandwidth has helped to achieve the data rate increase. This is exemplified for 802.11x in the wireless connectivity chart shown in Figure 21. The channel bandwidths for the WLAN standards has increased from the traditional 20MHz (802.11g) all the way to 2.16GHz (802.11ad). Because the available spectrum is limited in the low GHz range, for >1GHz channel bandwidth, the carrier frequency has moved from 2.4/5GHz (802.11a/b/g/n/ac) to 60GHz (802.11ad), in the mm-Wave range. With the available spectrum in the 60GHz range, data rates up to 6.76Gb/s can be achieved. However, design at mm-Wave frequencies comes with significant challenges, with academic research oriented to the reduction of power, while industry focuses on product-quality robustness and standards compliance. Currently, a new generation of chipsets, compliant with WiGig and 802.11ad, is ready for production.

Since spectrum is scarce, new carrier-aggregation techniques are being developed that can combine available channels in a flexible way, such as combining non-contiguous channels, or even channels in different frequency bands. Correspondingly, the new 802.11af standard aims to utilize “TV white space”, unused legacy analog TV frequency bands below 1GHz. This will be implemented, first using a database of available channels per geographical location, but eventually high-sensitivity spectrum sensing will be used to confirm the availability of the spectrum. The possibility of opening up this large amount of spectrum generates radio challenges, such as the need for highly-linear transceivers that can cover a very-wide frequency range and various channel bandwidths. As a consequence of high-linearity and wideband design requirements, distortion cancellation and tunable RF channel-selection techniques are very critical. Most transceivers in this category are adopting digital calibration and analog-feedback techniques to increase the linearity performance for a flexible and tunable front-end to cover a wide range of frequencies.

As wireless technology lowers in cost, it can be deployed in many devices, including sensors for monitoring environmental conditions. Wireless Sensor Networks (WSNs) require ultra-low-power radio to increase battery life and minimize the battery size, or better yet, eliminate the battery altogether by using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. A “wake-up radio” that monitors the channel and alerts the “main” radio when communication is requested becomes the primary building block for WSN designs. Once the radio is awake, power efficiency becomes the main target for both high- and low-data-rate communication. Another approach is to duty-cycle the radio operation, such as using the radio only for short communication bursts, which requires fast turn-on techniques. Such WSNs will enable electronics for sustainability.

Similar to the evolution in cellular, ultra-low-power radios are now becoming multistandard, covering for example Zigbee, BTLE, and IEEE 802.15.6. Multistandard implementation implies radio-block sharing, and standards management, including modulation, frequency, bandwidth, power output, sensitivity, and so on, while maintaining low power consumption, which is one of the keys to the success of such devices. Another main concern is the price. These multistandard radios must have small-silicon-area circuits in low-cost packaging.

Near Field Communication (NFC) is becoming more and more popular. This new secure-data wireless transmission mode is now embedded in smart phones and will become a *de-facto* requirement in coming years.

Digital architectures implementing radio functions are very efficient in deep-nm CMOS. In the past years, digital-PLLs have been developed for radio front-ends. Now, new digital approaches are being deployed in transmitters, targeting greater flexibility of the RF front-end that leverages CMOS scaling for reduced power dissipation and area, simplifying integration in large SoCs, and empowering the next generation of wireless communications.

Wireline

Wireline continues to be an important application of semiconductor technology as the need for wired communication flows out from its long distance origins into smaller and smaller environments, through backplanes to inter- and intra-chip connection. A continuing challenge in this evolution is the adaptation of techniques that originated on a large scale to shrinking environments.

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2-to-3x every 2 years. Demand for bandwidth has been driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth has been enabled by expanding the number of I/O pins per component. But, as a result, I/O circuitry consumes an increasing amount of area and power on today's chips. However, increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 22 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 23 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process-technology scaling. However, continuing with this rather amazing trend in I/O scaling will require more than just transistor scaling in the future. Significant advances in both energy efficiency and signal integrity must be made to enable the next-generation of low-power and high-performance computing systems.

Power Consumption and Energy Efficiency:

Power consumption for I/O circuits is a first-order design constraint for systems ranging from mobile phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. However, there is a strong correlation between the energy efficiency and the distortion introduced by the channel. Figure 24 plots the energy efficiency (expressed in mW/Gbps, which is equivalent to pJ/b) as a function of Nyquist loss for recently reported transceivers. These transceivers cover a wide variety of standards and process technologies. Based on these data points, the scaling factor between link power and signaling loss is approximately unity, meaning that required link power doubles with every additional 6dB of channel loss. As a result, simply increasing per-pin data rates with existing circuit architectures and channels while only scaling transistors is not a viable path, given fixed system-power limits. To address this issue, recent link research has focused on reducing power through both circuit and channel innovation. There have been a number of advances that reduce power through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS resonant clocking, low-swing voltage-mode transmitters, and links with low-latency power-saving states. Based on the relationship between channel loss and energy efficiency, power can also be reduced by changing the interconnect itself to either reduce the total loss or increase the interconnect density. Examples of these approaches include stacked die TSVs and proximity inter-



connects, silicon interposers, on-package I/O, and low-loss flexible interconnect. At ISSCC 2013, reported developments move the state-of-the-art well below 1pJ/b for short-range links. For example, a 20Gb/s chip-to-chip transceiver consuming only 540fJ/b is reported which employs single-ended ground-referenced signaling across high-density package interconnects. Another development describes a 1Tb/s aggregate bandwidth across low-loss flexible cabling consuming 2.6pJ/b.

Electrical Links:

Some types of channels, especially those related to medium-distance electrical I/O (such as server backplanes), must support high data rates along with high loss. Others (such as DDR), must contend with increasing amounts of crosstalk in addition to channel loss. For these links, the key to scaling has been improvements in clock jitter and equalization. There are several recent examples of transceivers able to signal across 30 to 35dB of loss at the Nyquist frequency at data rates up to 28Gb/s. These transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. In some cases, equalization is being done in the digital domain after first converting the data signal using 5-to-6b ADCs. Although the energy efficiency for these systems tends to be lower than in conventional equalization approaches, they enable more complex and flexible equalization techniques, as well as requiring equalization power that may scale more gracefully. A number of CDR circuit techniques have also been developed for these high-loss transceivers, including digital CDRs that employ baud-rate sampling, oversampling, and even blind sampling techniques. At ISSCC 2013, the fastest link components reported to date, includes a 66Gb/s 3-tap DFE consuming only 46mW without loop unrolling, and a 48Gb/s 88mW TX, both in standard 65nm CMOS. Also demonstrated are other significant advances in fully-integrated high-speed transceivers: A 39.8-to-44.6Gb/s chipset in 40nm CMOS, and several 32Gb/s TX and RX equalizers compensating up to 40dB of channel loss.

Optical Links:

As the bandwidth demand for traditionally electrical wireline interconnects accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnect. Relative to electrical interconnect, optics provides lower loss and potentially higher density through techniques, such as wavelength-division multiplexing. Optical components (including VCSELs, Mach-Zehnder Interferometers (MZI), optical ring modulators, and photodetectors) are simultaneously being developed for higher performance, lower power, and higher degrees of integration in standard CMOS processes. Circuit-design techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links requiring extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane, and chip-to-chip optical communication. ISSCC 2013 includes several examples of 25Gb/s optical transceivers, employing an RX that consumes only 4.9pJ/b. As well, ISSCC 2013 highlights significant advances in silicon photonic integration, including a 20Gb/s driver and associated silicon photonic MZI, and a 2.5Gb/s driver and ring modulator designed and fabricated in a standard CMOS process.

Overall, the continuing scaling of I/O bandwidth is both essential for the industry, yet extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain these goals. Advances in circuit architecture, interconnect topologies, and transistor scaling are, together, changing how I/O will develop over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2013.

Summary

Developments reported at ISSCC 2013 continue to present breakthroughs in the broad domain of solid-state circuits and systems. In this rich environment, presentations at ISSCC characteristically predict ways in which electronics techniques will fulfill the present and future needs of society. In this role, ISSCC continues to present a road map of things to come, both in the immediate future and in the longer term.

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Attendees at the Plenary-Session Break at ISSCC 2007.

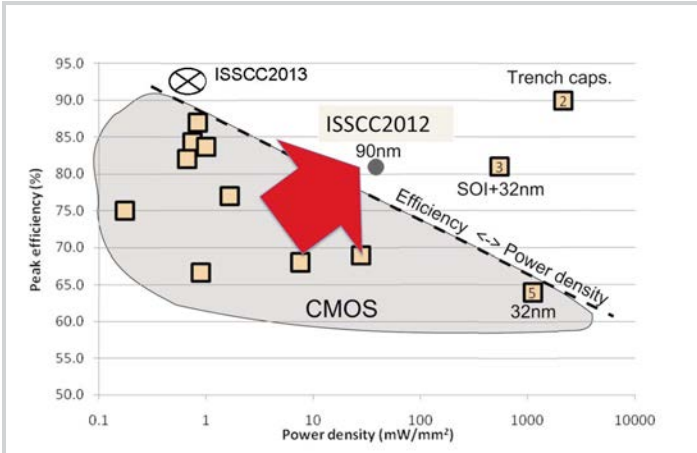


Figure 1: The development of integrated power conversion: Each year, more and more is integrated in standard CMOS technologies, optimizing efficiency versus power density. At ISSCC 2013, these trends are evident in a shift to higher performance, as shown by the arrow directed to the upper right.

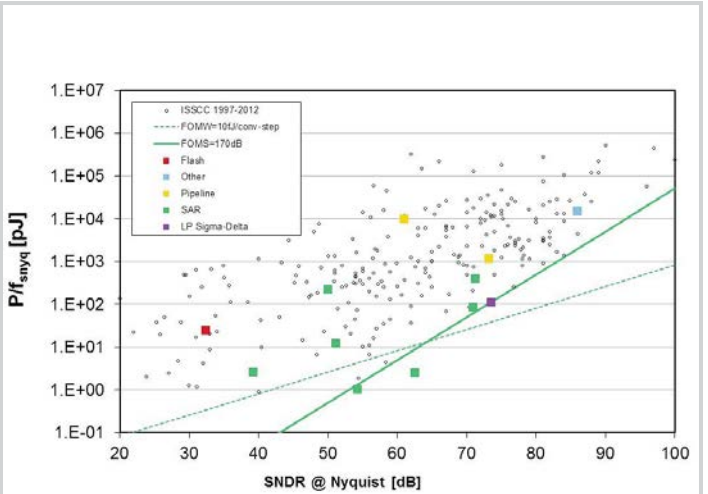


Figure 2: Power efficiency vs SNDR (highlighting ISSCC 2013 results).

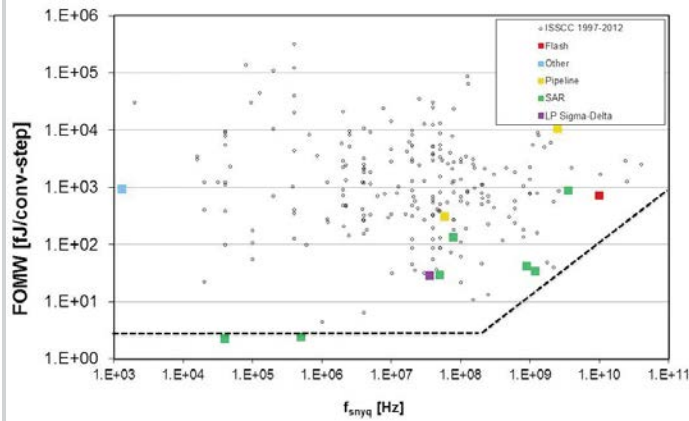


Figure 3: FoM (energy per conversion step) vs Nyquist-bandwidth for various converters.

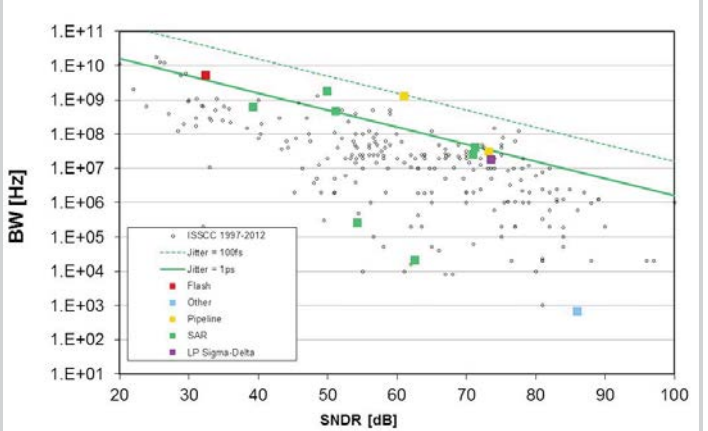


Figure 4: Bandwidth vs SNDR.

Graphics	2D, 3D	OpenGL (ES1.1)	OpenGLVg/MAX (ES2.0)	AR (Augmented Reality)						
Display	16b QVGA	VGA	Dual 24b WVGA @ 60fps	Dual 24b Stereo SXGA @ 60fps						
Camera	1-2M	3M	5-8M	10M	16M	20M	Dual camera			
Image/Video	JPEG, MPEG-4	H.264/AVC (VGA)	H.264/AVC (D1)	H.264/AVC (Full HD)		H.264/MVC H.264/SVC				
Audio	MP3	AAC	AAC Plus	WMA Dolby 5.1		Dolby TrueHD/Digital+				
Accelerator	DSP	FPU	SIMD Multi-core		Many-core					
downlink [Mb/s]	EGPRS 0.4	UMTS 0.4-2	HSPA 1.8-7		HSPA+ 7-42		LTE 100			
CPU [MIPS]	-300	300-500	500-800		800-2400		2400-6000			
	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013

Figure 5: Developments in application processors for smart phones.

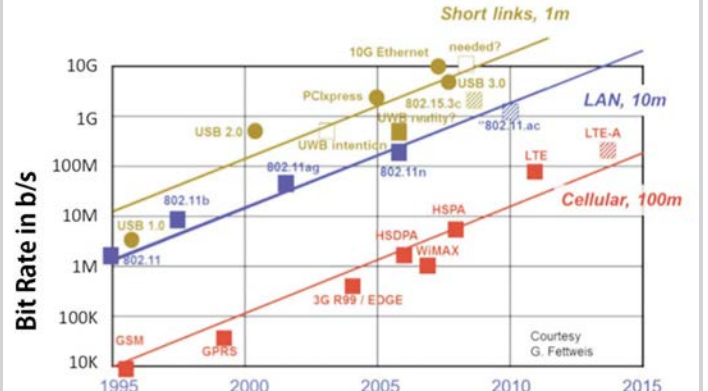


Figure 6: Wireless and wired data rates over time.

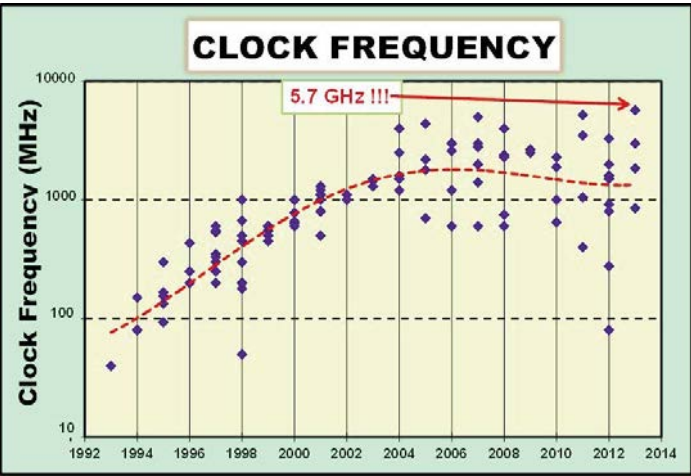


Figure 7: Chip Complexity.

Figure 8: Clock Frequency.

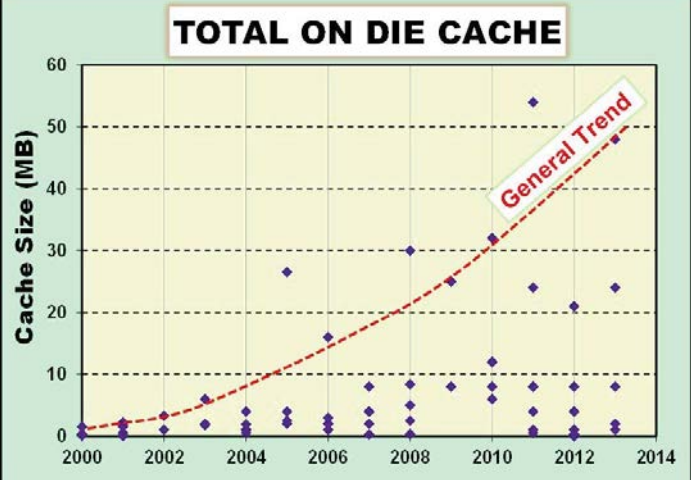
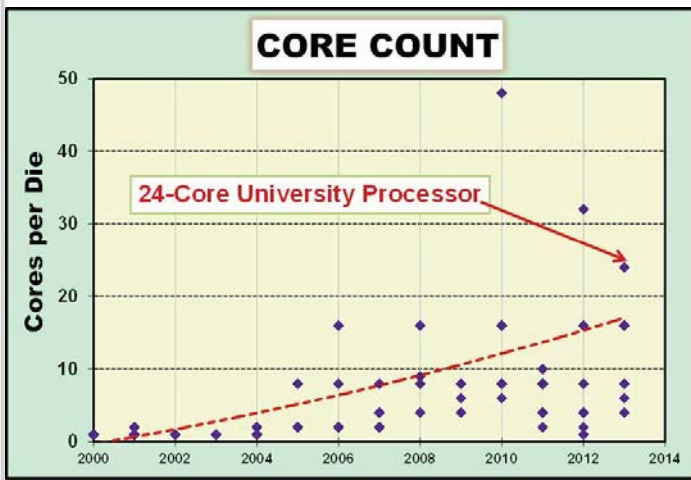


Figure 9: Core Count.

Figure 10: Total On-Die Cache.

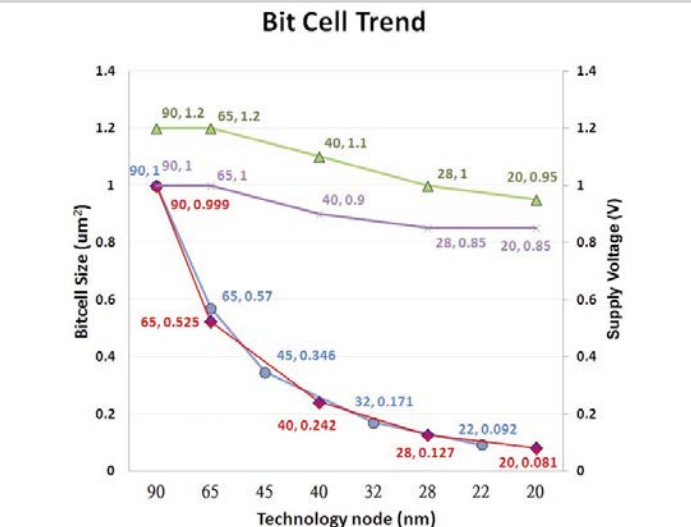
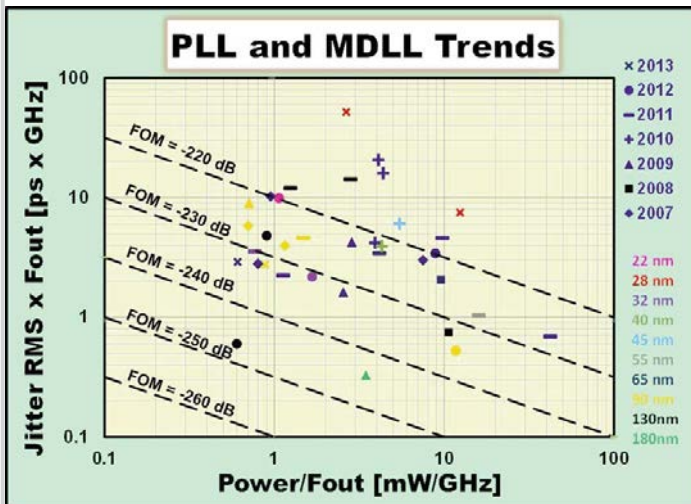


Figure 11: PLL and MDLL Trends.

Figure 12: SRAM bit-cell size and supply scaling range from major semiconductor manufacturers.

Data Rate for DDRx and GDDRx

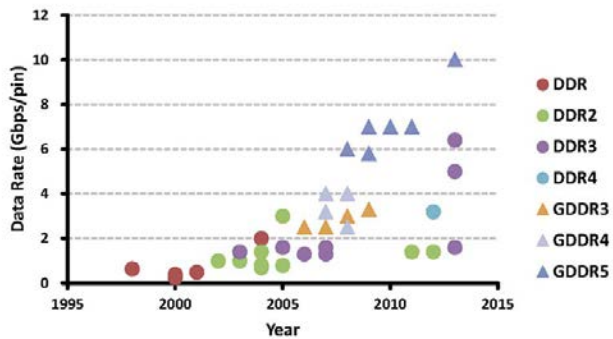


Figure 13: Trends in DRAM data rate/pin.

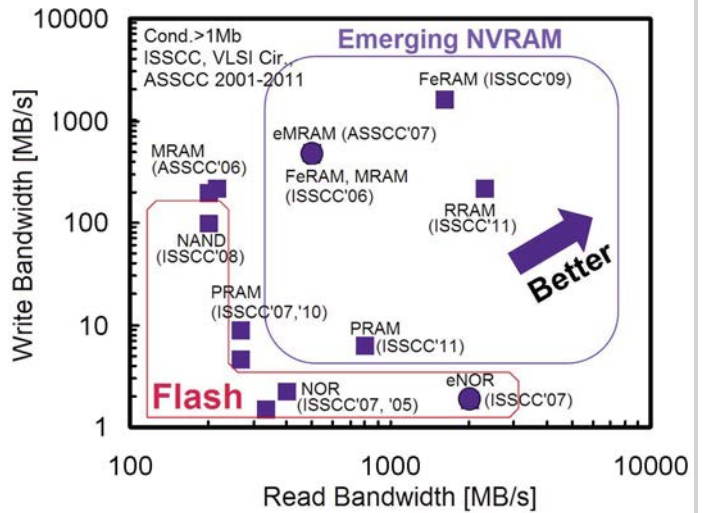


Figure 14: Read- and write-bandwidth comparison of nonvolatile memories.

Storage Capacity [Mb].

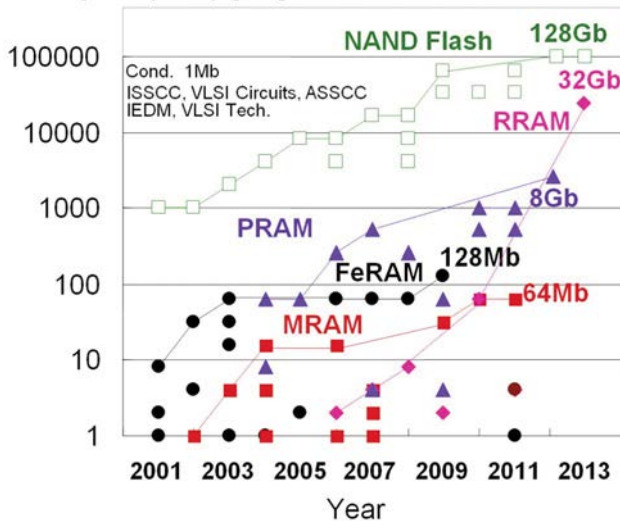


Figure 15: Memory capacity of emerging nonvolatile memories.

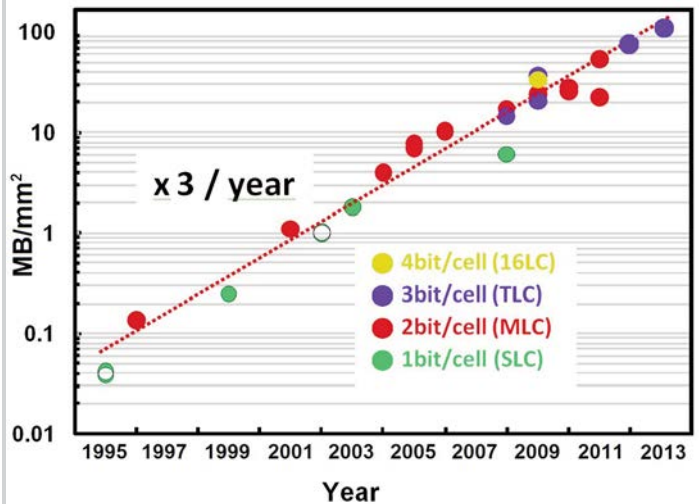


Figure 16: NAND Flash memory density.

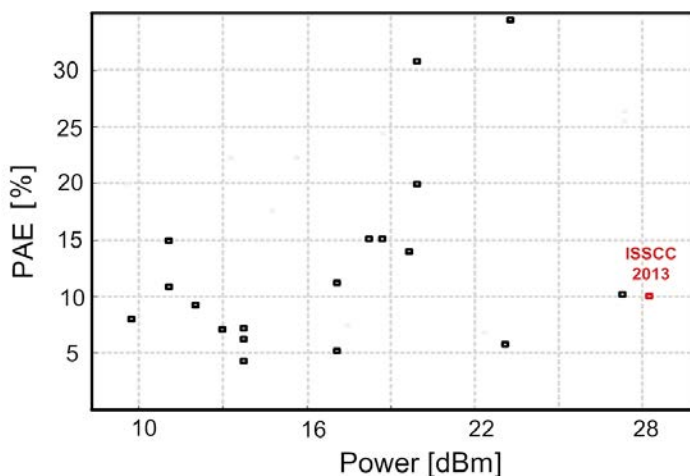


Figure 17: PAE vs output power for recent submicron mm-Wave CMOS PAs.

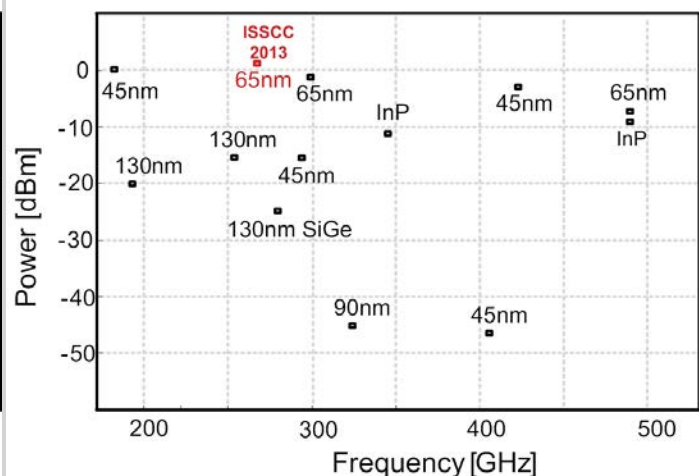


Figure 18: Output power vs frequency for mm-wave and sub-mm-wave sources.

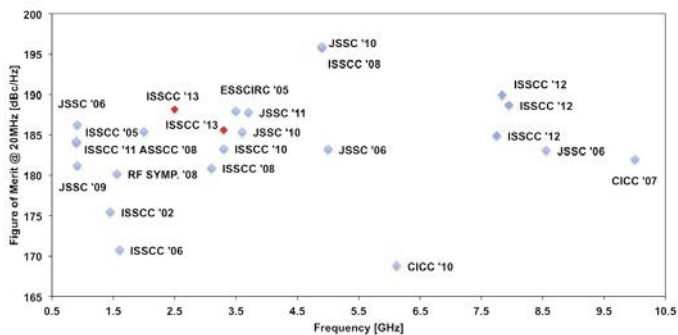


Figure 19: Phase-Noise FOM at 20MHz offset frequency vs oscillation frequency.

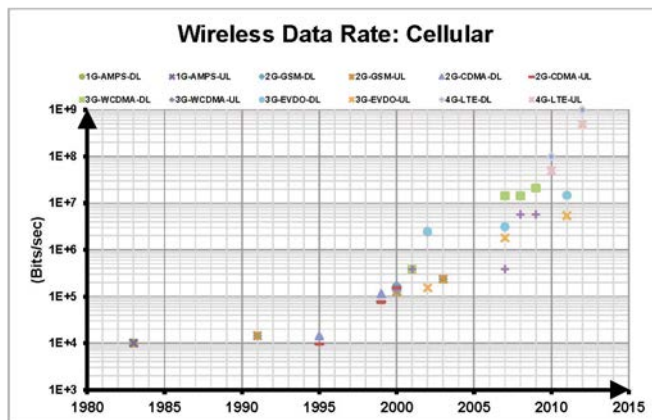


Figure 20: Data Rates for Cellular Standards.

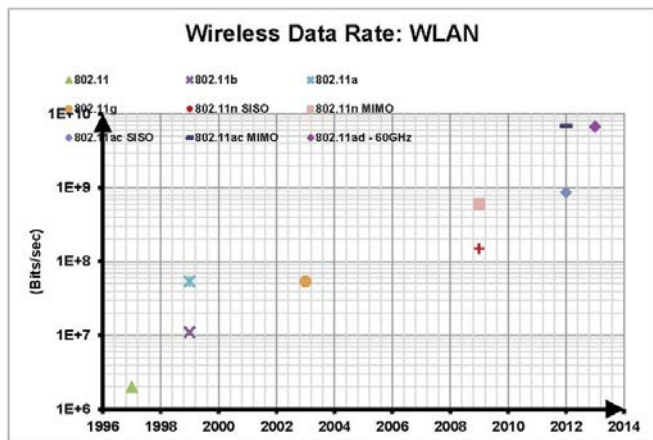


Figure 21: Data Rate for Wireless Connectivity Standards (802.11x).

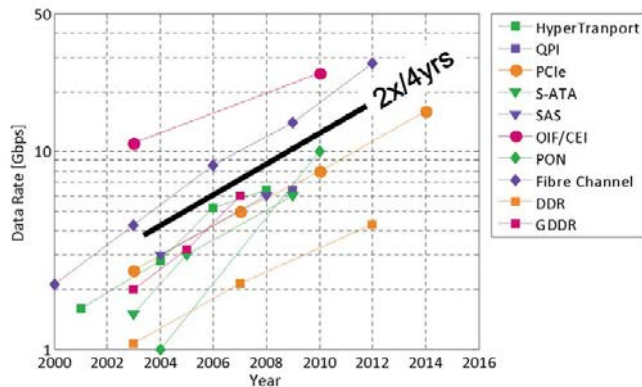


Figure 22: Per-pin data rate vs year for a variety of common wireline I/O standards.

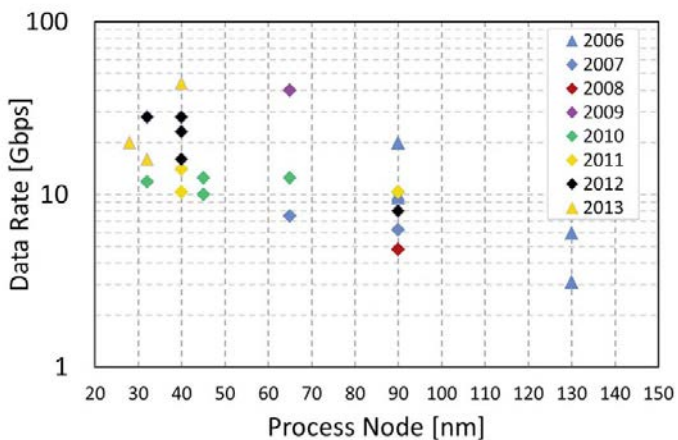


Figure 23: Wireline Data Rate vs Process Feature Size and Year.

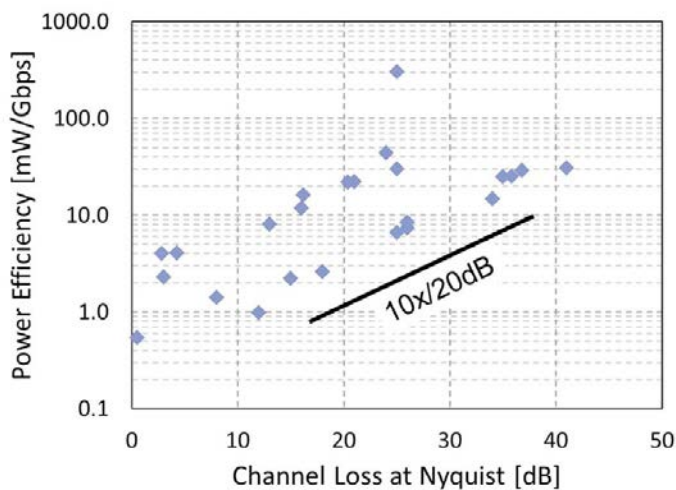


Figure 24: Wireline Transceiver Power Efficiency vs. Channel Loss.

THE VISUALS SUPPLEMENT AND THE SARATOGA GROUP – A 24 YEAR EVOLUTION

Laura Chizuko Fujino, University of Toronto, Toronto, Canada



Preamble:

The idea of providing attendees with all presentation material arose as a result of a variety of comments made in an attendee survey conducted for ISSCC 1989. The survey crystallized ideas which had been expressed for many years earlier concerning a heartfelt need to reconcile two problems that had long bothered the attendees: The first was dissatisfaction with those who snapped photos of the slides during presentations; The second was the often-heard lament that the audience was shown marvelous things that were not recorded or depicted in the Digest.

Since the data reduction of the survey was assigned to K.C. Smith, Laura Fujino performed the work, and was graciously allowed to present the findings at the August Executive Committee meeting in 1989. Amid a lot of discussion of various topics raised by the Survey, a decision was made by the Executive Committee that something needed to be done, and that a solution lay in some mechanism to provide copies of the all presentation slides to all attendees, after the Conference. Subsequent to the meeting in which Laura Fujino was present only for the Survey presentation, David Pricer as the Executive Committee Chair was assigned to seek some mechanism for the resolution of this problem. Shortly thereafter, he contacted Laura Fujino with an invitation to join the Executive Committee with the role of addressing this challenge. Within a few weeks, a concept emerged on how to proceed: The existence of a photocopier with a slide carousel-projector attachment was identified from which medium-size paper copies of the slides could be made. As well, this photocopier had a paper to paper enlarging/reduction facility, which though of limited range could be used in multiple passes to acquire a paper image of the desired size.

A production process was conceived as follows: Soon after the completion of the talk, the author's slide carousel was used to produce a set of paper images; later these images were sized using the photocopier to provide paper images that where combined on a fifteen-per-page presentation, by a manual cut-and-paste process; this was combined with the title, author data, and abstract, in a nominal two-page format with extensions at the back of the compiled book, called the "*Slide Supplement to the Digest of Technical Papers*".

Correspondingly, during the 1990 Conference held at the San Francisco Hilton, a group of volunteers and one part-time casual employee met in the "Saratoga Room" to implement this process. The group included: John Eggert (Digest and Supplement printer) and his wife Shirely, John Wuorinen (Digest Editor) and his wife Susan, Nancy Pricer, wife of Dave, Henry Osborne, K.C. Smith, under the direction of Laura Fujino. Thus, thereafter, this group was called the "Saratoga Group". Since the process was machine limited it took very long days to maintain a reasonable schedule with two operators (Henry and Laura). John Eggert led the manual final layout process, while Nancy Pricer collected the slides and sized paper copy, and the others were involved primarily with image sizing. (It was pleasing to note that no blood was spilled during the cut-and-paste process!) The final product, the ISSCC 1990 Slide Supplement was printed, bound, and mailed to all attendees, about one month after the Conference.

Later Developments:

The acceptance of the first edition of the Slide Supplement was sufficiently strong that we were encouraged to continue the logical development of the original concept. For the next two years, ISSCC 1991 and 1992, the process continued with some modification (including an eight-per-page format) in the "Saratoga Room" at the San Francisco Hilton. For ISSCC 1993, operations were moved to the San Francisco Marriott, where the Conference has remained.

For ISSCC 1991 and 1992, the major change was replacement of some of the initial volunteers and casual employee in the "Saratoga Group" by graduate-student volunteers from the University of Toronto.

For ISSCC 1993, following a change of the printer, Pat Duplessis joined the team in charge of manual page layout. This process continued with one major change, until electronic projection was introduced in 2001. The major change, introduced at ISSCC 1993, was to use author provided hard copy of their 35mm

slides to simplify image production but requiring a slide-to-paper checking process, which in turn required more volunteer students, but was otherwise faster and did not rely as much on unreliable equipment. For ISSCC 1997, Steve Bonney joined Pat Duplessis for page layout. For ISSCC 1998, 1999, and 2000, we replaced much of the photo reduction by scanning the author's hard copy, and thereafter, sizing and page layout by computer.

For ISSCC 2000, an experiment was conducted with electronic projection (replacing slide carousels by computer-driven projectors) in three sessions, necessitating some additional image processing for Supplement production. For ISSCC 2001, electronic projection for day sessions became the norm. This included the use of multiple computers for back up and reliability, with the need for more student volunteers to operate them, and provide set up and checking. At the same time, the name "Slide Supplement" was changed to "Visuals Supplement", and the task of page layout was assigned solely to professionals.

The Graduate-Student Volunteer Group:

Today, the graduate-student volunteers, the major part of the current Saratoga Group is involved in a diverse set of tasks: Before the Conference they set up and check the laptops of which three are used for each regular session to provide projection, projection back-up, and audio recording, as required; organize Speaker and Committee Registration material; handle corresponding Speaker and Committee Registration; setup equipment for Speaker Rehearsal; assist with Speaker Rehearsals; assist with Plenary Speaker Rehearsal; unpack and check Award plaques, organize and transport to the ballroom; man the Press desk; interact with unionized A/V staff; check slides with Speakers prior to presentation; operate the computer projection system for Tutorials, Forums, Plenary Session, Regular Sessions, Evening Sessions, Short Course; assist speakers during the question and answer period; operate the recording system for the Plenary Session, Tutorials, and Short Course; act as videographers for the Demonstration Sessions; take photos of on-going events; complete data reduction for Tutorials, Forums, Short Course; perform high light data reduction for Regular Sessions for JSSC paper selection; help with crisis intervention.

Over the past 24 years, the number of graduate-student volunteers annually has ranged from 2 for ISSCC 1991 through a peak of 22 for ISSCC 2008 (to support the audio recording of the entire Conference), to 17 for ISSCC 2012 and 2013.

An interesting vignette concerning the performance of the volunteer students occurred early on in the context of their handling of electronic-projection systems. Virtually at the moment that student operated projection began, there were many reports from attendees concerning a magical process that they had observed during the question and answer periods of sessions that they had attended: Their common comment was that miraculously, during the formation of the question by a questioner that a highly relevant slide illustrating the subject of the question and often its answer would appear suddenly on the screen. Their subsequent question to me was what marvelous artificial intelligence software had we acquired that allowed such instant insight and response! My retort was that it was not magic, but simply the consequence of care in selecting and assigning of the graduate-student volunteers: Each of them was highly selected from amongst senior members of a large graduate-student body, typically in the PhD program, or at the end of a Masters degree from a range of circuit-related specializations; further they were assigned to sessions that were in their area of research interests. Thus, they were amongst the most astute listeners in the audience!

It is interesting to note that a large fraction of these Saratoga-Group graduate-student volunteers have gone on to very successful careers in the solid-state area, both in industry and academia. Increasingly, one can find them presenting a paper at ISSCC!

Conclusion:

Upon reflection on the past 24 years, one is surprised that such a process evolved through technological change, personnel change, and vagaries of attendance variation. Beyond the annual appearance of increasingly higher quality of slide material, including videos, animation, and so on, the process has influenced an enormous number of young lives, hundreds of individuals whose outlook on life is different because of their week or so of frenetic, yet focused, activity at ISSCC.





IEEE Celebrates 50 Years

ISSCC 2013 congratulates each of the 9,400 current IEEE members who share the distinction of 50 years membership in the IEEE. To mark this occasion, they have each received an IEEE "Member 1st 50 Years" pin.

IEEE was founded on January 1, 1963, through the merger of the AIEE (founded in 1884) and the IRE (founded in 1912). Thus, 2012 marked IEEE's 50th year.

Of this 9,400, there are 120 in the IEEE Solid-State Circuits Society, as listed below. As well, the 9,400 includes a number of friends of ISSCC, some of whom we would like to acknowledge as indicated below. Please join ISSCC in congratulating these pioneering members of the IEEE.

SSCS members of the IEEE "Member 1st 50 Years" Pioneers

Ahmed, A	Dehoney, R	Kalander, G	Nishizawa, J	Spratt, James
Allen, Phillip	Diez, A	Kendal, Michael	Owen, Robert	Stangerup, P
Amazeen, Bruce	Dill, F	Kennedy, E	Oxner, E	Sterzer, Fred
Anderson, John	Doak, T	Kerwin, W	Penfield, P	Strain, R
Ball, J	Edelsohn, C	Kindlmann, Peter	Petschauer, Richard	Tauritz, Joseph
Batcheller, Robert	Embree, Milton	Knudsen, K	Phillips, Edward	Terman, Lewis
Berkovits, Robert	Fischer, John	Ladd, Glenn	Platt, Judith	Tongue, Ben
Bower, John	Fowler, Richard	Lagnado, Isaac	Polkinghorn, R	Trofimenkoff, F
Brennemann, A	Frescura, B	Leung, W	Price, Vernon	Venteicher, Leroy
Brewer, Joe	Gardner, Floyd	Lovelace, Ralph	Pricer, WD	Verhoeven, H
Brown, George	Gilbert, Barrie	Malmberg, James	Pritchard, R	Vittoz, E
Brownell, Dudley	Glaenzer, R	Mao, Roger	Rudolph, Raymond	Vutz, Peter
Buhler, O	Graham, Martin	Marren, Bernard	Rumin, Nicholas	Walden, R
Butz, A	Gray, W	Masenten, W	Sander, W	Wasserman, R
Callahan, D	Gutmann, Ronald	McCluskey, Edward	Scanlan, S	Waxman, R
Camenzind, Hans	Hant, W	Mccullough, Michael	Scull, Gerald	Weckler, Gene
Cappon, Arthur	Hashimoto, Ichiro	Meindl, James	Sekine, Keitaro	Weiner, Maurice
Cohen, E	Hepler, David	Morrell, Richard	Shopbell, Marlin	White, C
Colclaser, Roy	Hilibrand, J	Morris, Charles	Shoup, J	White, Marvin
Coles, William	Hodges, David	Moyers, Wayne	Shumacher, G	Wing, Omar
Craven, R	Hoff, M	Nahas, Joseph	Smith, Donald	Wozniczka, L
Danielson, G	Huber, William	Nelin, Bert	Smith, KC	Wyndrum, Ralph
Davis, Paul	Jelinek, Howard	Nevin, Joseph	Soderman, Donald	Yoshimura, Hisanori
Davis, W	Jespers, P	Newcomb, R	Solomon, James	Young, W

Some other friends of ISSCC from among the 9,400 IEEE Pioneers*

Gordon Moore, Takuo Sugano, Jerry Suran

*Our apologies if your name was not included in this list of ISSCC Friends.
If you would like to be included in future lists, please send a note to Laura Fujino (lcfujino@aol.com).

ISSCC Authors with 10 or More Papers in the Past 10 Years as Compiled from IEEE Xplore

Top 10 in Rank Order, Others Alphabetical

Author	Year of 1st Paper	Most Recent Paper	Affiliation	City	State/Country
Anantha Chandrakasan	1993	2013	Massachusetts Institute of Technology	Cambridge	MA/USA
Kofi Makinwa	2002	2013	Delft University of Technology	Delft	Netherlands
Bram Nauta	1995	2013	University of Twente	Enschede	Netherlands
Hoi-Jun Yoo	1995	2013	KAIST	Daejeon	South Korea
Tadahiro Kuroda	1992	2013	Kelo University	Yokohama	Japan
David Blaauw	2002	2013	University of Michigan	Ann Arbor	MI/USA
Gyu-Hyeong Cho	1997	2013	KAIST	Daejeon	South Korea
Ali Hajimiri	1998	2013	California Institute of Technology	Pasadena	CA/USA
Dennis Sylvester	2000	2013	University of Michigan	Ann Arbor	MI/USA
Takayasu Sakurai	1984	2013	University of Tokyo	Tokyo	Japan
Asad Abidi	1984	2012	University of California, Los Angeles	Los Angeles	CA/USA
Elad Alon	2004	2013	University of California, Berkeley	Berkeley	CA/USA
Mark Anders	2001	2012	Intel	Hillsboro	OR/USA
Pietro Andreani	2002	2013	Lund University	Lund	Sweden
Bertan Bakkaloglu	2003	2011	Arizona State University	Tempe	AZ/USA
Shekhar Borkar	1995	2012	Intel	Hillsboro	OR/USA
Jonathan Borremans	2007	2011	IMEC	Leuven	Belgium
Peter Buchmann	2005	2013	IBM	Rueschlikon	Switzerland
Rinaldo Castello	1984	2013	University of Pavia	Pavia	Italy
M-C Frank Chang	2003	2012	University of California, Los Angeles	Los Angeles	CA/USA
Liang-Gee Chen	2004	2012	National Taiwan University	Taipei	Taiwan
Jan Craninckx	1995	2013	IMEC	Leuven	Belgium
Hooman Darabi	2001	2013	Broadcom	Irvine	CA/USA
Vivek De	1993	2012	Intel	Hillsboro	OR/USA
Harmke de Groot	2010	2013	imec - Holst Centre	Eindhoven	Netherlands
Daniel Friedman	1997	2013	IBM T. J. Watson Research Center	Yorktown Heights	NY/USA
Mototsugu Hamada	1998	2011	Toshiba	Kawasaki	Japan
Pavan Hanumolu	2006	2013	Oregon State University	Corvallis	OR/USA
Toshihiro Hattori	1998	2013	Renesas Electronics	Tokyo	Japan
Masaaki Higashitani	2005	2013	Toshiba	Yokohama	Japan
Steven Hsu	2005	2012	Intel	Hillsboro	OR/USA
Qiuting Huang	1995	2010	ETH Zurich	Zurich	Switzerland
Johan Huijsing	1975	2013	Delft University of Technology	Delft	Netherlands
Hiroki Ishikuro	2003	2013	Keio University	Yokohama	Japan
Deog-Kyoon Jeong	1999	2013	Seoul National University	Seoul	South Korea
Young-Hyun Jun	2000	2012	Samsung Electronics	Hwasung	South Korea
Lee-Sup Kim	2005	2013	KAIST	Daejeon	South Korea
Eric Klumperink	2002	2013	University of Twente	Enschede	Netherlands
Marcel Kossel	2005	2013	IBM	Rueschlikon	Switzerland
Ram Krishnamurthy	2001	2012	Intel	Hillsboro	OR/USA
Hasnain Lakdawala	2008	2012	Intel	Hillsboro	OR/USA
Jri Lee	2005	2013	National Taiwan Univ.	Taipei	Taiwan
Domine Leenaerts	2002	2011	NXP Semiconductor	Eindhoven	Netherlands
Shen-luan Liu	2003	2013	National Taiwan University	Taipei	Taiwan
John Long	1996	2013	Delft University of Technology	Delft	Netherlands
Franco Maloberti	1996	2011	University of Pavia	Pavia	Italy
Sanu Mathew	2001	2012	Intel	Hillsboro	OR/USA
Andrea Mazzanti	2006	2013	University of Pavia	Pavia	Italy
Christian Menolfi	2001	2013	IBM	Rueschlikon	Switzerland
Noriyuki Miura	2004	2013	Keio University	Yokohama	Japan
Masayuki Mizuno	1995	2013	NEC Corporation	Sagamihara	Japan
Thomas Morf	2005	2013	IBM	Rueschlikon	Switzerland
Ali Niknejad	2004	2013	University of California, Berkeley	Berkeley	CA/USA
Behzad Razavi	1992	2010	University of California, Los Angeles	Los Angeles	CA/USA
Martin Schmatz	2005	2013	IBM	Rueschlikon	Switzerland
Jae-Yoon Sim	2001	2013	Pohang University of Science & Technology	Pohang	South Korea
Takao Someya	2004	2013	University of Tokyo	Tokyo	Japan
Bang-Sup Song	1983	2013	University of California, San Diego	La Jolla	CA/USA
Robert Staszewski	1997	2013	Delft University of Technology	Delft	Netherlands
Michiel Steyaert	1988	2013	KU Leuven	Leuven	Belgium
David Su	1998	2013	Atheros Commun	San Jose	CA/USA
Francesco Svelto	1999	2013	University of Pavia	Pavia	Italy
Makoto Takamiya	2002	2013	University of Tokyo	Tokyo	Japan
Hirofumi Tamura	1988	2013	Fujitsu Laboratories	Kawasaki	Japan
Thomas Toifl	2005	2013	IBM	Rueschlikon	Switzerland
Joseph Tschanz	2002	2012	Intel	Hillsboro	OR/USA
Chris Van Hoof	2006	2013	IMEC	Leuven	Belgium
Geert Van der Plas	1999	2006	IMEC	Leuven	Belgium
Piet Wambacq	2000	2013	IMEC	Leuven	Belgium

TOP ISSCC PAPER CONTRIBUTORS 2004 - 2013





TOP ISSCC PAPER CONTRIBUTORS 1954 - 2013

ISSCC Authors with 20 or More Papers in the Past 60 Years as Compiled from IEEE Xplore

30 or more In Rank Order, Others Alphabetical

Author	Year of 1st Paper	Most Recent Paper	Affiliation	City	State/Country
Anantha Chandrakasan	1993	2013	Massachusetts Institute of Technology	Cambridge	MA/USA
James Meindl	1966	2010	Georgia Institute of Technology	Atlanta	Georgia/USA
Paul Gray	1970	2006	University of California, Berkeley	Berkeley	CA/USA
Takayasu Sakurai	1984	2013	University of Tokyo	Tokyo	Japan
Bram Nauta	1995	2013	University of Twente	Enschede	Netherlands
Tadahiro Kuroda	1992	2013	Kelo University	Yokohama	Japan
Asad Abidi	1984	2012	University of California, Los Angeles	Los Angeles	CA/USA
Bruce Wooley	1970	2013	Stanford University	Stanford	CA/USA
Kofi Makinwa	2002	2013	Delft University of Technology	Delft	Netherlands
Hoi-Jun Yoo	1995	2013	KAIST	Daejeon	South Korea
Mark Horowitz	1982	2011	Stanford University	Stanford	CA/USA
Michiel Steyaert	1988	2013	KU Leuven	Leuven	Belgium
David Blaauw	2002	2013	University of Michigan	Ann Arbor	MI/USA
Shekhar Borkar	1995	2012	Intel	Hillsboro	OR/USA
Robert Brodersen	1975	2007	University of California, Berkeley	Berkeley	CA/USA
Rinaldo Castello	1984	2013	University of Pavia	Pavia	Italy
Gyu-Hyeong Cho	1997	2013	KAIST	Daejeon	South Korea
Jan Craninckx	1995	2013	IMEC	Leuven	Belgium
Ali Hajimiri	1998	2013	California Institute of Technology	Pasadena	CA/USA
David Hodges	1963	1989	University of California, Berkeley	Berkeley	CA/USA
Qiuting Huang	1995	2010	ETH Zurich	Zurich	Switzerland
Johan Huijsing	1975	2013	Delft University of Technology	Delft	Netherlands
Eric Klumperink	2002	2013	University of Twente	Enschede	Netherlands
Masayuki Mizuno	1995	2013	NEC Corporation	Sagamihara	Japan
Behzad Razavi	1992	2011	University of California, Los Angeles	Los Angeles	CA/USA
Bang-Sup Song	1983	2013	University of California, San Diego	La Jolla	CA/USA
Dennis Sylvester	2000	2013	University of Michigan	Ann Arbor	MI/USA
Hirotsuka Tamura	1988	2013	Fujitsu Laboratories	Kawasaki	Japan

Survey Methodology

The data used to identify the ISSCC Top Contributors was compiled through queries directed to the IEEE Xplore digital library. Initial searches returned all identified ISSCC regular papers with the same author/co-author name along with paper title, first-author affiliation, year of publication, and digest pages. Normally, names appear in the data base as surname followed by the first initial. Unfortunately, on this basis, there are many individuals with the same name. Interestingly, this is especially the case for Asian-originated authors, particularly Japanese. To resolve this difficulty, the original papers of all identified authors were reviewed to determine the correct totals.

Special thanks goes to Makoto Ikeda of the University of Tokyo, for reviewing the integrity of the Japanese data. Thanks also go to Andrew Shorten, Dustin Dunwell, and Mario Milicevic, all of the University of Toronto, for performing all database queries and assembling the initial compilation of possible top contributors. This initial list and supporting data were reviewed by John Trnka, Chair of the ISSCC 60th Anniversary Committee, in detail to identify spurious entries. Unfortunately, because of the limitations of the database, and the need for manual compilation, errors may have been introduced that have resulted in some authors not being credited with all their ISSCC papers. This is especially possible for authors who have used multiple versions of their names over the years. In the tables resulting from this study, the listed affiliation is that of the most recent paper, or the most listed. Thus, ISSCC offers an apology to anyone who has been missed in the preparation of these tables. If you feel your name should have appeared, please contact ISSCC via email at isscc.trnka@charter.net to bring this fact to our attention. If possible, include a list of all publications with title, year, and all author names. ISSCC would also like to hear from authors that have other corrections to other aspects of the tables.

For all authors listed in the tables, author recognition certificates have been generated and partially distributed. Those authors (in bold) were recognized at ISSCC 2013 Plenary Session. If you did not receive your certificate, please contact Laura Fujino at lcfujino@aol.com, and provide your mailing address.

There were many authors not listed who have barely missed the cutoff of 10 papers in the past decade, or 20 papers over the 60 years. Clearly, ISSCC appreciates your contributions although this has not been acknowledged publicly. A special thanks to all ISSCC authors, those on the list and others, who have contributed to the continuing success of ISSCC over 60 years!

MEMORABLE PLENARY TALKS OF THE PAST DECADE



2003 Gordon Moore – Intel



2004 Nick Donofrio - IBM



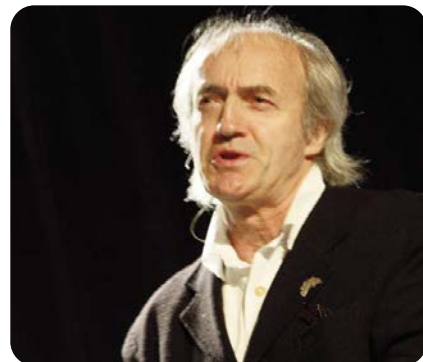
2005 Hugo De Man - IMEC



2006 Hermann Eul - Infineon



2007 Morris Chang - TSMC



2008 Bill Buxton – Microsoft Research



2009 John Cohn - IBM



2010 James Meindl
Georgia Institute of Technology



2011 Timothy Denison - Medtronic



2012 Eli Harari - SanDisk

COMMITTEE SIZE 1954-2013



Year	Location	Executive Committee	Program Committee	Topic Areas	Europe	Far East	Year	Location	Executive Committee	Program Committee	Topic Areas	Europe	Far East
1954	Univ of Pennsylvania	15	11	1			1984	SF Hilton	16	45	4	17	22
1955	Univ of Penn + Penn Sherwood Hotel	19	12	1			1985	NY Hilton	16	45	4	17	23
1956	Univ of Penn + Penn Sherwood Hotel	18	14	1			1986	Anaheim Hilton	17	42	4	17	24
1957	Univ of Penn + Bellevue Stratford Hotel	13	14	1			1987	NY Hilton	16	52	5	18	24
1958	Univ of Penn + Sheraton Hotel	13	12	1			1988	SF Hilton	17	52	5	19	26
1959	Univ of Penn + Sheraton Hotel	13	24	1			1989	NY Hilton	16	47	5	21	25
1960	Univ of Penn + Sheraton Hotel	19	22	1	2		1990	SF Hilton	16	44	5	21	20
1961	Univ of Penn + Sheraton Hotel	14	25	1	1		1991	SF Hilton	19	48	5	19	28
1962	Univ of Penn + Sheraton Hotel	24	21	1	1		1992	SF Hilton	19	51	6	19	28
1963	Univ of Penn + Sheraton Hotel	19	26	1	1		1993	SF Marriott	22	51	6	21	28
1964	Univ of Penn + Sheraton Hotel	19	33	1	1		1994	SF Marriott	23	57	7	21	29
1965	Univ of Penn + Sheraton Hotel	16	29	1	8		1995	SF Marriott	22	77	7	18	30
1966	Univ of Penn + Sheraton Hotel	16	30	1	6		1996	SF Marriott	22	82	7	18	34
1967	Univ of Penn + Sheraton Hotel	17	36	1	6		1997	SF Marriott	22	81	7	18	35
1968	Univ of Penn + Sheraton Hotel	17	42	4	9	2	1998	SF Marriott	21	88	7	17	35
1969	Univ of Penn + Sheraton Hotel	17	39	4	13	3	1999	SF Marriott	22	90	7	18	35
1970	Univ of Penn + Sheraton Hotel	17	42	4	10	6	2000	SF Marriott	24	96	7	22	36
1971	Univ of Penn + Sheraton Hotel	15	42	4	10	12	2001	SF Marriott	23	105	8	26	34
1972	Univ of Penn + Sheraton Hotel	16	44	4	11	19	2002	SF Marriott	24	113	8	31	36
1973	Phili Marriott Motor Hotel	16	41	4	13	22	2003	SF Marriott	28	114	8	33	40
1974	Phili Marriott Motor Hotel	16	41	4	12	19	2004	SF Marriott	29	112	8	33	51
1975	Phili Marriott Motor Hotel	16	46	4	15	19	2005	SF Marriott	30	146	8	36	46
1976	Phili Sheraton Hotel	18	47	4	17	21	2006	SF Marriott	30	171	9	39	55
1977	Phili Sheraton Hotel	16	40	4	20	21	2007	SF Marriott	28	181	10	43	56
1978	SF Hilton	16	41	4	19	22	2008	SF Marriott	27	183	10	48	59
1979	Phili Sheraton and Holiday Inn	15	48	4	12	21	2009	SF Marriott	27	185	10	49	52
1980	SF Hilton	14	43	4	14	21	2010	SF Marriott	22	162	11	47	53
1981	NY Grand Hyatt	14	41	4	13	22	2011	SF Marriott	21	162	10	46	51
1982	SF Hilton	16	40	4	17	22	2012	SF Marriott	20	160	10	44	50
1983	NY Sheraton Centre	15	45	4	16	25	2013	SF Marriott	18	163	10	47	54

- 1982 Added U of Penn and Bay Area reps
- 1992 Emerging Technologies added
- 2005 1st year of separate TD subcommittee
- 2007 Removed U of Penn and Bay Area reps



ISSCC 2011 Reunion of Current and Past Members of the Saratoga Group. The Saratoga Group is largely composed of volunteer graduate students from ECE, University of Toronto.



ISSCC 2008 Plenary-Speaker Luncheon in The View Lounge.



ISSCC 2011: Paul Gray motivating the audience at the Student Research Preview.



ISSCC 2008 Award winners receiving instructions from Laura Fujino before Plenary Session.



ISSCC 2008 Press Gallery in the Mission Tunnel.



ISSCC 2003: Top ISSCC Paper Contributors being recognized at the 50th Anniversary Plenary.

