2020

PRESS KIT

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The material presented here is preliminary.

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ISSCC 2020

VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

Table of Contents

Table of Contents 4
Preamble 7
FAQ on ISSCC 7
Overview: ISSCC 2020 – Integrated Circuits Powering the AI ERA 10
Plenary Session (Session 1) 10
Plenary Session — Invited Papers 12
Evening Events 15
Rising Stars 2020 15
Student Research Preview 15
Industry Showcase 15
Evening Panel: Quiz Show: “The Smartest Designer in the Universe” 17
Evening Panel: Is an Open-source Hardware Revolution on the Horizon? 17
Session Overviews and Highlights 18
Conditions of Publication 19
PREAMBLE 19
FOOTNOTE 19
Session 2 Overview: Processors 20
Session 2 Highlights: Processors 21
Session 3 Overview: Analog Techniques I 23
Session 3 Highlights: Analog Techniques I 24
Session 4 Overview: mm-Wave Wireless for Communication & Radar 25
Session 4 Highlights: mm-Wave Wireless for Communication & Radar 26
Session 5 Overview: Imagers and ToF Sensors 28
Session 5 Highlights: Imagers and ToF Sensors 29
Session 6 Overview: Ultra-High-Speed Wireline 31
Session 6 Highlights: Ultra-High-Speed Wireline 32
Session 7 Overview: High-Performance Machine Learning 34
Session 7 Highlights: High Performance Machine Learning 35
Session 8 Overview: Highlighted Chip Releases 36
Session 8 Highlights: Highlighted Chip Releases 38
Session 8 Highlights: Highlighted Chip Releases 39
Session 8 Highlights: Highlighted Chip Releases 40
Session 8 Highlights: Highlighted Chip Releases 41
Session 9 Overview: Noise-Shaping ADCs 42
Session 9 Highlights: Noise-Shaping ADCs 43

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Session 10 Overview: High Performance Transceivers 44
Session 10 Highlights: High Performance Transceivers 45
Session 11 Overview: DC-DC Converters 47
Session 11 Highlights: DC-DC Converters 48
Session 12 Overview: Advanced Optical Communication Circuits 49
Session 12 Highlights: Advanced Optical Communication Circuits 50
Session 13 Overview: Non-Volatile Memory 52
Session 13 Highlights: Non-Volatile Memories 53
Session 14 Overview: Low-Power Machine Learning 54
Session 14 Highlights: Low-Power Machine Learning 55
Session 15 Overview: SRAM and Compute-in-Memory 56
Session 15 Highlights: SRAM and Compute-In-Memory 57
Session 16 Overview: Nyquist and VCO-Based ADCs 58
Session 16 Highlights: Nyquist and VCO-Based ADCs 59
Session 17 Overview: Frequency Synthesizers and VCOs 60
Session 17 Highlights: Frequency Synthesizers and VCOs 61
Session 18 Overview: GaN and Isolated Power Conversion 62
Session 18 Highlights: GaN and Isolated Power Conversion 63
Session 19 Overview: Cryo-CMOS for Quantum Technologies 64
Session 19 Highlights: Cryo-CMOS for Quantum Technologies 65
Session 20 Overview: Low Power Circuits for IoT & Health 66
Session 20 Highlights: Low Power Circuits for IoT and Health 67
Session 21 Overview: Domain-Specific Processors 68
Session 21 Highlights: Domain-Specific Processors 69
Session 22 Overview: DRAM and High-Speed Interfaces 70
Session 22 Highlights: DRAM and High-Speed Interfaces 71
Session 23 Overview: Analog Techniques II 72
Session 23 Highlights: Analog Techniques II 73
Session 24 Overview: RF and mm-Wave Power Amplifiers 75
Session 24 Highlights: RF and mm-Wave Power Amplifiers 76
Session 25 Overview: Digital Power Delivery & Clocking Circuits 77
Session 25 Highlights: Digital Power Delivery & Clocking Circuits 78
Session 26 Overview: Biomedical Innovations 79
Session 26 Highlights: Biomedical Innovations 80
Session 27 Overview: IoT and Security 82
Session 27 Highlights: IoT and Security 83
Session 28 Overview: User Interaction and Diagnostic Technologies 84

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Session 28 Highlights: User Interaction and Diagnostic Technologies 85
Session 29 Overview: Emerging RF and THz Techniques 86
Session 29 Highlight: Emerging RF and THz Techniques 87
Session 30 Overview: Efficient Wireless Connectivity 88
Session 30 Highlights: Efficient Wireless Connectivity 89
Session 31 Overview: Digital Circuit Techniques for Emerging Applications 91
Session 31 Highlights: Digital Circuit Techniques for Emerging Applications 92
Session 32 Overview: Power Management Techniques 93
Session 32 Highlights: Power Management Techniques 94
Session 33 Overview: Non-Volatile Devices for Future Architectures 95
Session 33 Highlights: Non-Volatile Devices for Future Architectures 96
Session 34 Overview: Biomedical Sensing, Stimulation, and Harvesting 97
Session 34 Highlights: Biomedical Sensing, Stimulation, and Harvesting 98
Trends 99
Conditions of Publication 100
PREAMBLE 100
FOOTNOTE 100
Analog – 2020 Trends 102
Power Management – 2020 Trends 103
Data Converters – 2020 Trends 104
RF Subcommittee – 2020 Trends 108
Wireless – 2020 Trends 111
Wireline – 2020 Trends 113
Digital Architectures & Systems (DAS) – 2020 Trends 118
Digital Circuits – 2020 Trends 122
Machine Learning (ML) & AI – 2020 Trends 125
Memory – 2020 Trends 127
IMMD – 2020 Trends (Medical) 134
IMMD – 2020 Trends (Imagers) 135
Technology Directions – 2020 Trends 136
INDEX 137
Technical Topics Mapped to Papers 138
Selected Presenting Companies/Institution Mapped to Papers 138
Contact Information 145

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Preamble

FAQ on ISSCC

What is ISSCC?

ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US$468.8 billion in sales in 2018 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Who Attends ISSCC?

Attendance at ISSCC 2020 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%**.

Where is ISSCC?

The **67th ISSCC** will be held at the San Francisco Marriott Marquis on February 16th through February 20th 2020.

Are there Keynote Speakers?

After a day devoted to educational events, ISSCC 2020 begins formally on Monday, February 17, 2020 with four exciting plenary talks:

- Jeff Dean, Google Senior Fellow and SVP of Research, Mountain View, CA
- Kou-Hung Lawrence Loh, Senior Vice President & Corporate Strategy Officer, MediaTek Inc., Hsinchu, Taiwan
- Nadine Collaert, Program director, imec, Leuven, Belgium
- Dario Gil, Director of IBM Research, IBM Thomas J. Watson Research Center, Yorktown Heights, NY

What is the Technical Coverage at ISSCC?

ISSCC covers a full spectrum of design approaches in advanced technical areas broadly categorized as: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovations including micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking developments that may take three or more years for commercialization.

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How are ISSCC Papers Selected?

Currently around 600 submissions are received each year across the broad spectrum of specified topics. Review is by a team of over 150 scientific and industry experts from the Far-East, Europe, and North America. These experts are organized into 12 Sub-Committees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline Subcommittees
- **Analog Systems** includes Analog, Power Management, and Data Converter Subcommittees
- **Digital Systems** includes Memory, Digital Circuits, Digital Architectures and Systems, and Machine Leaning and AI Subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees

What Companies are Presenting this year?

Companies presenting papers at ISSCC 2020 include Analog Devices, AMD, Hitachi, IBM, Intel, MediaTek, NXP Semiconductors, Panasonic, Qualcomm, Renesas, Samsung, Sony, Texas Instruments, TSMC, Toshiba, and Xilinx, just to name a few. A more complete list can be found in the Index.

Are there educational sessions?

ISSCC features a variety of educational events which include:

- Ten Tutorials (targeted toward participants looking to broaden their horizon)
- Six Forums (targeted toward experts in an information sharing context)
- One Short Course (targeted toward in-depth appreciation of a current hot topic)

Are There Other Events?

A more complete list of all activities at ISSCC 2020:

- Four Plenary Presentations
- Four Invited Industry Talks on Highlighted Chip Releases
- Technical Sessions (34 distinct sessions)
- Five Evening Events and Panels, including:
  - Two Evening Panels
  - Industry Showcase
  - Rising Stars 2020
  - Student Research Preview (for the introduction of graduate-student research-in-progress)
- Educational Sessions Featuring:
  - Ten Tutorials
  - Six Forums
  - One Short Course
- Demonstration Sessions from Academia and Industry
- Networking Social Events
- Author Interview Sessions

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- A Number of University Alumni Events
- Book Display

How Do I Use this Press Kit?

The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes SESSION OVERVIEWS AND HIGHLIGHTS of all 34 technical sessions into which the 197 papers are grouped, together with brief descriptions and context for each. As well, there is an abstract for each of the Plenary talks. For your convenience, the Kit includes two structural charts in the INDEX section: (a) a list of the 4 Technical Topics and their associated Subcommittees and Sessions; (b) a list of contributing companies and institutions with their associated papers. Thus, to located information of interest you can access Chart 4.1 to identify sessions of interest, after which you might logically access its Session's Overview or Highlight section. Alternatively, if your interest is in particular organization then Chart 4.1 will direct you immediately to papers of interest each of which is detailed in its corresponding Session Overview and possibly in the Highlights section. For anyone's interest it is useful to use Chart 4.1 to access the appropriate Trend information which provides a broad historical view of the context of your interest and often includes reference to current ISSCC 2020 papers.

Anything New This Year?

ISSCC will hold an invited Industry Track (Session 8) which will highlight recent hot-product releases from Intel, Xilinx, ARM and AMD and discuss innovative ways they solved product-level challenges.

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Overview: ISSCC 2020 – Integrated Circuits Powering the AI ERA

The steady advancement of solid-state circuits has led to technological betterment in our daily living, demonstrated by exploding applications ranging from medical, wearable and mobile electronics to IoT, virtual reality, autonomous driving and robotics. While the widespread excitement resides in the applications where end-users touch and feel, the systems are enabled by integrated circuits engines that are woven into this technological fabric of our lives. Galvanized by this reality, the solid-state circuits community is driven to enhance the platform that continues to evolve. With much enthusiasm and anticipation, and even uncertainty, we look onward to this emerging AI era.

Plenary Session (Session 1)

The Plenary Session on the morning of Monday, February 17, 2020, will feature four renowned speakers:

- Jeff Dean, Google Senior Fellow and SVP of Research, Mountain View, CA will discuss "The Deep Learning Revolution and Its Implications for Computer Architecture and Chip Design", highlighting recent advances in deep learning and also discussing ways that machine learning may be able to help with aspects of the circuit design process.
- Kou-Hung Lawrence Loh, Senior Vice President & Corporate Strategy Officer, MediaTek Inc., Hsinchu, Taiwan, will give his insights into "Fertilizing AIoT from Roots to Leaves", and will explain the challenges and opportunities for our industry going forward to meet the vision of over 350 billion connected intelligent devices in 2030.
- Nadine Collaert, Program director, imec, Leuven, Belgium, will describe "Future Scaling: Where Systems and Technology Meet" and will explain why a rethinking of what the semiconductor industry calls scaling is needed, including a push to technology diversification and blending of different technologies together to achieve benefits at the system level.
- Dario Gil, Director of IBM Research, IBM Thomas J. Watson Research Center, Yorktown Heights, NY will discuss "The Future of Computing: Bits + Neurons + Qubits", and how this future will enable the next generation of intelligent mission critical systems and accelerate the rate of science-driven discovery.

Highlights of these Plenary talks are provided in the following section.

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PLENARY SESSION – INVITED PAPERS

Plenary Session — Invited Papers

Chair: ***Jan Van der Spiegel,*** University of Pennsylvania, PA

ISSCC Conference Chair

Associate Chair: ***Un-Ku Moon*****,** Oregon State University, Corvallis OR

ISSCC International Technical-Program Chair

1.1 The Deep Learning Revolution and Its Implication for Computer Architecture and Chip Design

Jeff Dean**,** *Google Senior Fellow and SVP of Research, Mountain View, CA*

The past decade has seen a remarkable series of advances in machine learning, and in particular deep learning approaches based on artificial neural networks, to improve our abilities to build more accurate systems across a broad range of areas, including computer vision, speech recognition, language translation, and natural language understanding tasks. In this talk, I will highlight some of these advances, and their implications on the kinds of computational devices we need to build, especially in an era where general purpose computers are no longer improving their performance significantly year-over-year. I'll also discuss some of the ways that machine learning may also be able to help with some aspects of the circuit design process. Finally, I'll provide a sketch of at least one interesting direction towards much larger-scale multi-task models that are sparsely activated and employ much more dynamic, example- and task-based routing than the machine learning models of today.

1.2 Fertilizing AIoT from Roots to Leaves

Kou-Hung Lawrence Loh**,** *Senior Vice President & Corporate Strategy Officer, MediaTek Inc., Hsinchu, Taiwan*

Artificial intelligence (AI) creates new opportunities for all kinds of “things” to interface with the world in unprecedented ways. As IC technology advances, AI has evolved from traditional expert systems toward cognitive intelligence, which involves multidimensional perception, self-learning, decision-making, and interaction. Enabling cognitive AI in everything (AIoT) demands comprehensive circuit technologies to enhance the performance, power dissipation, and form factor of edge devices as well as cloud infrastructure, which forms the roots to support a variety of leaf-applications. The root-technologies cover a very broad range, including heterogeneous computing, 5G wireless communication, high-speed wireline communication, human-machine interfaces, and advanced packages. These fundamental technologies can be grouped into three trunks that support intelligent applications spanning across mobile devices, smart home, automotive platform, and smart city. In this talk, the advancement of these root technologies allowing the transition from conventional ICs to AIoT will be discussed. Technical innovations for edge AI SoC and communication technologies to enable cloud-edge collaboration will be explored. To reach the vision of over 350 billion connected intelligent devices in 2030, the challenges and opportunities for our industry going forward will be summarized.

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1.3 Future Scaling: Where Systems and Technology Meet

Nadine Collaert, *Program director, imec, Leuven, Belgium*

In a smart society where everything will be connected, an avalanche of data is coming toward us, with numbers going to several hundreds of zettabytes per year by 2025. This data will need to be sent around, stored, computed and analyzed. At the heart of it all will be innovations at the technology and system level. With Moore's law under pressure, a rethinking of what the semiconductor industry calls scaling will be needed.

In this work, we will show the strong push to technology diversification, blending different technologies together to achieve benefits at the system level. This brings the interaction of technology and design to the next level: System-Technology co-optimization (STCO), with 3D technologies taking a central stage. Furthermore, the growing demand for storage will put an increasing pressure on the memory hierarchy where emerging concepts like MRAM, FeFET.... have the potential to bring new speed and capacity benefits. Next to that, memories like e.g. RRAM are getting a lot of traction for analog in-memory computing to enable energy efficient machine learning at the IoT edge. Finally, we will also briefly review the status of quantum computing, these days gaining a lot of interest as a path to ultra-powerful computing.

1.4 The Future of Computing: Bits + Neurons + Qubits

Dario Gil*, Director of IBM Research, IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

The laptops, cell phones, and internet applications commonplace in our daily lives are all rooted in the idea of zeros and ones – in bits.

This foundational element originated from the combination of mathematics and Claude Shannon's Theory of Information. Coupled with the 50-year legacy of Moore's law, the bit has propelled the digitization of our world.

In recent years, artificial intelligence systems, merging neuron-inspired biology with information, have achieved superhuman accuracy in a range of narrow classification tasks by learning from labelled data. Advancing from narrow AI to broad AI will encompass the unification of learning and reasoning through neuro-symbolic systems, resulting in a form of AI which will perform multiple tasks, operate across multiple domains, and learn from small quantities of multi-modal input data.

Finally, the union of physics and information led to the emergence of Quantum Information Theory and the development of the quantum bit - the qubit - forming the basis of quantum computers. We have built the first programmable quantum computers, and although the technology is still in its early days, these systems offer the potential to solve problems which even the most powerful classical computers cannot.

The future of computing will look fundamentally different that it has in the past. It will not be based on more and cheaper bits alone, but rather, it will be built upon bits + neurons + qubits. This future will enable the next generation of intelligent mission critical systems and accelerate the rate of science-driven discovery.

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EVENING EVENTS

Evening Events

ISSCC 2020 will continue the popular tradition of evening panels and evening sessions, where experts, often of opposing views, discuss topics which range from the lighthearted to the controversial (but always informative and entertaining!). This year's panels are "Quiz Show: The Smartest Designer in the Universe and "Open-Source Hardware Revolution".

In addition, ISSCC 2020 will include additional evening events including a Rising Stars 2020, an Industry Showcase and a Student Research Preview.

Rising Stars 2020

Sunday, February 16

Rising Stars 2020 is an educational workshop for graduate and undergraduate students, and young professionals who have graduated within the last two years who are interested in learning how to excel at academic and industry careers in computer science, computer and electrical engineering. "Rising to the Top in Industry" career panel will touch upon topics such as mentoring, setting career goals, filing patents, management vs. technical tracks, and more. "Navigating the Assistant Professorship" will address applying for a faculty position, tenure review, and managing day-to-day life in academia. This event is open to the public and all are welcome to join.

Student Research Preview

Sunday, February 16

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 90 second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research.

The Student Research Preview will include the talk "The Lessons of History: Sometimes it's the very people who no one can imagine anything of who do the things no one can imagine" by Tadahiro Kuroda, Professor University of Tokyo.

Industry Showcase

Monday, February 17

ISSCC will hold a plenary Industry Showcase event on the evening of Monday, February 17th, which will highlight how advances in silicon circuits, SoCs and systems are fueling the most innovative industrial applications and products of the future. Following the recognized role of ISSCC as the foremost global forum for advances in solid-state circuits and systems-on-chip (SoCs), the goal of this event will be to highlight the role of silicon in the creation of novel products. It will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation. The featured presentations were chosen through a nomination and voting process by members of the Industry Showcase Committee and represent an exciting introduction to the next generation of applications and products enabled by the sustained evolution of solid-state integrated circuits.

Participant	Title	Highlight
Intel, Portland, OR	Lakefield: Hybrid Computing with 3D silicon integration	Intel will showcase Lakefield with Hybrid computing and Three-Dimensional Stacking to enable the industry's first mobility PC product in a 12x12 (mm^2) Package on Package (POP) form factor.
Wiliot, Caesarea, Israel	Low cost sensor tags for IoT, using sticker-format Bluetooth Low Energy, powered from ambient radio	This showcase demonstrates fully passive Bluetooth SoCs to enable low cost auto-ID tags that can harvest RF energy from Bluetooth Low Energy beacons. The demonstration shows the devices being utilized in a sticker format on wine bottles in a merchandizing application.
IBM Systems and Technology, Poughkeepsie, NY	IBM z15: A 12 Core 5.2GHZ Microprocessor	This showcase demonstrates IBM's z15's microprocessor (CP) and system control chips (SC) built in a 14nm technology with significant improvements in cache density and system performance.

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Butterfly Network, Inc., Guilford, CT	Butterfly iQ: Handheld Whole-Body Imager with Ultrasound-on-Chip	This demonstrates Butterfly iQ, the first FDA cleared and CE approved, "one probe, whole body imaging" medical ultrasound device, that directly plugs into a smart phone, and at a 50-fold lower price tag than existing solutions. The showcase will include the product live scanning on human bodies.
Weebit Nano, Hod HaSharon, Israel	Spiking Neural Network using ReRAM	Weebit-Nano showcases 3rd generation neuromorphic computing implemented using analog neurons and resistive synapses based Spiking Neural Networks is shown in a live demonstration.
Samsung Semiconductor, Hwaseong-si, Korea	Motion-resilient VGA Time-of-Flight Image Sensor	Samsung demonstrates its 2nd generation Time-of-Flight based image sensor using their 4-tap 7µm global-shutter ToF pixel technology that is currently in mass production.
Samsung Electronics, Bengaluru, India	A 1/1.33-inch 108MP CMOS Image Sensor with 0.8µm Unit Pixels	Samsung exhibits a 108MP CMOS image sensor that they believe is the world's first commercial 108MP image sensor for mobile phones with resolution comparable to high-end DSLR cameras.
Samsung Electronics, Hwaseong-si, Korea	A Blocker-Tolerant Direct Sampling Receiver for Wireless Multi-Channel Communication	In this showcase, Samsung will demonstrate, using a live FM radio reception, a blocker-tolerant direct sampling receiver that includes a current re-use LNA and a digital-assisted ADC designed for a wireless FM mobile radio system.
Ferric, New York, NY	Fully Programmable Power Converter Chiplet using Ferric Integrated Inductors	Power delivery requirements for advanced processors, FPGAs, and ASICs present challenges for maximizing system performance. Ferric will be showcasing its Fe1202 product, that it believes is the first single-chip buck converter with fully integrated ferromagnetic inductors and powertrain that achieves a current density exceeding 2A/mm^2.
Texas Instruments, Bengaluru, India	Camera Based Perception and 3D Surround View for Autonomous Valet Parking on a 16nm Automotive SoC	Texas Instruments demonstrates the key algorithmic elements needed to enable autonomous parking using surround camera perception using a single high performance, cost and power efficient 16nm SoC. Both camera perception and 3D surround view are demonstrated live on the SoC.
Advanced Micro Devices, Santa Clara, CA	AMD Radeon RX5700 graphics power and performance demonstration	AMD will demonstrate key AMD Navi technologies showcasing real-world benefits of PCIe Gen 4 speeds, overclocking capabilities, power efficiency for gaming, and CPU and GPU cooperative power management in a mobile form-factor.
Western Digital Research, Milpitas, CA	A Vehicle Security Surveillance based on Artificial Intelligence of Things (AIoT)	Western Digital Research showcases a parking mode security surveillance system that deters and records vehicle break-ins leveraging the state of art in internet of things and artificial intelligence technology.
MediaTek, Hsinchu Taiwan	A Dual Core Deep Learning Accelerator for Versatile AI Applications in a 7nm 5G Smartphone SoC	Mediatek will demonstrate running an AI-based video super-resolution application on the deep learning accelerator in its 5G smartphone SoC. The demonstration will showcase the performance and power efficiency of its accelerator solution.
Alibaba Group, Sunnyvale, California	Hanguang 800, a High Throughput AI Inference Chip	Alibaba will showcase a live demonstration of its newly announced Hanguang 800, a cloud inference chip built on 12nm, to be soon deployed to their data centers to accelerate AI applications such as smart city, image-based search and medical image processing.

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Evening Panel: Quiz Show: “The Smartest Designer in the Universe”

Tuesday, February 18

Good silicon engineering is like practicing sports on an Olympic scale. Be the best and be known being the best. But who is actually the smartest designer in the universe? Who is capable of combining endless creativity with superb knowledge and insight? And where will we find this person: in industry or in academia? Or will the students rise up and show the former generation their tail?

In this interactive quiz show, three teams representing industry, academia and students will compete for the honor and the prestigious title: "The Smartest Designer in the Universe". In several rounds, the contestants will solve questions and puzzles covering all parts of electrical engineering.

They will baffle you with their knowledge, surprise you with their wit and entertain you with their to the point remarks. This all topped with a gentle sauce of made of irony, since the smartest designer in the universe should be smart enough to appreciate the special relativity of it all.

Join this session not only to support your own team but enroll in the game. Everybody will be able to actively participate using an app. Show your strength and support your team!

Evening Panel: Is an Open-source Hardware Revolution on the Horizon?

Tuesday, February 18

Open-source has revolutionized software, fostering innovation and enhancing productivity. Hardware design is complex in distinct ways, which, on the one hand, make such progression necessary, but, on the other hand, institute completely new challenges. Are the challenges show stoppers, or just new ways of thinking and engineering? If open-source hardware could be attained, what would it look like, and would there be significant up-side (e.g., compared to today’s IP licensing)? Whatever the answers, the success of open-source hardware will require alignment, partnership, and collective will across the hardware ecosystem, from design, to methodologies, to business models. This evening session brings together panelists representing and debating from these different perspectives, to make and break the case.

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ISSCC 2020

SESSION OVERVIEWS AND HIGHLIGHTS

Conditions of Publication

PREAMBLE

The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2020 in February in San Francisco

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You are welcome to use this material, copyright- and royalty-free, with the following understanding:

- That you will maintain at least one reference to ISSCC 2020 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.
- That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 67th appearance of ISSCC, on February 16th to February 20th, 2020, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2020, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 16 - February 20, 2020,

at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: Processors

Digital Architectures and Systems Subcommittee

Session Chair: Christopher Gonzalez, IBM, Yorktown Heights, NY

Session Co-Chair: Thomas Burd, Advanced Micro Devices, Santa Clara, CA

Processors continue to provide higher performance, integrating more cores using the latest process technology, as well as advanced chiplet stacking technology, enabling a wide range of performance targets with economic solutions. The first paper describes a high-performance CPU, followed by papers on chiplet-stacking technology. The latest fully integrated smartphone SoCs come next, followed by a highly integrated ASIL-D automotive SoC. The final paper presents a state-of-the-art high-performance processor for mainframe computers.

- In Paper 2.1, AMD unveils the “Zen 2” core, which is an energy-efficient high-performance x86-64 microprocessor core fabricated in a 7nm FinFET process technology, integrating 475M transistors into 1 Core Slice with a private 0.5MB L2 cache and 4MB of shared L3 cache.
- In Paper 2.2, AMD presents a chiplet architecture using hybrid process technology of 7nm and 12nm ranging from a top-end server with 38.74B transistors (64 cores @ 2W/core), to desktop processors achieving 4.7GHz.
- In Paper 2.3, CEA-LETI-MINATECH demonstrates a chiplet-based manycore architecture composed of 96 cores in 6 chiplets 3D-stacked on an active interposer delivering 220GOPS performance.
- In Paper 2.4, Samsung introduces a 7nm AP SoC for smartphones powered with tri-cluster CPUs and a sparsity-aware NPU for improved energy efficiency, as well as a hardware auto-clock-gating feature.
- In Paper 2.5, MediaTek presents a 7nm AP SoC with a dual-gear octa-core CPU subsystem for a fully integrated 5G smartphone, incorporating advanced droop techniques and a novel approach to CPU clocking.
- In Paper 2.6, Texas Instruments announces an automotive SoC integrating 3.5B transistors implemented in 16nm process technology, supporting 14TOPS in 2-to-10W with an integrated safety MCU, 512b-vector DSP and embedded vision and imaging acceleration.
- In Paper 2.7, IBM introduces the z15 microprocessor, integrating 12 cores running at 5.2GHz, and a system-control chip, both using 14nm technology. Core count is increased by 20% and cache capacity significantly enlarged.

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Session 2 Highlights: Processors

[2.1] Zen 2: The AMD 7nm Energy-Efficient High-Performance x86-64 Microprocessor Core

[2.3] A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm² Inter-Chiplet Interconnects and 156mW/mm² @ 82%-Peak-Efficiency DC-DC Converters

[2.4] A 7nm High-Performance and Energy-Efficient Mobile Application Processor with Tri-Cluster CPUs and a Sparsity-Aware NPU

Paper 2.1 Authors: Teja Singh[1], Sundar Rangarajan[1], Deepesh John[1], Russell Schreiber[1], Spence Oliver[1], Rajit Seahra[2], Alex Schaeferr[1]

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Paper 2.4 Authors: Youngduk Kim, Wookyeong Jeong, Lakkyung Jung, Dongsuk Shin, Jae Geun Song, Jinook Song, Hyeokman Kwon, Yoonjoo Kwon , Nak HeeSeong, Taejin Kim

Paper 2.4 Affiliation: Samsung Electronics, Gyeonggi-do, Korea

Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA

CONTEXT AND STATE OF THE ART

- Next-generation 7nm microprocessor cores push the performance and power efficiency envelope across the entire microprocessor space, ranging from high-end servers, to desktop products, to mobile devices.
- As Moore's Law slows down and advanced CMOS process nodes become more challenging to manufacture and yield, new packaging techniques are required to continue on the historical density improvement trends.

TECHNICAL HIGHLIGHTS

- AMD introduces their industry-leading "Zen 2" core complex manufactured in TSMC 7nm with 0.5MB L2 and 4MB of shared L3 cache per core.
- A collaboration led by CEA-LETI-MINATEC demonstrates a 220GOPS 96-core processor using a 28nm FDSOI 3D-stack active interposer with 20μm-pitch micro-bumps.
- Samsung showcases their next-generation 7nm moble application processor featuring three power-performance-optimized core strengths and a sparsity-aware neural processing unit.

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APPLICATIONS AND ECONOMIC IMPACT

- AMD's "Zen 2" core complex will be the cornerstone for the next wave of CPU products ranging from high-end servers to industry-leading desktop products.
- Active interposer technology offers a promising technique to continue the ever-expanding pursuit of increased SoC integration, raising yields by permitting smaller dies to be composed into larger systems.
- Next-generation mobile application processors will continue to expand functionality in smartphone devices, while increased energy efficiency will enable a longer battery life for an overall better user experience.

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Session 3 Overview: Analog Techniques I

Analog Subcommittee

Session Chair: Youngcheol Chae, Yonsei University, South Korea

Session Co-Chair: Michael Perrott, Texas Instruments, NH

Subcommittee Chair: Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

Analog techniques continue to improve and diversify in order to address an ever-wider range of applications. New technologies are being utilized, including co-packaged BAW resonators to achieve better than 30ppm frequency stability from -40ºC to 85ºC and the first GaN voltage reference offers very wide temperature range operation (-50ºC to 200ºC). Frequency references maintain accuracy while reducing power consumption and area. The performance of temperature sensors continues to improve, with BJT-based sensors achieving significantly higher energy efficiency (resolution FoM), and resistor-based temperature sensors achieving higher accuracy.

- In Paper 3.1, TI presents a CMOS frequency reference, in which a co-packaged BAW resonator, a low-power dynamic divider, a temperature sensor and a digital PLL are combined to achieve ±30ppm frequency stability from -40ºC to 85ºC.
- In Paper 3.2, the University of Illinois at Urbana Champaign presents a compact RC-based temperature sensor that achieves a min-max inaccuracy of ±0.72ºC from -30ºC to 90ºC with 1-point trim and a resolution FoM of 92fJ·K^2.
- In Paper 3.3, the University of Michigan introduces a periodically pulsed 32kHz crystal oscillator (XO) with an Allan deviation of 2ppb and a power dissipation of 0.51nW, some 5× lower than the state-of-the-art.
- In Paper 3.4, TU Delft presents a 16MHz frequency reference, which achieves ±400ppm inaccuracy from -45ºC to 85ºC after a 2-point trim and a linear temperature compensation scheme.
- In Paper 3.5, the University of Illinois at Urbana Champaign (UIUC) introduces an FLL-based 32MHz frequency reference, which achieves an inaccuracy of ±530ppm from -40ºC to 85ºC after a 2-point trim.
- In Paper 3.6, TU Delft describes a Wheatstone-bridge temperature sensor that achieves 0.4ºC (3σ) inaccuracy from −55ºC to 125ºC after a 1-point trim, and a resolution FoM of 10fJ·K^2, which corresponds to state-of-the-art energy efficiency.
- In Paper 3.7, SiTime presents a BJT-based temperature-to-digital converter (TDC). Intended for the temperature compensation of a MEMS frequency reference, it achieves a resolution FoM of 190fJ·K^2.
- In Paper 3.8, National Chiao Tung University presents a voltage reference in a GaN-on-Si process. Intended for automotive applications, it has a very wide operating temperature range (-50ºC to 200ºC).

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Session 3 Highlights: Analog Techniques I

[3.1] An Integrated BAW Oscillator with <±30ppm Frequency Stability Over Temperature, Package Stress, and Aging Suitable for High-Volume Production

Paper 3.1 Authors: Danielle Griffith[1], Ernest Yen[2], Kaichien Tsai[1], Habeeb Mohammed[1], Baher Haroun[1], Ali Kiaei[2], Ahmad Bahai[2]

Paper 3.1 Affiliation: [1]Texas Instruments, Dallas TX ; [2] Texas Instruments, Santa Clara CA

Subcommittee Chair: Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

CONTEXT AND STATE OF THE ART

- Radio applications typically require a costly crystal–based oscillator as a frequency reference to provide frequency stability. Lower-cost co-packaged Bulk-Acoustic-Wave oscillators have not been suitable to replace the crystals in the past.

TECHNICAL HIGHLIGHTS

- **Texas Instruments introduces an Integrated BAW Oscillator with <±30ppm Frequency Stability over Temperature, Package Stress, and Aging Suitable for High-Volume Production**
    - A 2.5GHz BAW oscillator is integrated with a radio-chip-in-package to realize crystal-less operation.
    - Overall stability of <+/-30 ppm is demonstrated with active compensation including all environmental impacts.
    - This work meets power and cost requirements and is suitable for mass production.

APPLICATIONS AND ECONOMIC IMPACT

- The co-packaged BAW 2.5GHz oscillator enables low-cost and low-power crystal-less radio applications.

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Session 4 Overview: mm-Wave Wireless for Communication & Radar

Wireless Subcommittee

Session Chair: Matteo Bassi, Infineon Technologies AG, Villach, Austria

Session Co-Chair: Vito Giannini, Uhnder Inc., Austin TX

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR

Mm-wave wireless communication and radar systems are key drivers for cutting-edge integrated circuit design advancements. The session features papers describing state-of-the-art mm-wave transceivers, antenna-RX co-integration, multiplexed MIMO RX arrays, MIMO systems, spatial-modulated secure directional transmitters, and FMCW radars with 100GHz bandwidth.

- In Paper 4.1, Samsung Electronics presents a 5G NR solution including a 39GHz 16-channel RF phased-array transceiver IC in 28nm bulk CMOS and a dual-stream IF transceiver IC in 65nm bulk CMOS.
- In Paper 4.2, Georgia Institute of Technology and Rice University present an E-band high-linearity antenna-LNA front-end achieving 4.8dB NF and 2.2dBm IIP3. It exploits on-antenna noise canceling and a gm-boosting scheme. Over-the-air modulation testing demonstrates its capability to support >10Gb/s high-order QAM signals.
- In Paper 4.3, Oregon State University and Columbia University demonstrate a novel harmonic-mixing-based beam-space RX architecture that achieves both spatial filtering and frequency-domain multiplexing with a single IF interface. The four-element 28GHz RX array consumes <30mW per-stream/per-element. An OTA wireless MIMO test shows concurrent reception of two 400Mb/s streams.
- In Paper 4.4, Carnegie Mellon University introduces a multi-layer hybrid/digital architecture enabling efficient scaling of MIMO streams and demonstrating full-duplex (FD) multi-antenna communication.
- In Paper 4.5, Intel enables both high throughput and spectral reuse with a 4-element 60GHz phased-array RX with dual-polarization MIMO data rates up to 64Gb/s. It demonstrates measurements of in-band spatial interferer tolerance at 60GHz for dense multi-user connectivity.
- In Paper 4.6, Princeton University describes a scalable spatio-temporal modulated mm-wave TX array for physically secure directional wireless links across 71 to 76 GHz.
- In Paper 4.7, Hong Kong University of Science and Technology, Tehran University of Technology and the University of California at Berkeley present a single-antenna FMCW W-band CMOS radar TRX that uses an adaptive feedback leakage cancellation technique to mitigate TX leakage.
- In Paper 4.8, Massachusetts Institute of Technology and Universidad Politécnica de Madrid present a frequency-comb-based scalable FMCW radar architecture to achieve state-of-the-art cumulative chirp bandwidth of 100GHz. Implemented in 65nm CMOS, the TRX radar chip prototype demonstrates seamless coverage of the entire 220-to-320GHz band.

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Session 4 Highlights: mm-Wave Wireless for Communication & Radar

[4.1] A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications

[4.2] An E-Band High-Linearity Antenna-LNA Front-End with 4.8dB NF and 2.2dBm IIP3 Exploiting Multi-Feed On-Antenna Noise-Canceling and G_m-Boosting

[4.8] A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth

Paper 4.1 Authors: Hyun-Chul Park, Daehyun Kang, Sang Min Lee, Byungjoon Park, Kihyun Kim, Jooseok Lee, Yuuichi Aoki, Youngchang Yoon, Sangho Lee, Donghyun Lee, Daehoon Kwon, Seokhyeon Kim, Jihoon Kim, Woojae Lee, Chunsuk Kim, Sangyong Park, Jaehong Park, Bohee Suh, Jaesik Jang, Meeran Kim, Donggyu Minn, Inhyeok Park, Sunryoul Kim, Kihong Min, Jeeho Park, Sehyug Jeon, An-Sang Ryu, Yunsung Cho, Jaehyup Kim, Kyu, Hwan An, Yonghoon Kim, Jeong Ho Lee, Juho Son, Sung-Gi Yang

Paper 4.1 Affiliation: Samsung Electronics, Suwon, Korea

Paper 4.2 Authors: Sensen Li[1], Taiyun Chi[2], Doohwan Jung[1], Tzu-Yuan Huang[1], Min-Yu Huang[1], Hua Wang[1]

Paper 4.2 Affiliation: [1]Georgia Institute of Technology, Atlanta, GA; [2]Rice University, Atlanta, GA

Paper 4.8 Authors: Xiang Yi[1], Cheng Wang[1], Muting Lu[1], Jinchen Wang[1], Jesus Grajal[1,2], Ruonan Han[1]

Paper 4.8 Affiliation: [1]Massachusetts Institute of Technology, Cambridge, MA; [2]Universidad Politécnica de Madrid, Madrid, Spain

Subcommittee Chair: Stefano Pellerano, Intel Corporation, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- Increasing demands on high data-rate and low latency cellular communications are accelerating the developments of millimeter-wave systems for 5G NR in the 28 and 39GHz bands.
- Merging antenna with front-end circuits creates a new design paradigm to advance front-end innovations and performance beyond electronics-only designs.
- The increasing demands for low-cost, compact, and high-resolution radar systems have driven the operation frequency to terahertz (THz) due to the shorter wavelength and larger available bandwidth.

TECHNICAL HIGHLIGHTS

- **The world's first commercial 39GHz-band CMOS RF phased-array transceiver IC for 5G NR base-station**
  - Samsung Electronics presents a 5G NR solution including a 39GHz 16-channel RF phased-array transceiver IC in 28nm bulk CMOS and a dual-stream IF transceiver IC in 65nm bulk CMOS.
- **E-band Antenna/RX front-end co-design achieves 16.5Gb/s 64QAM in over-the-air modulation tests**
  - Georgia Institute of Technology and Rice University present an E-band high-linearity antenna-LNA front-end achieving 4.8dB NF and 2.2dBm IIP3. It exploits on-antenna noise canceling and a gm-boosting scheme. Over-the-air modulation testing demonstrates its capability to support >10Gb/s high-order QAM signals.
- **THz radar architecture breaks bandwidth limitations to achieve millimeter-range resolution sensing**
  - Massachusetts Institute of Technology and Universidad Politécnica de Madrid present a frequency-comb-based scalable FMCW radar architecture to achieve state-of-the-art cumulative chirp bandwidth of 100GHz. Implemented in 65nm CMOS, the TRX radar chip prototype demonstrates seamless coverage of the entire 220-to-320GHz band.

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APPLICATIONS AND ECONOMIC IMPACT

- Low-cost and high-performance RF chipset solutions enable the effective deployment of 5G communication systems worldwide.
- Due to compact on-chip mm-wave antennas and intimate interfaces with electronics, Antenna/Front-End co-design is critical for applications such as 5G-and-beyond communication and radar sensing.
- High-accuracy radar scenarios include industrial robotics and small defect detections, and require tradeoffs between bandwidth and detection range.

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Session 5 Overview: Imagers and ToF Sensors

Imagers, Medical, MEMS and Displays Subcommittee

Session Chair: Seong-Jin Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea

Session Co-Chair: Hayato Wakabayashi, Sony Semiconductor Solutions Corporation, Kanagawa, Japan

The session opens with two LiDAR papers, first a 40-channel, 225m max-distance, 240×192 resolution LiDAR SoC, followed by a 1M pixel, VAPD-based LiDAR system capable of 10cm resolution. A 500MHz demodulation, indirect time-of-flight iTOF sensor based on Ge-on-Si is then presented after which a QVGA iTOF sensor featuring motion artifact suppression and background light cancelation is described. Rolling and global shutter pixel scaling continues with the presentation of a 2.3μm, 1Mpixel voltage-domain global shutter sensor followed by an 44Mpixel CMOS image sensor with 0.7μm pixel pitch. A 132dB dynamic range, single exposure sensor is then described followed by a 1.45μm pixel, BSI sensor featuring an in-pixel differential amplifier for improved read noise. The session ends with two event-driven vision sensors, the first presenting a multi-mode sensor capable of motion and saliency detection, followed by a 3D-stacked, 4.86μm event-based sensor.

- In Paper 5.1, Toshiba describes a 240×192 pixel automotive LiDAR SoC capable of 225m maximum range distance at 10fps, while operating at up to 70klux ambient light based on 40-channel voltage/time dual-data-converter-based AFE.
- In Paper 5.2, Panasonic presents a 1200×900 VAPD-based time-of-flight system capable of both direct and indirect ranging up to a maximum range distance of 250m with a 10cm minimum resolution.
- In Paper 5.3, Artilux presents an indirect time-of-flight range sensor based on a Ge-on-Si platform capable of 500MHz demodulation frequency, while offering sensitivity at wavelengths up to 1400nm.
- In Paper 5.4, Sungkyunkwan University presents a QVGA iTOF CMOS sensor. Based on a pseudo 4-tap scheme, this device features motion artifact suppression and switching ΔΣ background light cancelation. The sensor offers ranging up to 1m under 120klux, with sub-4.2mm accuracy.
- In Paper 5.5, Samsung Electronics presents a 2.3μm pitch, 1Mpixel, voltage-domain global shutter CMOS image sensor realizing a low parasitic light sensitivity of less than -105dB, random noise of 2.1e^- RMS and 42% QE at 940nm light, utilizing high-density in-pixel capacitors.
- In Paper 5.6, Samsung Electronics demonstrates a 1/2.65in, 44Mpixel, CMOS image sensor with 0.7μm pixel pitch fabricated using advanced full-depth DTI technology.
- In Paper 5.7, Sony Semiconductor Solutions presents a 132dB single-exposure dynamic range, 5.4Mpixel, CMOS image sensor. 0.6e^- RMS random noise is achieved, while maintaining a minimum composition SNR of 25dB at 100°C.
- In Paper 5.8, Sony Semiconductor Solutions presents a 1.45μm pixel, BSI-stacked 1/2.8 inch CIS achieving 0.5e^- RMS using a reference-shared in-pixel differential amplifier to improve read noise by 30% versus a conventional in-pixel differential amplifier.
- In Paper 5.9, National Tsing Hua University presents a multi-mode vision sensor for motion and saliency detection based on a ping-pong PWM pixel operating with a 0.8V supply. The sensor features in-pixel frame differencing, and mixed-mode event counting capability, achieving a frame rate of 510/890fps for frame difference / saliency detection modes at 74.4/121.6μW.
- In Paper 5.10, PROPHESEE presents a 3D-stacked, 1280×720 resolution, event-based vision sensor. Featuring a 4.86μm pixel and 1.066GEPS readout, the sensor achieves a dynamic range of >124dB with a programmable event rate controller and dynamic data formatting.

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Session 5 Highlights: Imagers and ToF Sensors

[5.1] A 240×192Pixel 10fps 70klux 225m-Range Automotive LiDAR SoC Using a 40ch 0.0036mm² Voltage/Time Dual-Data-Converter-Based AFE

[5.6] A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7μm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology

[5.7] A 132dB Single-Exposure-Dynamic-Range CMOS Image Sensor with High Temperature Tolerance

Paper 5.1 Authors: Satoshi Kondo[1], Hiroshi Kubota[2], Hisaaki Katagiri[2], Yutaka Ota[2], Masatoshi Hirono[3], Tuan Thanh Ta[1], Hidenori Okuni[1], Shinichi Ohtsuka[2], Yoshinari Ojima[2], Tomohiko Sugimoto[2], Hirotomo Ishii[2], Kentaro Yoshioka[1], Katsuyuki Kimura[2], Akihide Sai[1], Nobu Matsumoto[2]

Paper 5.1 Affiliation: [1]Toshiba, Kawasaki, Japan, [2]Toshiba Electronics Device & Storage Corporation, Kawasaki, Japan, [3]Toshiba, Yokohama, Japan

Paper 5.6 Authors: HyunChul Kim, Insung Joe, Jongeun Park, Doowon Kwon, Johyoung Kim, Dongsuk Cho, Taehun Lee, Changkyu Lee, Haeyong Park, Soojin Hong, Chongkwang Chang, Jingyun Kim, Jaekyu Lee, Yitae Kim, Sangil Jung, JungChak Ahn, Hyeongsun Hong, Kyupil Lee, Hokyu Kang

Paper 5.6 Affiliation: Samsung Electronics, Hwaseong, Korea

Paper 5.7 Authors: Yorito Sakano[1], Takahiro Toyoshima[1], Ryosuke Nakamura[1], Tomohiko Asatsuma[1], Yuki Hattori[1], Takayuki Yamanaka[2], Ryoichi Yoshikawa[2], Naoki Kawazu[1], Tomohiro Matsuura[1], Takahiro Iinuma[1], Takahiro Toya[1], Tomohiko Watanabe[2], Atsushi Suzuki[1], Yuichi Motohashi[1], Junichiro Azami[1], Yasushi Tateshita[1], Tsutomu Haruta[1]

Paper 5.7 Affiliation: [1]Sony Semiconductor Solutions, Atsugi, Japan, [2]Sony Semiconductor Manufacturing, Kikuyo, Japan

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

CONTEXT AND STATE OF THE ART

- Time-of-Flight (ToF) imaging is gaining traction for automotive applications of 3D ranging in short and long ranges up to a few hundred meters with reasonable depth resolutions.
- Advanced process technology with circuit innovations for CIS facilitates the pixel scaling and integrates in-pixel capacitor and Cu-Cu bonding, providing essential features, such as global shutter, wide dynamic range, and motion extraction.

TECHNICAL HIGHLIGHTS

- **Toshiba presents an analog front-end (AFE) based on dual-data-converter (DDC) incorporated with an off-chip SiPM achieving a higher angular resolution and long measurement range for scanning LiDAR in 28nm CMOS.**
  - A 40ch DDC-based AFE with a VCO measures time and analog signals simultaneously, demonstrating 2× higher pixel-resolution and 225m distance measurement under 70klux in 5× smaller area.
- **Samsung presents aggressive pixel scaling with advanced technologies, such as full-depth deep trench isolation (DTI) filled with doped polysilicon, realizing the smallest pixel to date.**
  - An advanced DTI with polysilicon in-situ deposition-etching-deposition (DED) process achieves 0.7μm pixel size without degrading performance relative to the previous generation in terms of full well capacity and YSNR.

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- **Sony introduces a dual photodiode approach with different sizes and an in-pixel floating capacitor for improving the dynamic range while maintaining SNR, even at high temperature.**
    - A large and a small photodiode with an in-pixel floating capacitor operating with the correlated double sampling technique achieves single-exposure dynamic range (DR) of 132dB, while maintaining SNR above 25dB over the full range at 100°C.

APPLICATIONS AND ECONOMIC IMPACT

- Scanning LiDAR is a strong candidate for self-driving cars and robot vision.
- High-resolution image sensors with continued pixel scaling remain in significant demand for mobile devices, such as smart phones and tablets, driving high volumes and leading to reduced manufacturing cost.
- As wide dynamic range image sensors are improving, their deployment in automotive and surveillance applications becomes widespread.

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Session 6 Overview: Ultra-High-Speed Wireline

Wireline Subcommittee

Session Chair: *Amir Amirkhany, Samsung Electronics, San Jose, USA*

Session Co-Chair: *Andrew Joy, Marvell Semiconductor, Northampton, UK*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, USA*

Data centers continue to drive the demand for high-speed interconnects. In the last few years we have witnessed the emergence of 56Gb/s and 112Gb/s transmitters and receivers with unparalleled complexity. This year, the trend continues with two complete transceiver designs at 112Gb/s, a complete transmitter at 112Gb/s, and a complete 56Gb/s transceiver. Another paper in this session pushes the limits by demonstrating 100Gb/s NRZ transmission in a 40nm CMOS process. While the first five papers in the session target ultra-high-performance communication, the other four papers discuss innovative techniques that tackle some of the practical challenges of getting high-speed interfaces into products. One paper in particular draws insights from machine-learning and stochastic detection techniques to implement a referenceless CDR with a very wide frequency locking range. Another paper deploys matrix feed-forward equalization to cancel crosstalk and increase the interconnect density on silicon interposers. Another publication introduces methods to track reference noise variations between transmitter and receiver in single-ended systems.

- In Paper 6.1, Xilinx describes a complete 112Gb/s PAM-4 transceiver in 7nm FinFET technology. The receiver deploys a 36-way time-interleaved successive approximation ADC and an inverter-based analog front-end, which achieves an analog energy-efficiency of 4.94pJ/b.
- In Paper 6.2, MediaTek also reports on a complete 112Gb/s ADC-DSP based PAM-4 transceiver in 7nm FinFET technology. The transceiver includes 4 TX and RX lanes with 3 common PLLs and achieves analog energy efficiency of 4.1pJ/b.
- In Paper 6.3, Rambus Inc. presents a 10-to-112Gb/s NRZ and PAM-4 transmitter with 1.2Vpp output swing. The transmitter is DAC-based and utilizes lookup-tables for pre-emphasis and achieves energy efficiency of 3.1pJ/b.
- In Paper 6.4, Samsung Electronics describes an ADC-based 56Gb/s transceiver with a baud-rate CDR. The transceiver is designed in a 10nm FinFET process and achieves an energy-efficiency of 7.7pJ/b.
- In Paper 6.5, Seoul National University presents a wide-locking-range reference-less CDR inspired by machine-learning and stochastic detection techniques. Measurements from a 6.4-to-32Gb/s 0.96pJ/b prototype in 40nm CMOS are presented to validate the techniques.
- In Paper 6.6, Nvidia Corporation introduces a novel reference noise compensation scheme for single-ended package-to-package links based on tracking of the duty-cycle of a single-ended forwarded clock lane. A 25Gb/s/pin prototype that deploys this technique and is fabricated in 16nm FinFET technology is described in the paper.
- In Paper 6.7, Seoul National University presents feed-forward cross-talk cancellation techniques suitable for HBM systems to enable higher routing density on a silicon interposer. The effectiveness of these concepts are demonstrated on an 8Gb/s/um prototype in 65nm technology.
- In Paper 6.8, Yuan Ze University describes a 100Gb/s NRZ transmitter in 40nm CMOS technology. The transmitter incorporates a 7b DAC and an 8-tap FFE.

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Session 6 Highlights: Ultra-High-Speed Wireline

[6.1] A 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET

[6.2] A 460mW 112Gbps DSP-Based Transceiver with 38dB Loss Compensation for Next Generation Data Centers in 7nm FinFET technology

[6.5] A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS

Paper 6.1 Authors: Jay Im[1], Kevin Zheng[1], Adam Chou[1], Stanley Chen[1], Jae Wook Kim[1], Lei Zhou[1], Yipeng Wang[2], KeeHian Tan[2], Declan Carey[3], Ilias Chlis[3], Marc Erett[3], Ade Bekele[1], Ying Cao[1], Winson Lin[1], Arianne Roldan[1], David Mahashin[1], Hong Ahn[1], Hongtao Zhang[1], Yohan Frans[1], Ken Chang[1]

Paper 6.1 Affiliation: [1]Xilinx, San Jose, CA, [2]Xilinx, Singapore, Singapore, [3]Xilinx, Cork, Ireland

Paper 6.2 Authors: Tamer Ali[1], Ehung Chen[1], Henry Park[1], Ramy Yousry[1], Yu-Ming Ying[1], Mohammed Abdullatif[1], Miguel Gandara[1], Chun-Cheng Liu[2], Po-Shuan Weng[2], Huan-Sheng Chen[2], Mohammad Elbadry[1], Qaiser Nehal[1], Kun-Hung Tsai[2], Kevin Tan[2], Yi-Chieh Huang[2], Chung-Hsien Tsai[2], Yuyun Chang[2], Yuan-Hao Tung[2]

Paper 6.2 Affiliation: [1]MediaTek, Irvine, CA, [2]MediaTek, Hsinchu, Taiwan

Paper 6.5 Authors: Kwanseo Park, Minkyo Shim, Han-Gon Ko, Deog-Kyoon Jeong

Paper 6.5 Affiliation: Seoul National University, Seoul, Korea

Subcommittee Chair: Amir Amirkhany, San Jose, CA

CONTEXT AND STATE OF THE ART

- Complete transceivers for state-of-the-art serial interfaces for electrical interconnects now achieve 112Gb/s to meet increasing bandwidth demands in data centers and telecommunication infrastructure. Power and area will continue to improve in order to meet the demand for higher bandwidth and achieve better energy efficiency, particularly in data centers.
- Rapid adoption of 7nm FinFET technology provides denser and lower-power digital logic. Continuing improvements in architecture and design techniques are also reported.

TECHNICAL HIGHLIGHTS

- **Xilinx introduces one of the first complete transceivers for 112Gb/s PAM-4 over long-reach copper interconnects. This 36-way time-interleaved 56GS/s 7b ADC-based receiver is combined with a quarter-rate transmitter using distributed inductor peaking and multi-phase clocking calibration techniques.**
  - The transceiver achieves < 1e-8 PRBS31 PAM-4 BER over a channel with 37.5dB loss at 28GHz while dissipating 602mW per channel, excluding the DSP.
- **MediaTek also presents a complete 112Gb/s ADC-based transceiver with very low power dissipation. The 56-way time-interleaved 7b asynchronous SAR ADC with 8-way track and hold sampler is used to perform an 8-to-24 tap FFE and 1-tap loop unrolled DFE.**
  - The transceiver achieves a BER better than 5e-7 with 38.9dB of channel loss with all near-end and far-end aggressors turned on with only 460mW of analog power.

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- **Seoul National University presents a technique inspired by machine learning to design a referenceless CDR. The stochastic phase-frequency detection algorithm uses the same information that the Alexander phase detector produces to learn the optimum weights for the phase and frequency correction.**
    - The CDR provides and unlimited frequency detection capability and a fast lock time of 11μs while avoiding harmonic locking. It achieves 0.96pJ/b at 32Gb/s with a BER of 1e-12.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced circuit techniques for robust > 100Gb/s transceivers in 7nm FinFET CMOS enables bandwidth scaling for data centers and high-performance computing in a power- and cost-efficient way. Low-power bandwidth scaling is required to keep pace with data center, cloud, and 5G infrastructure applications.
- High-speed and low-power referenceless CDRs are required for applications like optical modules used in data centers and communications infrastructure.
- The techniques of referenceless designs is allowing significant reductions of power in the clocking circuits. This leads to more aggressive power to be achieved.

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Session 7 Overview: High-Performance Machine Learning

Machine Learning Subcommittee

Session Chair: Geoffrey W. Burr, IBM Research Almaden, San Jose, CA

Session Co-Chair: Yan Li, Western Digital, Milpitas, CA

Machine-learning-specific processors continue to advance in performance, for the cloud and mobile devices at the edge, for mainstream applications such as convolutional networks. At the same, architectures are being developed for novel application opportunities, such as combinatorial optimization and specialized Neural Networks, such as GANs (Generative Adversarial Networks). This session comprises four papers, each representing advances in machine-learning chip performance in terms of energy efficiency, inference latency or time-to-convergence, and speed in terms of images-per-second.

- In Paper 7.1, MediaTek describes a 3.04mm^2 AI accelerator implemented in 7nm technology for a 5G smartphone SoC, introducing optimizations to reduce memory bandwidth and computing overhead, leading to 3.6TOPS, while also improving both area and power efficiency, ranging from 3.4-to-13.3TOPS/W.
- In Paper 7.2, Alibaba presents a 709mm^2 programmable CNN-optimized Neural Processing Unit (NPU) implemented in 12nm technology, which realizes 825TOPS at 700MHz in inference acceleration to achieve high throughput (78563images/s) and low latency (0.1ms) on the Resnet-50 network.
- In Paper 7.3, Tokyo Institute of Technology, Hokkaido University, and Hitachi describe STATICA – a 65nm 3×4mm^2 annealing processor for solving combinatorial optimization (Ising) problems, using a stochastic cellular automata architecture for single-cycle update of 512 fully-connected spins, which converges 2000× faster than simulated annealing approaches and 400× faster than CPU-based simulated annealing.
- In Paper 7.4, KAIST presents GANPU: a 32.4mm^2 energy-efficient (135TFLOPS/W) DNN training processor in 65nm technology, achieving high utilization for inference and training of GANs (Generative Adversarial Networks) by combining adaptive spatio-temporal workload multiplexing, sparsity exploitation, and exponent-only ReLU speculation.

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Session 7 Highlights: High Performance Machine Learning

[7.1] A 3.4-to-13.3TOPS/W 3.6TOPS Dual-Core Deep-Learning Accelerator for Versatile AI Applications in 7nm 5G Smartphone SoC

[7.2] A 12nm Programmable Convolution-Efficient Neural-Processing-Unit Chip Achieving 825TOPS

Paper 7.1 Authors: Chien-Hung Lin, Chih-Chung Cheng, Yi-Min Tsai, Sheng-Je Hung, Yu-Ting Kuo, Perry H Wang, Pei-Kuei Tsung, Jeng-Yun Hsu, Wei-Chih Lai, Chia-Hung Liu, Shao-Yu Wang, Chin-Hua Kuo, Chih-Yu Chang, Ming-Hsien Lee, Tsung-Yao Lin, Chih-Cheng Chen

Paper 7.1 Affiliation: MediaTek, Hsinchu City, Taiwan

Paper 7.2 Authors: Yang Jiao[1], Rong Jin[2], Yi-Jung Su[1], Chiente Ho[1], Li Yin[3], Yun Li[1], Long Chen[1], Zhen Chen[1], Liang Han[1], Lu Liu[3], Zhuyu He[3], Yu Yan[3], Jun He[3], Jun Mao[3], Xiaotao Zai[3], Xuejun Wu[3], Yongquan Zhou[3], Mingqiu Gu[1], Guocai Zhu[1], Rong Zhong[1], Wenyuan Lee[1], Ping Chen[1], Yiping Chen[1], Weiliang Li[3], Deyu Xiao[3], Qing Yan[3], Mingyuan Zhuang[3], Jiejun Chen[3], Yun Tian[3], Yingzi Lin[3], Wei Wu[3], Hao Li[4], Zesheng Dou[4]

Paper 7.2 Affiliation: [1]Alibaba, Sunnyvale, CA, [2]Alibaba, Seattle, WA, [3]Alibaba, Shanghai, China, [4]Alibaba, Hangzhou, China

Subcommittee Chair: Marian Verhelst, KU Leuven, Belgium, ML Subcommittee Chair

CONTEXT AND STATE OF THE ART

- The importance of machine learning is increasing rapidly, as deep learning gains widespread use in applications for processing images, speech and text – both in the cloud, as well as in mobile devices at the edge.
- In both the cloud computing and mobile contexts, improvements in the area and power efficiency of machine learning are crucial to enable more compute within a given electricity and cooling cost envelope, as well as to extend the battery life of edge devices.

TECHNICAL HIGHLIGHTS

- MediaTek introduces various optimizations, such as data re-use, weight compression and native asymmetric quantization to reduce memory bandwidth by 63% and also reduce computing overhead. This results in up to 2.78× better power efficiency and 3.41× higher area efficiency compared to prior art.
- Alibaba presents a machine-learning accelerator with 825TOPS at 700MHz via a convolution-efficient architecture. The chip achieves high throughput of 78563images/s or low latency of 0.1ms for Resnet-50, outperforming prior state-of-the-art by 2-to-5×.

APPLICATIONS AND ECONOMIC IMPACT

- The dual-core deep-learning accelerator demonstrated by Media Tek enhances versatile AI applications on 5G smartphones, with higher energy efficiency helping to prolong battery life.
- The programmable CNN interference accelerator implemented by Alibaba can potentially improve machine learning in the data center, particularly for the convolutional networks used for image processing, as well as for many other applications.

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Session 8 Overview: Highlighted Chip Releases

Industry Showcase Committee

Session Chair: *Alice Wang, Everactive, Santa Clara, CA*

Session Co-Chair: *Kush Gulati, Omni Design, Milpitas, CA*

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Sonia Leon, Intel, Santa Clara, CA

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Patrick Mercier, University of San Diego, CA

James Myers, ARM, Cambridge, UK

Mijung Noh, Samsung Electronics, Gyeonggi-do, Korea

Phillip Restle, IBM T.J. Watson, Yorktown Heights, NY

Naveen Verma, Princeton University, Princeton, NJ

Long Yan, Samsung Electronics, Gyeonggi-do, Korea

This special invited session highlights innovations in recent products announced within the last year. All of the product papers are at the cutting-edge within their respective markets. The papers delve into practical product-related topics, mass-production-related issues and solutions (e.g. reliability, thermal/voltage issues, packaging, etc.) in addition to circuit content and silicon measurement results.

- In Paper 8.1, Intel presents a hybrid mobile processor using active logic 3D stacking of 10nm and 22nm low-power FinFET chips with package-on-package (POP) DRAM in a 12×12mm^2 package to deliver client performance and mobile power and form factor. The chips use a Foveros Die interface and low-power signaling between the compute and base die achieving 0.2pJ/b. The base die includes a SERDES IP operating up to 11.7GB/s to support standards such as PCI Express Gen 3, USB 3.1 and MIPI MPHY Gear 4.
- In Paper 8.2, Xilinx introduces the Adaptive Compute Acceleration Platform (ACAP) processor targeted for workloads, such as deep learning and 5G wireless processing. The processor, designed in 7nm TSMC, includes general-purpose and real-time processors, programmable logic (PL), I/Os and transceivers, network-on-chip, DSP engines, and AI Engine (AIE) – an array of a specialized VLIW cores. Implemented using a combination of the AIE and PL, a 5-layer CNN achieves 5x10^6 images/s digit classification at a batch size of 50.

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- In Paper 8.3, ARM demonstrates their Neoverse N1 Software Development Platform, which includes a 7nm system-on-chip (SoC) containing four Neoverse N1 CPUs. The N1 processor is intended for data-center-class applications requiring many high-performance cores all working concurrently on a single chip. Compared to the previous-generation core (Cortex-A72), the N1 CPU provides 60% higher performance at the same frequency, and a 30% power efficiency gain in the same process technology.
- In Paper 8.4, AMD showcases a 7nm Radeon RX 5700 series GPU, incorporating 40 upgraded compute units, 256b-wide GDDR6 memory running at 14Gb/s for a total of 448GB/s bandwidth, a ×16 PCIe→ Gen4 link interface, six DP 1.4 HDR Display Ports, and the new RDNA graphics architecture. The chip achieves up to 1.5× greater performance per watt than its predecessor.

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Session 8 Highlights: Highlighted Chip Releases

[8.1] Lakefield: A Hybrid Three Dimensional 10nm and 22FFL Processor System in 12×12mm^2, 1mm Package-on-Package

Paper Authors: *Wilfred Gomes[1], Sanjeev Khushu[2], Doug B Ingerly[1], Patrick N Stover[3], Nasirul I Chowdhury[1], Frank Omahony[1], Ajay Balankutty[1], Noam Dolev[3], Martin G Dixon[1], Lei Jiang[3], Surya Prekke[5], Biswajit Patra[5], Pavel V Rott[1], Rajesh Kumar[1]*

Paper Affiliation: *[1]Intel Corporation, Hillsboro, OR, [2]Intel, Santa Clara, [3]Intel, Chandler, [4]Intel, Bengaluru, India*

Industry Showcase Co-Chairs:

Alice Wang, Everactive, Santa Clara, CA,

Kush Gulati, Omni Design Technologies, Milpitas, CA

CONTEXT AND STATE OF THE ART

- Low power consumption and small form factor are key targets of the development of mobile processor units
- Hybrid compute enables high performance and low power systems
- 3D Heterogeneous integration provides a new toolbox to advance Moore's law by mixing and matching best IP and Process nodes.
- Mapping architectures to Three Dimensional Logic on Logic Integration brings better than monolithic power and performance benefits for new mobile products

TECHNICAL HIGHLIGHTS

Intel introduces Lakefield, a hybrid mobile processor implemented using active logic 3D stacking to create a new class of products to deliver client performance and mobile power with small form factor.

- A 3D stacked 10nm+ and 22FFL FinFET hybrid processor system is integrated inside a 12×12mm^2, 1mm package-on-package. Stacking allows a large dynamic range in performance and power modes.
- Hybrid compute enabled by combining Sunnycove Big Core and Tremont Atom Cores
- The compute die is on an Intel 10nm+ process for power-performance and includes the CPU, GPU, IPU, memory and display engine based on IP from the Icelake product family.
- The base die is on Intel's 22FFL low-power FinFET process and contains the chipset functionality, including PCIe Gen3, USB type-C, storage, and the audio and sensor hub.

APPLICATIONS AND ECONOMIC IMPACT

- 3D Logic on Logic stacking enables a new class of computers with a wide range of performance and power modes.
- Low power, performance efficiency, and flexibility are key assets to drive effective economic impacts in the mobile space.
- Hybrid compute enables both high performance and low power scenarios

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Session 8 Highlights: Highlighted Chip Releases

[8.2] A Versatile 7nm Adaptive Compute Acceleration Platform Processor

Paper 8.2 Authors: Prasun K Raha, Tomai Knopp, Fu-Hing Ho, Ahmad Ansari, Thomas To, Vamsi Nalluri, Mrinal Sarmah, Rajeev Patwari

Paper 8.2 Affiliation: Xilinx, San Jose, CA

Industry Showcase Co-Chairs:

Alice Wang, Everactive, Santa Clara, CA,

Kush Gulati, Omni Design Technologies, Milpitas, CA

CONTEXT AND STATE OF THE ART

- New applications, such as autonomous driving, sensor fusion, robotics and IoT have high processing requirements and require a high-bandwidth interface (I/O) to be flexible and adapt to the changing requirements of different applications.
- General-purpose processors, like CPUs and GPUs, are increasingly less power efficient for these new applications and as the benefits of Moore's Law and Dennard scaling diminish.

TECHNICAL HIGHLIGHTS

Xilinx introduces the Adaptive Compute Acceleration Platform (ACAP) processor targeted for workloads, such as deep learning and 5G wireless processing.

- The processor, designed in 7nm TSMC, includes general-purpose and real-time processors, programmable logic (PL), I/Os and transceivers, a network-on-chip, DSP engines, and AI Engine (AIE) – an array of a specialized VLIW cores.
- Implemented using a combination of the AIE and PL, a 5-layer CNN achieves 5×10^6 images/s digit classification at a batch size of 50.

APPLICATIONS AND ECONOMIC IMPACT

- A heterogeneous platform leveraging field-programable gate array (FPGA) logic is well-suited for future applications with changing specifications – an application's implementation can be realized without a hardware upgrade.

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Session 8 Highlights: Highlighted Chip Releases

[8.3] A 3GHz Arm Neoverse N1 CPU in 7nm FinFET for Infrastructure Applications

Paper Authors: Robert Christy[1], Stuart Riches[2], Sujil Kottekkat[3], Prasanth Gopinath[4], Ketan Sawant[3], Anitha Kona[1], Rob Harrison[3]

Paper Affiliation: [1]ARM, Austin, Texas, [2]ARM, Cambridge, UK, [3]ARM, Sheffield, UK, [4]ARM, Bangalore, India

Industry Showcase Co-Chairs:

Alice Wang, Everactive, Santa Clara, CA,

Kush Gulati, Omni Design Technologies, Milpitas, CA

CONTEXT AND STATE OF THE ART

- Compute density and power efficiency requirements vary widely across the internet infrastructure.
- The ARM Neoverse family of processors target a combination of high performance and compute density, enabling computing platforms to be optimally scaled from IoT gateways to datacenter servers.

TECHNICAL HIGHLIGHTS

The first-generation Neoverse CPU (N1) achieves 60% higher performance at the same clock frequency (3GHz), and a 30% power-efficiency gain in the same process technology (7nm FinFET) compared to the previous generation.

- Performance gains come from a range of design features, including a dynamic 11-stage pipeline that lengthens or shortens according to the current operation, and a memory hierarchy supporting low latency, high bandwidth and scalability.

APPLICATIONS AND ECONOMIC IMPACT

- The Neoverse Platform is highly scalable from 25W 8-core systems to 128+ cores in servers. This enables a cloud-to-edge infrastructure transformation, with processing pushed to the edge where data is generated, providing more scalability than moving all data to centralized datacenters.

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Session 8 Highlights: Highlighted Chip Releases

[8.4] Radeon RX 5700 Series: The AMD 7nm Energy-Efficient High-Performance GPUs

Paper Authors: *Sal Dasgupta[1], Teja Singh[2], Ashish Jain[2], Samuel Naffziger[3], Deepesh John[4], Chetan Bisht[5], Pradeep Jayaraman[1]*

Paper Affiliation : *[1]AMD, Santa Clara, CA, [2]AMD, Austin, TX, [3]AMD, Ft. Collins, [4]AMD, Austin, [5]AMD, Orlando, FL*

Industry Showcase Co-Chairs:

Alice Wang, Everactive, Santa Clara, CA,

Kush Gulati, Omni Design Technologies, Milpitas, CA

CONTEXT AND STATE OF THE ART

- Low power consumption, high performance, programmability and architectural compatibility with prior generations are key targets in the development of new graphics-processor products.
- Moving to advanced process nodes, such as 7nm, combined with advanced low-power circuit techniques and microarchitectural innovation is needed to achieve these requirements.

TECHNICAL HIGHLIGHTS

AMD leverages 7nm FinFET technology, advanced power management and the new RDNA architecture in the Radeon RX 5700, which achieves up to 1.5× higher performance at the same power consumption as the previous generation in the same physical configuration.

- The GPU incorporates a 256b-wide memory interface of GDDR6 memory, operating at 14Gb/s for a total of 448GB/s bandwidth, an ×16 PCIe® Gen4 link interface, and six 1.4 Display Ports.
- The chip has 10.3B transistors on a 251mm^2 die in a 42.5×42.5mm^2 BGA package and operates up to 1.91GHz.

APPLICATIONS AND ECONOMIC IMPACT

- Moving to advanced process nodes brings significant benefits for graphics processors, when coupled with new design methodologies and CAD tools.
- Architectural compatibility allows the end-user to experience 1.5× more performance with the same power consumption as the previous generation on existing game titles.

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Session 9 Overview: Noise-Shaping ADCs

Data Converter Subcommittee

Session Chair: Dominique Morche, LETI, Grenoble, France

Session Co-Chair: Yun Chiu, University of Texas at Dallas, TX

Noise shaping continues to enable the high-DR ADC performance for many applications, including sensor, audio interface, and communication devices. This session begins with a 140dB DR current-sensing continuous-time ΔΣ modulator, and an audio-band ΔΣ ADC using chopped negative resistors. These are followed by three noise-shaping SARs with SNDR as high as 90dB and bandwidth as wide as 625kHz. A SAR-assisted noise-shaping pipeline ADC with 40MHz bandwidth is then presented. The session wraps up with a background calibrated 2-2 MASH continuous-time ΔΣ ADC and a reconfigurable, 4-channel audio ADC with integrated LDOs.

- In Paper 9.1, MediaTek demonstrates a 140dB DR current measurement continuous-time incremental ADC that uses a 12b DSM and achieves an 8ppm INL at 4kS/s.
- In Paper 9.2, Yonsei University presents an audio-band CT ΔΣ modulator with chopped negative resistors that achieves a 99.4dB SNDR while consuming 134μW.
- In Paper 9.3, Tsinghua University reports a 90dB-SNDR passive noise-shaping SAR that realizes a 4× passive gain with a 40kHz bandwidth while consuming 67μW.
- In Paper 9.4, University of Michigan presents a 4th-order single-channel cascaded-noise-shaping SAR ADC that achieves an 88dB SNDR over 100kHz bandwidth.
- In Paper 9.5, UT Austin describes a second-order noise-shaping SAR ADC uses a calibration-free closed-loop dynamic amplifier to achieve a 13.5b ENOB in a 625kHz bandwidth.
- In Paper 9.6, University of Macau shows a SAR-assisted noise-shaping pipeline ADC using partial interleaving to achieve a 40MHz bandwidth with 75dB SNDR while consuming 2.56mW.
- In Paper 9.7, Renesas describes a 2-2 MASH continuous-time ΔΣ ADC in 28nm CMOS with multi-rate LMS background calibration to achieve a 15MHz bandwidth and a 67.5dB SNDR.
- In Paper 9.8, NXP reports a reconfigurable, 4-channel audio ADC in 28nm CMOS that has all references and LDOs on-chip and achieves a peak SNR of 106dB while consuming 6mW.

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Session 9 Highlights: Noise-Shaping ADCs

[9.1] A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s

[9.5] A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier

Paper 9.1 Authors: Su-Hao Wu, Yun-Shiang Shu, Albert Yen-Chih Chiou, Wei-Hsiang Huang, Zhi-Xin Chen, Hung-Yi Hsieh

Paper 9.1 Affiliation: MediaTek, Hsinchu, Taiwan

Paper 9.5 Authors: Xiyuan Tang[1], Xiangxing Yang[1], Wenda Zhao[1], Chen-Kai Hsu[1], Jiaxin Liu[2], Linxiao Shen[1], Abhishek Mukherjee[1], Wei Shi[1], David Pan[1], Nan Sun[1]

Paper 9.5 Affiliation: [1]University of Texas, Austin, TX, [2]Tsinghua University, Beijing, China

Subcommittee Chair: Michael Flynn, University of Michigan, Ann Arbor, MI

CONTEXT AND STATE OF THE ART

- High-dynamic-range ADCs enable the sensing of critical parameters, which is required in many applications such as biomedical and electromechanical sensors, structure health monitoring, and environmental control. Today, the resolution of such ADCs is limited to a few hundred Hz, which limits the range of applications.
- The emerging noise-shaping SAR ADCs provide high resolution with high energy efficiency and compactness. However, passive noise shaping exhibits limited performance. The problem is solved by using an energy-efficient dynamic amplifier, but at the cost of PVT sensitivity.

TECHNICAL HIGHLIGHTS

- **MediaTek introduces a current sensor front-end realized in 55nm CMOS, which achieves a much wider bandwidth than previous state-of-the-art high-resolution ADCs.**
  - A continuous-time incremental ADC with 12b SAR quantizer and reset-then-open DAC demonstrates 140dB dynamic range at 4kS/s with only 1mW power consumption.
- **UT Austin presents a noise-shaping SAR ADC with a process, voltage, temperature (PVT)-robust closed-loop dynamic amplifier in 40nm CMOS. The design features sharp noise shaping and does not require gain calibration.**
  - A second-order noise-shaping SAR achieves 13.5b ENOB with less than 1dB SNDR drop across –10°C to 80°C and ±12% power supply variation with a Walden FoM of 6.8fJ/conversion-step.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced circuit techniques that enable higher-DR and wider-BW ADCs make many new applications possible and efficient.
- High-performance and low-power temperature-process-voltage-insensitive ADCs significantly reduce manufacturing cost.
- Lower power consumption while preserving performance eases the development of portable applications.

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Session 10 Overview: High Performance Transceivers

Wireless Subcommittee

Session Chair: Renaldi Winoto, Mojo Vision, Saratoga, CA

Session Co-Chair: Xin He, NXP, Netherlands

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR

5G-NR and 802.11ax standards require extreme in-band signal fidelity, low out-of-band emission, large signal bandwidth, multi-carrier concurrency and a large number of ports for MIMO/spatial signal processing. This session will demonstrate record data-rates and the highest level of transceiver integration. A state-of-the-art digital PA capable of 1024-QAM and 160MHz bandwidth is presented. Innovative RF & mixed-signal techniques to suppress out-of-band noise and spurious will be showcased.

- In Paper 10.1, the University of Macau and Instituto Superior Tecnico/University of Lisboa utilize an N-path technique that is popular in RF receivers, to improve RX-band noise performance of 5G-NR transmitters. An out-of-band noise level of -157.5dBc/Hz is achieved using the proposed technique.
- In Paper 10.2, the University of Southern California presents a reconfigurable Sigma-Delta RF-DAC with a novel Tri-Level Time-Approximation Filter that can be used for cellular FDD radio.
- In Paper 10.3, Mediatek showcases a highly-integrated multi-mode, multi-band 2/3/4/5G transceiver supporting carrier aggregation and 200MHz bandwidth with 4×4 RX-MIMO and 2×2 TX-MIMO.
- In Paper 10.4, Mediatek presents a dual-band, configurable 4×4 or dual-concurrent 2×2 802.11ax transceiver with 1024-QAM and 160MHz bandwidth.
- In Paper 10.5, Intel demonstrates the first dual-band, digital PA capable of 1024-QAM, 160MHz bandwidth at 19dBm output power and 21% power efficiency.
- In Paper 10.6, Mediatek proposes a new approach to address the difficult CIM3 spec. A CIM3 of < -65dBc is achieved with a harmonic rejection mixer using two-path 25% duty-cycle LO.
- In Paper 10.7, Michigan State University, the University of Utah and Oregon State University push the linearity boundary of quadrature digital transmitters, achieving an EVM of better than -40dB across a wide output power range.
- In Paper 10.8, Washington State University proposes a novel time-domain spatial signal processor that can be used for beam-forming, beam-nulling and spatial filtering.

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Session 10 Highlights: High Performance Transceivers

[10.3] A 12nm CMOS RF Transceiver Supporting 4G/5G UL MIMO

[10.4] A 4x4 Dual-Band Dual-Concurrent WiFi 802.11ax Transceiver with Integrated LNA, PA, and T/R Switch Achieving +20dBm 1024-QAM MCS11 P_{out} and -43dBm EVM Floor in 55nm CMOS

[10.5] A Fully Integrated 27dBm Dual-Band All-Digital Polar Transmitter Supporting 160MHz for Wi-Fi 6 Applications

Paper 10.3 Authors: Ming-Da Tsai[1], Song-Yu Yang[1], Chi-Yao Yu[1], Ping-Yu Chen[1], Tzung-Han Wu[1], Mohammed Hassan[2], Chi-Tsan Chen[1], Chao-Wei Wang[1], Yen-Chuan Huang[1], Li-Han Hung[1], Wei-Hao Chiu[1], Anson Lin[1], Bo-Yu Lin[1], Arnaud Werquin[2], Chien-Cheng Lin[1], Yen-Horng Chen[1], Jen-Che Tsai[1], Yuan-Yu Fu[1], Bernard Tenbroek[2], Chinq-Shiun Chiu[1], Yi-Bin Lee[1], Guang-Kaai Denhg[1]

Paper 10.3 Affiliation: [1]MediaTek, Hsinchu, Taiwan, [2]MediaTek, Kent, United Kingdom

Paper 10.4 Authors: Eric Lu[1], Wen-Kai Li[2], Zhiming Deng[1], Edris Rostami[1], Pi-An Wu[2], Keng-Meng Chang[2], Yu-Chen Chuang[2], Chang-Ming Lai[2], Yang-Chuan Chen[1], Tzu-Hsui Peng[2], Tzung-Chuen Tsai[2], Hui-Hsien Liu[2], Chien-Chih Chiu[2], Bryan Huang[1], Yao-Chi Wang[2], Jing-Hong Conan Zhan[2], Osama Shanaa[1]

Paper 10.4 Affiliation: [1]MediaTek, San Jose, USA, [2]MediaTek, Hsinchu, Taiwan

Paper 10.5 Authors: Assaf Ben-Bassat[1], Shahar Gross[2], Anna Nazimov[1], Ashoke Ravi[3], Bassam Khamaisi[1], Elan Banin[2], Eli Borokhovich[2], Nahum Kimigarov[2], Phillip Skliar[2], Rotem Banin[1], Sarit Zur[2], Sebastian Reinhold[4], Smadar Bruker[2], Tzvi Maimon[1], Uri Parker[2], Ofir Degani[1]

Paper 10.5 Affiliation: [1]Intel, Haifa, Israel, [2]Intel, Petach Tikva, Israel, [3]Intel, Hillsboro, USA, [4]Intel, Munich, Germany

Subcommittee Chair: Stefano Pellerano, Intel Corporation, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- Both WiFi and cellular standards continue to evolve with 5G-NR and WiFi-6/802.11ax to deliver ever increasing data throughput. This is accomplished by using dense 1024-QAM modulation, a wide bandwidth of up to 200MHz and multiple parallel data-streams using uplink & downlink MIMO
- Carrier aggregation and concurrent operation allows cellular and WiFi radios to obtain larger spectrum resources when a single contiguous frequency range is not available
- Modern cellular and WiFi radios ultimately find application in mobile, IoT and other constrained devices that necessitate a high level of integration, compact form factor and efficient use of limited battery power

TECHNICAL HIGHLIGHTS

- **MediaTek introduces a 2/3/4/5G compliant transceiver in 12nm FinFET CMOS supporting 200MHz bandwidth, 2×2 Up-link Coherence MIMO.**
  - A multi-mode, multi-band cellular transceiver supporting 6-carrier aggregation downlink, 2-carrier aggregation uplink, 4×4 MIMO 256-QAM employs a novel LO phase-synchronization for the first demonstration of 2×2 coherent up-link MIMO.
- **MediaTek introduces a WiFi 802.11ax transceiver in 55nm CMOS supporting 4×4 dual-band WiFi, and 2×2+2×2 dual-band, dual-concurrent operation.**

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- A fully-integrated transceiver with PA linearization achieves +20dBm output power with -35dB EVM and 160MHz bandwidth. Furthermore a new dynamic impedance-switching biasing technique to reduce crystal noise contribution enables an EVM floor of better than -41dB in the 5GHz band.

- **Intel introduces a wideband polar digital WiFi 6 transmitter in 28nm CMOS supporting (2.5/5GHz) dual-band WiFi.**
  - A digital-to-time converter-based digital polar transmitter with a switched-capacitor PA achieves state-of-the-art back-off efficiency of 21.2% at MCS11/160MHz/5GHz, and 35% for MCS7/40MHz/2.5GHz.

APPLICATIONS AND ECONOMIC IMPACT

- 5G radio technology promises a 10-to-100× increase in data-rate with a 10× reduction of latency. This will continue the exponential growth of traditional mobile data traffic and open new opportunities in machine autonomy, virtual reality and pervasive connected devices and sensors.
- WiFi 6 or 802.11ax offers higher data throughput for immersive experience applications and connecting more smart devices in an environment with high device density.
- Deployment of 5G and WiFi6 has begun and will power mobile and connected devices throughout the next decade.

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Session 11 Overview: DC-DC Converters

Power Management Subcommittee

Session Chair: *Yan Lu, University of Macau, Taipa, Macao*

Session Co-Chair: *Makoto Takamiya, University of Tokyo, Tokyo, Japan*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA*

DC-DC converters are essential for high-efficiency and high-power-density energy conversion. To cater for higher output current with a low output voltage, hybrid converters that utilize both inductors and capacitors are promising to achieve considerably higher voltage-conversion ratios and efficiencies at the same time. This session covers the full scope of buck, boost, as well as buck-boost hybrid DC-DC converters. Finally, this session also includes a battery-cell reconfiguring converter enabling maximum energy extraction from multiple cells.

- In Paper 11.1, the University of Texas at Richardson and Texas Instruments present a tri-state double step-down converter to achieve direct 12/24V-to-1V conversion with 91.2% peak efficiency and 3W peak power. Online flying capacitor voltage rebalancing is improved by 16.7% with 9ns on-duty mismatch, improving reliability.
- In Paper 11.2, Dartmouth College presents a fully integrated DC-DC converter using a multiphase LC resonator, which merges planar spiral (coupled) inductors with distributed flying capacitors, to improve current distribution and quality factor while improving efficiency and power density. It achieves >80% efficiency over an output power range of 10 to 750mW.
- In Paper 11.3, Leibniz University Hannover presents a self-timed resonant high-voltage DC-DC converter in HV CMOS SOI with one-step conversion from a voltage in the 100-to-325V range to an output voltage in the 3.3-to-10V range, optimized for <500mW applications, such as IoT and smart homes. It comprises an on-chip power stage with only one external inductor (10µH) and one external capacitor (0.47µF).
- In Paper 11.4, the University of Texas at Dallas reports a 2MHz 48-to-80V input DC-DC bus converter that adopts the adaptive ZVT controller realized in a 0.5µm 120V CMOS process, which adaptively reduces the peak auxiliary current with the load to improve the light-load efficiency by 14%.
- In Paper 11.5 the University of Macau, South China University of Technology, and University of Lisboa present a 2-phase hybrid boost converter for high conversion ratios, with a doubled switching pulse width, soft charging between the flying capacitors, and lower switch V_{DS} stresses. It achieves an efficiency of 93.5 and 91.7% with conversion ratios of 4.5 and 6, respectively.
- In Paper 11.6, Sookmyung Women's University presents a single-inductor bipolar-output converter for AMOLED displays simultaneously transferring energy to bipolar outputs. The proposed converter achieves small ripple voltages on positive and negative outputs of 24.5 and 28 mV, respectively, at load current of 300mA.
- In Paper 11.7, Samsung Electronics presents a voltage-tolerant buck-boost converter with continuous output transfer current and flying capacitor soft charger. In addition, to support a wide range of load current and a high voltage-conversion ratio, a dual-channel interleaved topology is proposed.
- In Paper 11.8, KAIST and Samsung Electronics present a step-up/down converter powering disposable IoTs with up to 3 reconfigurable alkaline battery cells, which enables its input/output currents to be continuous, resulting in reduced power loss on the inductor and battery DCRs. With a battery cell balancer, the battery operation time is extended.

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Session 11 Highlights: DC-DC Converters

[11.2] A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator

Paper Authors: *P. H. Mclaughlin, Z. Xia, J. T. Stauth*

Paper Affiliation: *Dartmouth College, Hanover, NH*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management Subcommittee*

CONTEXT AND STATE OF THE ART

- DC-DC converters are used in many applications ranging from servers to mobile products.
- The size and cost of DC-DC converters are limited by their passive components including inductors and capacitors.
- There is a compelling need to eliminate or shrink the passive components that are embedded in the existing systems.

TECHNICAL HIGHLIGHTS

- Dartmouth College presents a fully integrated DC-DC converter using a multiphase LC resonator.
- The converter merges planar spiral (coupled) inductors with distributed flying capacitors to improve current distribution and quality factor while improving efficiency and power density.
- The converter achieves over 80% efficiency from 10 to 750mW and peak efficiency over 85%.

APPLICATIONS AND ECONOMIC IMPACT

- A very compact size DC-DC converter without off-chip passive components for variety of applications including mobile and performance computing, mobile communications, and embedded systems.

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Session 12 Overview: Advanced Optical Communication Circuits

Wireline Subcommittee

Session Chair: Mounir Meghelli, IBM T.J. Watson Research Center, New York, USA

Session Co-Chair: Takashi Takemoto, Hitachi, Ltd., Sapporo, Japan

Optical communications continue to hold a lot of promise to satisfy the ever-increasing need for higher bandwidth while lowering cost and power consumption. Papers in this session describe advances in circuits and devices combined with higher levels of integration between photonics and electronics. The first paper of the session describes a 112Gb/s PAM-4 micro-ring-based optical transmitter using a 3D-integrated silicon photonic and CMOS circuits assembly. Continuing with the advances in silicon-photonic-based optical communications, the second paper describes a 4-channel electro-optical transceiver operating at an aggregate bandwidth of 200Gb/s using 55nm BiCMOS ICs 3D-integrated onto a silicon photonic IC. The third paper describes the design of a 48GHz-bandwidth linear driver implemented in 65nm CMOS and targeting beyond 400Gb/s coherent optical transmission. The last paper of the session describes a 55nm BiCMOS 100GS/s 4:1 interleaver achieving 4.9b ENOB and >53GHz bandwidth and demonstrating a 100GBaud PAM-4 signal.

- In paper 12.1, Intel describes a 3D-integrated 112Gb/s PAM-4 optical transmitter using a micro-ring modulator. The highly integrated transmitter consists of a silicon photonic IC and a 28nm CMOS electronic IC assembled using copper-pillar flip-chip bonding. The photonic IC consists of a 10µm radius depletion-mode micro-ring modulator with integrated heater, a III-V/Si hybrid 1310nm laser, monitor photodiodes and output fiber coupler. The CMOS IC includes a 112Gb/s PAM-4 serializer/modulator driver and temperature control circuitry. The optical transmitter achieves a 7.5pJ/b power efficiency including laser power and is capable of sub-GHz modulator tuning resolution at temperatures up to 55ºC.
- In paper 12.2, STMicroelectronics presents a 4-channel 200Gb/s PAM-4 electro-optical transceiver. The device is fabricated in a 55nm BiCMOS technology and 3D-assembled onto a silicon photonic front-end IC through copper pillars. The device achieves a -9.5dBm optical input sensitivity at 2e-4 BER and 6dB extinction ratio at the TX output while consuming 850mW per channel.
- In paper 12.3, NTT describes a 65nm CMOS broadband low-power linear driver IC for coherent optical links. It achieves 48GHz bandwidth and 225mW power consumption by using multi-peaking and stacked current re-use techniques. A four-channel driver was integrated on a single chip co-packaged with a four-channel Mach-Zehnder modulator and successfully demonstrated 64GBaud dual polarity 32-QAM optical output for an aggregate data rate of 640Gb/s at a power efficiency of 1.4pJ/b.
- In paper 12.4, IMEC and Ghent University describe the design of a 100GS/s 4:1 interleaver implemented in 55nm BiCMOS technology. It is constructed using 2:1 sub-interleavers using a return-to-zero generation that features an intrinsic feed-forward equalizer. The interleaver has an ENOB of 4.9 bits with an analog bandwidth larger then 53GHz and was demonstrated at 100GBaud PAM-4.

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Session 12 Highlights: Advanced Optical Communication Circuits

[12.1] A 3D-Integrated Microring-Based 112Gb/s PAM-4 Silicon-Photonic Transmitter with Integrated Nonlinear Equalization and Thermal Control

[12.2] A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications

Paper 12.1 Authors: Hao Li, Ganesh Balamurugan, Meer Sakib, Ranjeet Kumar, Hasitha Jayatilleka, Haisheng Rong, James Jaussi, Bryan Casper

Paper 12.1 Affiliation: Intel, Hillsboro, OR

Paper 12.2 Authors: Enrico Sentieri[1], Tino Copani[2], Andrea Paganini[1], Matteo Traldi[1], Angelo Palladino[1], Antonio Santipo[1], Lorenzo Gerosa[1], Matteo Repossi[1], Gianluca Catrini[2], Marta Campo[2], Roberto Pelleriti[2], Daniele Baldi[1], Gianluca Radaelli[1], Angelo Moroni[1], Francesco Clerici[2]

Paper 12.2 Affiliation: [1]STMicroelectronics, Agrate, Italy, [2]STMicroelectronics, Catania, Italy

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- Optical communication is increasingly used to interconnect the computing, storage, and networking hardware inside data centers. Large data centers require links spanning up to 2 km, and metro-area data centers require even longer links. Compact and low-cost optical modules capable of transmitting and receiving 200 – 400 Gb/s over such distances will be needed for future data centers. The papers in this session describe circuits to address this need by communicating 50 – 100 Gb/s over each fiber using PAM-4 modulation. For example, paper X.2 specifically addresses the IEEE802.3bs 200GBASE-DR4 standard.
- Since many such modules are packed side-by-side in networking and computing infrastructure, low power consumption is required to prevent overheating the equipment. The highly-integrated approaches in this session permit low power consumption, obviating the need for expensive water-cooling. For example, paper X.1 permits the use of micro-ring modulators whose small size (10μm-diameter) imply low energy consumption. The thermal variability and nonlinearities that usually plague such modulators are elegantly addressed.

TECHNICAL HIGHLIGHTS

- **Intel describes a 3D-integrated 112Gb/s PAM-4 optical transmitter using a micro-ring modulator. The highly integrated transmitter consists of a silicon photonic IC and a 28nm CMOS electronic IC assembled using copper-pillar flip-chip bonding**
    - The optical transmitter achieves a 7.5pJ/b power efficiency including the laser and is capable of sub-GHz modulator detuning resolution up to 55ºC with less than 0.5dB power penalty.
- **STMicroelectronics presents a 4-Channel PAM-4 electro-optical transceiver compliant with the IEEE 200GBASE-DR4 standard. The device is fabricated in a 55nm BiCMOS technology and 3D-assembled onto a silicon photonics front-end IC through copper pillars.**
    - The device achieves a -9.5dBm optical input sensitivity at 2e-4 BER and 6dB extinction ratio at the Mach-Zehnder-based transmitter output while consuming 850mW per channel.

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APPLICATIONS AND ECONOMIC IMPACT

- Optical communications form the communication backbone within data centers and network infrastructure. They also hold promise as an alternative to copper for within-rack communication. These papers demonstrate optical transceiver components that satisfy the need for higher bandwidth while lowering cost and power consumption by combining advances in circuits and devices along with higher levels of integration between photonics and electronics.

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Session 13 Overview: Non-Volatile Memory

Memory Subcommittee

Session Chair: Jongmin Park, SKhynix, Icheon, Korea

Session Co-Chair: Yasuhiko Taito, Renesas Electronics, Kodaira, Japan

The five papers in this session include the fast advancing non-volatile memory technologies. The 4b/cell of 3D NAND flash technology becomes practical in many applications and the high-speed SLC NAND flash has great potential to improve computing system performance by filling the latency gap between DRAM and flash memories. Embedded MRAMs need higher read speed and lower power operation for practical use in the next generation.

- In Paper 13.1, Samsung presented a 1Tb 4b/cell 92-stacked-WL 3D V-NAND flash memory featuring 5th generation technology with 1.2Gb/s high-speed interfaces. To improve program and read performance, the number of verify during program is reduced and an adaptive read scheme is developed.
- In Paper 13.2, SKhynix demonstrated a 1Tb 4b/cell 3D NAND flash memory with 30MB/s program throughput utilizing the highly area-efficient technology of peripheral circuits under the memory cell array, which achieves an 8.4Gb/mm^2 area capacity.
- In Paper 13.3, TSMC presented a 32Mb embedded STT-MRAM chip in a 22nm logic process. The read speed of the 10ns access time and read power of 0.8μA/MHz/bit are demonstrated.
- In Paper 13.4, National Tsing Hua University presented a 22nm 1Mb STT-MRAM macro using its multibit sense amplifier to achieve compact-area, low peak current, and low read energy for dual-mode operations.
- In Paper 13.5, KIOXIA Corporation developed a 128Gb 1b/cell 3D flash memory using 96-word-line-layer technology. The flexible suspend operation for program and erase are developed for a smaller random read latency of under 50μs. Also, 75μs program time and 4μs read latency is achieved from the novel optimized floorplan.

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Session 13 Highlights: Non-Volatile Memories

[13.5] A 128Gb 1b/Cell 96-Word-Line-Layer 3D Flash Memory to Improve Random Read Latency with t_{PROG}=75us and t_R=4us.

[13.3] A 22nm 32Mb Embedded STT-MRAM with 10ns Read Speed, 1M Cycle Write Endurance, 10 Years Retention at 150°C and High Immunity to Magnetic Field Interference

Paper 13.5 Authors: Toshiyuki Kouchi[1], Noriyasu Kumazaki[1], Masashi Yamaoka[1], Sanad Bushnaq[1], Takuyo Kodama[1], Yuki Ishizaki[1], Yoko Deguchi[1], Akio Sugahara[1], Akihiro Imamoto[1], Norichika Asaoka[1], Ryosuke Isomura[1], Takaya Handa[1], Junichi Sato[2], Hiromitsu Komai[1], Atsushi Okuyama[1], Kanagawa Naoaki[1], Yasufumi Kajiyama[1], Yuri Terada[1], Hidekazu Ohnishi[1], Mami Kakoi[1], Masahiro Yoshihara[1], Hiroki Yabe[3], Cynthia Hsu[3]

Paper 13.5 Affiliation: [1] KIOXIA Corporation, Yokohama, Japan, [2]KIOXIA Systems Corporation, Yokohama, Japan, [3]Western Digital, Milpitas, CA

Paper 13.3 Authors: Yu-Der Chih, Yi-Chun Ehtan Shih, Chia-Fu Lee, Yen-An Chang, Po-Hao Lee, Hon-Jarn Lin, Yu-Lin Chen, Chieh-Pu Lo, Meng-Chun Shih, Kuei-Hung Shen, Harry Chuang, Tsung-Yung Jonathan Chang

Paper 13.3 Affiliation: TSMC, Hsinchu, Taiwan

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

CONTEXT AND STATE OF THE ART

- X.5 reveals the high-speed SLC NAND flash with fast random access read and program performance targeting storage class memory (SCM) applications.
- X.3 demonstrates the embedded MRAM for flash memory replacement.

TECHNICAL HIGHLIGHTS

- **KIOXIA presents a 128Gb 1 bit/cell 3D flash memory chip that has been developed on a 96-word-line-layer technology.**
  - The flexible suspend operation for program and erase realizes smaller random read latency of under 50μs.
  - 75μs program time and 4μs read latency is achieved from the novel optimized floorplan.
- **TSMC presents an embedded MRAM in a 22nm logic CMOS process for flash memory replacement.**
  - A 32Mb embedded MRAM with a 10ns read access with low power of 0.8μA/MHz/bit.
  - Increasing magnetic interference immunity by three orders of magnitude with deposited magnetic shield film on package.

APPLICATIONS AND ECONOMIC IMPACT

- With an optimized SSD controller in combination with fast flash memory chips with read latency (t_R) of 3μs, the random read latency (RRL) of the SSD system has been improved by 4× ~ 10× compared to that of conventional SSDs with normal 3D flash memories.
- Shows that MRAM can be a strong candidate for next-generation low-cost/low-power SoCs and MCUs for IoT and wearables with lower cost adder and high speed.

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Session 14 Overview: Low-Power Machine Learning

Machine Learning and AI Subcommittee

Session Chair: Jun Deguchi, Kioxia Corporation, Kawasaki, Japan

Session Co-Chair: Rangharajan Venkatesan, NVIDIA, Santa Clara

Subcommittee Chair: Marian Verhelst, KU Leuven, Belgium, ML Subcommittee

Deep-learning hardware finds increasing application in edge and mobile devices, which are typically battery powered and operated in an always-ON state, demanding extremely low power of operation. This session explores circuit, architecture, and neural-network optimizations to efficiently exploit sparsity and data reuse along with mixed-precision computation and adaptive power gating.

- In Paper 14.1, Southeast University, EPFL, and Columbia University present a 0.44×0.52 mm^2 ultra-low-power keyword-spotting chip using a depthwise-separable CNN and Mel Frequency Cepstrum Coefficient circuit, achieving 510nW (a 10× power reduction over state of the art) with 2KB on-chip memory in 28nm CMOS.
- In Paper 14.2, Tsinghua University and Anhui University describe a video-processor chip that leverages temporal correlation across frames to improve energy efficiency without accuracy loss for surveillance and auto-pilot applications. The 4.0×3.0 mm^2 chip demonstrates 24.7-to-34.3μJ/frame for MobileNet-16 in 65nm technology.
- In Paper 14.3, Tsinghua University and National Tsing Hua University present a 3.0×3.0mm^2 compute-in-memory processor that exploits sparsity in both input activations and weights along with efficient data reuse to achieve 2.9-to-35.8TOPS/W in 65nm technology.

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Session 14 Highlights: Low-Power Machine Learning

[14.1] A 510nW 0.41V Low-Memory Low-Computation Keyword-Spotting Chip Using Serial FFT-Based MFCC and Binarized Depthwise Separable Convolutional Neural Network in 28nm CMOS

Paper Authors: W. Shan[1], M. Yang[2], J. Xu[1], Y. Lu[1], S. Zhang[1], J. Yang[1], M. Seok[3], L. Shi[1]

Paper Affiliation: [1]Southeast University, Jiangsu, China, [2]EPFL Neuchâtel, Switzerland, [3]Columbia University, New York

Subcommittee Chair: Marian Verhelst, KU Leuven, Belgium, ML Subcommittee

CONTEXT AND STATE OF THE ART

- Voice has become a common way to interact with electronic devices. Keyword-spotting chips are designed for always-on, hands-free control of battery-powered applications and therefore, require ultra-low power dissipation. They are tuned to recognize only a specific set of keywords instead of performing full speech recognition.
- State-of-the-art keyword spotting chips use highly customized signal processing and machine-learning approaches to reduce the power dissipation to several tens of microwatts and below. This enables operation from a small battery for several years.

TECHNICAL HIGHLIGHTS

- **A keyword-spotting chip that achieves sub-microwatt operation by leveraging several architectural techniques to reduce computation and memory footprint.**
    - It uses a power-efficient serial FFT to process 32ms long audio frames.
    - Its neural network is binarized, leading to a total memory footprint of 2KB for the detection of two keywords.
    - Using near-threshold operation in 28nm CMOS, the total power dissipation is 510nW.

APPLICATIONS AND ECONOMIC IMPACT

- The design is suitable for wake-up keyword detection in personal assistants, such as Alexa or Siri. It can also be used to implement a user interface for small autonomous devices, such as wireless earphones and other wearables.
- Power-efficient keyword spotting will fuel further proliferation of voice-controlled electronics in low-cost, resource-constrained hardware platforms.

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Session 15 Overview: SRAM and Compute-in-Memory

Memory Subcommittee

Session Chair: Kyu-Hyoun Kim, IBM, Yorktown Heights, NY

Session Co-Chair: Eric Karl, Intel, Hillsboro, OR

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

Energy efficient acceleration of machine learning and AI workloads is a key that will enable further breakthroughs in deep learning (DL) applications. Shifting computation to inside the memory array (compute-in-memory) is a leading approach to enable breakthroughs in energy efficiency and throughput. SRAM continues to be a critical technology enabler for a wide range of applications from low-power to high-performance computing and is a key element in emerging architectures for compute-in-memory (CIM). This session showcases the leading-edge SRAM developments in 5nm technology and showcases progress in CIM designs that increase precision, throughput and computation energy efficiency. TSMC shows the first 5nm SRAM technology and highlights key supporting circuit techniques. TSMC presents a 7nm CIM approach based upon foundry-standard bitcells and Flash ADCs. National Tsing Hua University presents three papers with innovations in CIM design.

- In Paper 15.1, TSMC presents a 5nm 135Mb SRAM array implemented with EUV and high-mobility transistor technology. Two write assist circuits demonstrate > 300mV V_{CCMIN} reduction while achieving > 30Mb/mm^2 bit density – the highest reported SRAM array density to date.
- In Paper 15.2, National Tsing Hua University presents a 6T SRAM CIM with 8b-input × 8b-weight MAC operations that supports not only forward computation (for inference) but also backward propagation (for training).
- In Paper 15.3, TSMC describes a 4b-input × 4b-weight CIM utilizing standard 8T SRAM bitcells and a Flash ADC in a 7nm CMOS FinFET technology. The array computes 4b multiply and average functions delivering 372 GOPS and 351 TOPS/W.
- In Paper 15.4, National Tsing Hua University demonstrates a 22nm 2Mb ReRAM non-volatile CIM that supports 4b-input and signed 4b-weights in scrambled 2's complement format. This paper features a 4b-input non-volatile CIM that achieves access time of 18.3ns at its full precision.
- In Paper 15.5, National Tsing Hua University proposes a 6T SRAM CIM that performs 8b-weight MAC operations in a bitwise manner that enables the low-MAC aware scheme to save energy consumption. The paper features 16.63 TOPS/W for 8b-input × 8b-weight, and 68.44 TOPS/W for 4b-input × 4b-weight operations.

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Session 15 Highlights: SRAM and Compute-In-Memory

[15.1] A 5nm 135Mb SRAM in EUV and High-Mobility-Channel FinFET Technology with Metal Coupling and Charge-Sharing Write-Assist Circuitry Schemes for High-Density and Low-V_{MIN} Applications

Paper Authors: Jonathan Chang

Paper Affiliation: TSMC, Hsinchu, Taiwan

Subcommittee Chair: Jonathan Chang, TSMC

CONTEXT AND STATE OF THE ART

- Advances in compute performance across a range of product applications are driving the need for improved bandwidth and energy efficiency from the memory hierarchy.
- On-die SRAM is increasingly important to provide low latency, energy efficient caches to drive further compute performance improvements.
- Rapidly accelerating compute requirements and energy constraints are driving the need for improved bandwidth, reduced latency, higher density and better energy efficiency from the memory hierarchy.
- Caches based on highest-density on-die SRAM are indispensable for achieving the required improvements, e.g. for supercomputing, AI and CIM.

TECHNICAL HIGHLIGHTS

- TSMC showcases the first 5nm SRAM array featuring the world's smallest bitcell (0.0214um^2) and array bit density exceeding 30Mb/mm^2.
- 5nm SRAM minimum operating voltage (V_{MIN}) matches 7nm technology capability and the paper presents two write assist circuits that achieve > 300mV reduction in the minimum operating voltage.

APPLICATIONS AND ECONOMIC IMPACT

- SRAM is a foundational component of the memory hierarchy in all modern system-on-chip designs, ranging from mobile processors to servers and high-performance compute accelerators.
- Continued SRAM scaling paves the way for improved products ranging from mobile to high-performance computing applications.

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Session 16 Overview: Nyquist and VCO-Based ADCs

Data converters Subcommittee

Session Chair: Bob Verbruggen, Xilinx, Dublin, Ireland

Session Co-Chair: Takashi Oshima, Hitachi Ltd., Tokyo, Japan

This session highlights the latest developments in Nyquist and VCO-based ADCs. These ADCs use innovative architectures and techniques to improve speed, linearity or power consumption. Three designs with GHz bandwidth, two SAR-based designs with tens of MHz of bandwidth and two VCO-based designs offer an interesting mix of architectures and applications. Several designs also attempt to tackle the challenge of driving the ADC, using track-and-hold amplifiers, input capacitance reduction, or inherent anti-aliasing.

- In Paper 16.1, Analog Devices presents a 16nm design that achieves a record 18GS/s with >50 dB linearity. It achieves 48dB SNDR and 54dB SFDR for an 8GHz signal sampled at 18GS/s. This performance is enabled by a wideband track-and-hold amplifier and extensive background calibration.
- In Paper 16.2, University of Macau presents a 65nm 8b 10GS/s 4× time-interleaved time-domain pipeline ADC using 16× interpolation-based inter-stage gain. It achieves 37.6dB SNDR for an 18GHz input signal sampled at 10GS/s while consuming 50.8mW.
- In Paper 16.3, University of Macau presents a 6b 3.3GS/s single-channel pipeline ADC in 28nm. It uses a look-ahead pipeline scheme to allow amplification and comparison to happen at the same time and achieves 34.2dB SNDR for a Nyquist input at 3.3GS/s with 5.5mW of power.
- In Paper 16.4, National Cheng Kung University presents a weighted-averaging correlated level shifting technique for a 14b pipelined SAR manufactured in 28nm CMOS. The design achieves 71.7dB SNDR for a Nyquist input at 100MS/s and consumes only 0.7mW of power.
- In Paper 16.5, Tsinghua University presents a 13b 40MS/s ADC fabricated in 40nm CMOS. It reduces kT/C noise by sampling at the output of a preamplifier and achieves 69dB SNDR for Nyquist input at 40MS/s with an input capacitance of only 240fF and 0.59mW of power consumption.
- In Paper 16.6, Analog Devices proposes a continuous-time pipeline ADC with a VCO-based back-end and an on-chip digital reconstruction filter in 16nm FinFET. In addition to peak SNDR of 58dB in an 800MHz of bandwidth it offers 28dB inherent anti-alias filtering for 280mW of power.
- In Paper 16.7, the University of Southern California introduces a noise-shaping non-uniform sampling ADC with phase-domain level crossing and an embedded digital signal processor in 28nm. This design achieves 76.2dB SNDR in a 40MHz bandwidth while consuming a total power of 55.5mW.

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Session 16 Highlights: Nyquist and VCO-Based ADCs

[16.1] A 12b 18GS/s RF Sampling ADC with an Integrated Wideband Track-and-Hold Amplifier and Background Calibration

Paper Authors: A. Ali, H. Dinc, P. Bhoraskar, S. Bardsley, C. Dillon, M. Kumar, M. McShea, R. Bunch, J. Prabhakar, S. Puckett

Paper Affiliation: Analog Devices, Greensboro, NC

Subcommittee Chair: Michael Flynn, University of Michigan, Ann Arbor, MI

CONTEXT AND STATE OF THE ART

- High-bandwidth data converters capable of directly sampling RF signals are required for future communication, instrumentation and defense applications.
- Advanced IC technologies like 16nm FinFET CMOS offer improved bandwidth and speed, as well as allowing complex calibration at reasonable power and area.

TECHNICAL HIGHLIGHTS

- **This ADC offers an unprecedented 9GHz of Nyquist bandwidth with >50 dB linearity.**
    - A wideband track-and-hold amplifier decouples the RF sampling from quantization.
    - Extensive background calibration is used to improve linearity.
    - The converter achieves 48dB SNDR and 54dB SFDR for an 8GHz signal sampled at 18GS/s while consuming 1.3W.

APPLICATIONS AND ECONOMIC IMPACT

- The record 9GHz Nyquist bandwidth will simplify system design for wireless base-stations, instrumentation and defense applications.

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Session 17 Overview: Frequency Synthesizers and VCOs

RF Subcommittee

Session Chair: *Wanghua Wu, Samsung, San Jose, CA*

Session Co-Chair: *Jiayoon Ru, XINYI Information Technology, Shanghai, China*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF*

This session presents the latest advances in digital and analog phase-locked loops (PLLs), FMCW chirp generators, and VCOs from 5 to 60GHz for high-performance wireless applications.

- In Paper 17.1, KAIST presents a 7.7GHz ring-DCO-based digital PLL (DPLL). It achieves low in-band phase noise (-132.7dBc/Hz at 100kHz, normalized to 1GHz) and 373fs_{rms} jitter by proportional- and integral-gain co-optimization. This ring-DCO DPLL achieves a -240dB figure of merit (FoM) at 7GHz.
- In Paper 17.2, Politecnico di Milano and Infineon Technologies demonstrate a fractional-N bang-bang PLL in 28nm CMOS. It achieves 66fs_{rms} jitter at 15GHz and performs a 1GHz hop to within 0.1% of the steady-state frequency in 18.55μs.
- In Paper 17.3, KAIST presents a 5.5GHz low-jitter fractional-N ring-oscillator-based DPLL, achieving -233.8dB-jitter FoM and worst-case fractional spurs less than -58dBc while occupying 0.1mm^2.
- In Paper 17.4, the University of Electronic Science and Technology of China describes a mm-wave multicore oscillator that achieves a 73% tuning range in 40nm CMOS. The oscillator operates from 18.6 to 40.1GHz and achieves phase noise better than -100.3dBc/Hz at a 1MHz offset while consuming less than 15mW.
- In Paper 17.5, Politecnico di Milano and Infineon Technologies present a type-I sampling PLL in 28nm CMOS, comprising a digital background phase-error corrector to enable fractional-N operation. It achieves 58 and 51fs_{rms} jitter integrated from 1kHz to 100MHz in fractional-N and integer-N modes, respectively, corresponding to FoMs of –252.1 and -253.2dB at 14GHz.
- In Paper 17.6, University College Dublin describes a charge-sharing locking technique for mm-wave quadrature frequency synthesis. It achieves 75 to 80fs_{rms} jitter over 21.7 to 26.5GHz, while consuming 16.5mW and resulting in the FoM of -250dB.
- In Paper 17.7, imec and Vrije Universiteit Brussel demonstrate a 10GHz subsampling PLL for FMCW radar, using a low-power charge-integrating DAC to tune the VCO for wideband low noise modulation. The PLL consumes 11.7mW to generate a 23.6MHz/μs chirp slope with 89kHz rms-frequency-error for a 1.21GHz chirp bandwidth.
- In Paper 17.8, KAIST describes a wide-lock-in range sub-sampling PLL (SSPLL) using an ultra-low power frequency-disturbance-correcting loop. The SSPLL achieves a lock-in range up to 340% of f_{REF}, 83fs_{rms} jitter and a -253dB FoM at 14GHz. The FCL consumes only 150μW.
- In Paper 17.9, the University of Macau demonstrates a current-mode frequency-tripling LO generator at 60GHz. It achieves 186.7dBc/Hz FoM with 9mW power consumption and utilizes a 20GHz 3rd-harmonic-rich current-output VCO, a harmonic-current filter, and a 60GHz transimpedance amplifier.

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Session 17 Highlights: Frequency Synthesizers and VCOs

[17.2] A 66fs_{rms} Jitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking

[17.5] A 12.5GHz Fractional-N Type-I Sampling PLL Achieving 58fs Integrated Jitter

Paper 17.2 Authors: *A. Santiccioli[1], M. Mercandelli[1], L. Bertulessi[1], A. Parisi[1], D. Cherniak[2], A. Lacaita[1], C. Samori[1], S. Levantino[1]*

Paper 17.2 Affiliation: [1]*Politecnico di Milano, Milan, Italy,* [2]*Infineon Technologies, Villach, Austria*

Paper 17.5 Authors: *M. Mercandelli[1], A. Santiccioli[1], A. Parisi[1], L. Bertulessi[1], D. Cherniak[2], A. Lacaita[1], C. Samori[1], S. Levantino[1]*

Paper 17.5 Affiliation: [1]*Politecnico di Milano, Milan, Italy,* [2]*Infineon Technologies, Villach, Austria*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF*

CONTEXT AND STATE OF THE ART

- Phase noise (jitter), power consumption, and silicon area are three essential design metrics that are traded off in the design of CMOS frequency synthesizers.
- Local oscillators for 5G wireless transceivers require integrated jitter below 100fs_{rms} to enable spectrally efficient modulation schemes.

TECHNICAL HIGHLIGHTS

- **Bang-bang PLL with 66fs_{rms} jitter and <20µs locking time**
  - In Paper 17.2, Politecnico di Milano presents a fractional-N bang-bang PLL in 28nm CMOS. It achieves 66fs_{rms}jitter at 15GHz with the FoM of -250.6dB and performs a 1GHz hop to within 0.1% of the steady-state frequency in 18.55µs.
- **0.16mm^2, type-I sampling PLL with 58fs_{rms} jitter**
  - In Paper 17.5, Politecnico di Milano presents a sampling PLL in 28nm CMOS, consisting of a digital background phase-error corrector to enable fractional-N operation. It achieves 58 and 51fs_{rms} jitter integrated from 1kHz to 100MHz in fractional-N and integer-N modes, respectively, corresponding to FoMs of -252.1 and -253.2dB at 14GHz.

APPLICATIONS AND ECONOMIC IMPACT

- Modern wireless communication systems demand PLLs achieving low phase noise and fast lock concurrently.
- These PLLs are among the best in class for high-performance wireless communication systems.

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Session 18 Overview: GaN and Isolated Power Conversion

Power Management Subcommittee

Session Chair: *Robert Pilawa-Podgurski, University of California, Berkeley, CA*

Session Co-Chair: *Harish K Krishnamurthy, Intel, Hillsboro, OR*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA*

GaN and isolated power converters promise higher-voltage higher-frequency power conversion in order to achieve higher power density and better end-to-end efficiency across a wide operating range of voltages and currents. At the same time, several challenges remain for implementing the perfect power converter for 110/220V AC and/or 48V DC input-voltage applications. This session aims at showcasing some of the best work in the field and addresses some of the key challenges in signal isolation for high voltage and isolated power conversion.

- In Paper 18.1, the University of Texas at Dallas presents an online r_{DS_ON} monitoring system with a fully integrated learning engine that trains itself autonomously with a prediction accuracy of <2.77%. A logarithmic expression of r_{DS_ON} and its dependency on junction temperature minimizes the circuit overhead while maintaining sufficient accuracy. The monitoring system is measured on a 9W DC-DC converter switching at 3.3MHz from 0 to 120°C.
- In Paper 18.2, Leibniz University Hannover and Texas Instruments present an offline, fully monolithic buck (step-down) power converter IC in GaN with an integrated control loop, and on-chip supply regulator for driving LED lights from grid voltages. The converter can deliver 15W of power at 30 to 60V DC, from a 60 to 400V (AC or DC) supply, with 95.6% efficiency.
- In Paper 18.3, Texas Instruments presents a 120mA offline power converter IC for low cost e-metering and other industrial applications. A synchronous bridge followed by a 4:1 charge pump reduces the amount of HV capacitance needed by 4× with lower quiescent power and no external magnetics.
- In Paper 18.4, CoilEasy Technologies and University of Electronic Science and Technology of China present a 5kV galvanically isolated DC-DC converter with an advanced micro transformer. A Leakage-Inductance Resonant Flyback is proposed to lower the frequency to 11MHz. Techniques for zero-voltage switching and avoiding a feedback device across the isolation barrier are also presented.
- In Paper 18.5, Richtek presents a zero-voltage-switching flyback-converter IC achieving a peak efficiency of 93.5% at 60W/20V/3A to optimize USB power delivery. The 2-IC controller along with an MCU employs a pulse-transformer to send signals across the isolation barrier and avoids opto-coupler drawbacks.
- In Paper 18.6, Seoul National University and Samsung Electronics present a 48V-to-1V, 60A, 3-level Half-Bridge (HB) isolated DC-DC converter. With the voltage stresses on the input side halved due to the 3-level and current-doubler rectifier topology, a peak efficiency of 92.8% is demonstrated. A 3-level HB gate driver is proposed to minimize the voltage imbalance on the flying capacitor to <1.2%.
- In Paper 18.7, Toshiba presents a fully integrated CMOS isolation amplifier that is suitable for both current and voltage sensing. With a voltage isolation of over 5kV and a 1000× bandwidth expansion over prior art, a DC-to-35.2MHz signal BW is demonstrated with 63.4mW of power consumption.
- In Paper 18.8, Toshiba presents a bi-directional full-triplex isolator with 100mW of power transfer for a gate-drive interface. Along with the power transfer, techniques to transmit at 21Mb/s and 500kb/s rates in the forward direction and 14Mb/s in the reverse direction are presented. This single-package galvanic isolator realizes full triplex communication.

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Session 18 Highlights: GaN and Isolated Power Conversion

[18.2] A Monolithic E-Mode GaN 15W 400V Offline Self-Supplied Hysteretic Buck Converter with 95.6% Efficiency

Paper Authors: *M. Kaufmann[1], Michael Lueders[2], Cetin Kaya[3], Bernhard Wicht[1]*

Paper Affiliation: *[1]Leibniz University, Hannover, Germany, [2]Texas Instruments, Freising, Germany, [3]Texas Instruments, Dallas, TX*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management Subcommittee*

CONTEXT AND STATE OF THE ART

- Size reduction and efficiency improvements are key performance drivers for power conversion. GaN technology is enabling increased switching frequency and the corresponding size reduction of power converters for a wide variety of applications.
- The integration of drivers and control circuitry on the same die as the GaN power transistor can yield both performance and cost improvements but are made difficult by the lack of PMOS devices.

TECHNICAL HIGHLIGHTS

- Leibniz University Hannover and Texas Instruments present an offline buck (step-down) power-converter IC in GaN with a fully integrated control loop and on-chip supply regulator for driving LED lights from grid voltages.
    - The converter can deliver 15W of power at 30 to 60V ac from a 60 to 400V (ac or dc) supply, with 95.6% efficiency.
    - All control, startup, and zero current detection techniques are fully integrated, enabling an ultra-compact solution.

APPLICATIONS AND ECONOMIC IMPACT

- Very small size and efficient power converter for grid connected loads, such as LED lamps.
- Fully integrated in a GaN technology, enabling high performance, cost reductions, and mass production.

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Session 19 Overview: Cryo-CMOS for Quantum Technologies

Technology Directions Subcommittee

Session Chair: Edoardo Charbon, EPFL, Switzerland

Session Co-Chair: Rabia Yazicigil, Boston University, Boston, MA

Interim Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, TD Subcommittee Chair

Cryogenic CMOS (cryo-CMOS) circuits and systems are emerging as the ideal solution to work in tandem with a variety of quantum technologies. The first paper of the session describes an IC controlling spin and superconducting qubits for a scalable, fault-tolerant quantum computer. The second paper focuses on cryo-CMOS components interfacing with a double-quantum-dot device at 110mK. The third paper proposes a digital calibration loop for an oscillator operating from 3K to 300K achieving very low frequency noise and a FOM of 200dB.

- In Paper 19.1, Delft University of Technology describes a cryo-CMOS IC designed to control spin and superconducting qubits by way of programmable waveforms from 2 to 20GHz, fabricated in Intel's 22nm FinFET technology node and operating at 3K for up to 4×32 frequency-multiplexed qubits.
- In Paper 19.2, CEA-LETI-MINATEC presents a 28nm FD-SOI CMOS chip featuring a 2.8GHz ring oscillator and an amplifier interfacing with an on-chip double quantum-dot device, all operating at 110mK.
- In Paper 19.3, Delft University of Technology proposes a digital calibration loop designed to optimize the performance of an oscillator operating from 3K to 300K. The chip, fabricated in 40nm CMOS, achieves a frequency noise of 1.6kHz and a FOM of 200dB.

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Session 19 Highlights: Cryo-CMOS for Quantum Technologies

[19.1] A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers

Paper 19.1 Authors: Bishnu Patra[1], Jeroen P.G. van Dijk[1], Sushil Subramanian[2], Andrea Corna[3], Xiao Xue[1], Charles Jeon[2], Farhana Sheikh[2], Esdras Juarez-Hernandez[2], Brando Perez-Esparza[2], Huzaifa Rampurawala[2], Brent Carlton[,2], Nodar Samkharadze[4], Surej Ravikumar[2], Carlos Nieva[2], Sungwon Kim[2], Hyung-Jin Lee[2], Amir Sammak[4], Giordano Scappucci[1], Menno Veldhorst[1], Lieven Vandersypen[1,2], Masoud Babaie[1], Fabio Sebastiano[1], Edoardo Charbon[2,5], Stefano Pellerano[3]

Paper 19.1 Affiliation: [1]Delft University of Technology, Delft, The Netherlands, [2]Intel Hillsboro, OR, [3]Zurich Instruments, Zurich, Switzerland, [3]TNO, Delft, The Netherlands, [5]EPFL Neuchatel, Switzerland.

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, TD Subcommittee Chair

CONTEXT AND STATE OF THE ART

- The core of a quantum computer is an array of quantum bits (qubits) that are controlled by bulky room-temperature instrumentation today.
- Such an implementation is not compact and may be prone to unreliable operation.

TECHNICAL HIGHLIGHTS

- **Delft University of Technology presents the first fully integrated control for spin qubits and transmons for fault-tolerant quantum computing cores.**
  - Delft University of Technology partners with Intel to deliver the first cryogenic control chip for spin and superconducting qubits implemented in 22nm FinFET CMOS technology.
  - The chip provides 2 to 20GHz control signals for up to 4×32 frequency-multiplexed qubits in a 1GHz band with 48dB SNR and 45dB SFDR.
  - Experiments show coherent spin qubit control at several frequencies.

APPLICATIONS AND ECONOMIC IMPACT

- Quantum computing holds the promise of solving some of today's intractable problems using superposition and entanglement, two important properties of quantum mechanics.
- Industry's investments in quantum computing research has led to a number of notable developments, creating significant economic activity in this field.
- It is expected that quantum computers will soon surpass classical computers in terms of computing power, thus reaching so-called quantum supremacy or quantum advantage. This chip represents an important milestone in this direction.

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Session 20 Overview: Low Power Circuits for IoT & Health

Technology Direction Subcommittee

Session Chair: Nick Van Helleputte, imec, Belgium

Session Co-Chair: Munehiko Nagatani, NTT, Japan

The push for ever lower power solutions in IoT and health applications creates unique opportunities and challenges. The first paper presents a low-power IC designed for communicating with commodity WiFi transceivers via backscattering. The second paper introduces a 54nW always-on wake-up chip for general purpose IoT devices. Next comes an electronics nose with a very accurate limit of detection. Finally, the session ends with 3D localization chip based on magnetic field gradient sensing for surgical implants.

- In Paper 20.1, the University of San Diego presents an IC with a 2.8μW wake-up receiver that can be woken up directly with a commodity Wi-Fi TRX and a 28μW SSB QBSP modulator that backscatters to a frequency-translated WiFi channel.
- In Paper 20.2, Peking University describes a software-defined always-on wake-up IC consuming just 57nW in standby-mode and increasing to 75nW average power consumption in a typical IoT application.
- In Paper 20.3, Samsung demonstrates an electronics nose with 6 integrated micro sensors based on chemically selective film on a 2.5GHz SH-SAW basis achieving 1ppm toluene gas detection and LoD of 0.02ppm.
- In Paper 20.4, California Institute of Technology describes a 3D localization system using magnetic field gradients for high-precision surgery achieving <100μm localization error.

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Session 20 Highlights: Low Power Circuits for IoT and Health

[20.1] A 28μW IoT Tag That Can Communicate with Commodity WiFi Transceivers via a Single-Side-Band QPSK Backscatter Communication Technique

Paper Authors: P.-H. Wang, C. Zhang, H. Yang, D. Bharadia, P.P. Mercier

Paper Affiliation: University of California, San Diego, CA

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions

CONTEXT AND STATE OF THE ART

- Most IoT devices need to communicate with commodity wireless infrastructure (like WiFi) to enable rapid low-cost deployment.
- However, most WiFi transceivers require 100s of mW to operate.
- This means that most WiFi-compatible IoT devices either have to have a large battery, poor battery life, or must be plugged into a wall – all of which limits use cases in which we can deploy next-generation IoT devices.

TECHNICAL HIGHLIGHTS

- **A new chip that can directly communicate with existing WiFi infrastructure at >1,000× lower power via backscatter technique.**
  - The chip takes incident WiFi signals from an existing access point or smartphone operating in a pre-specified channel and modulates this signal with a single-side-band QPSK backscatter technique onto another WiFi channel, for reception by another access point or smartphone.
  - This leads to a power consumption of 28μW, which is at least 1,000× lower power than most commercial WiFi chipsets, all while achieving a data rate of 2Mbps.

APPLICATIONS AND ECONOMIC IMPACT

- WiFi functionality can now potentially be integrated into a new class of small IoT devices that previously could not satisfy the power demands of a full WiFi transceiver.
- Since WiFi is ubiquitous, this can help enable low-cost deployment within existing infrastructure.

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Session 21 Overview: Domain-Specific Processors

Digital Architectures and Systems Subcommittee

Session Chair: Massimo Alioto, National University of Singapore, Singapore

Session Co-Chair: Ingrid Verbauwhede, KU Leuven, Belgium

Domain-specific processors continue to be applied in an ever-wider range of applications. The first paper describes an energy-efficient accelerator for low-cost genome sequencing and genetic variant discovery. The second paper presents an energy-efficient path-planning processor for autonomous navigation with low latency. The session is concluded by an image processor supporting high dynamic range for automotive applications.

- In Paper 21.1, National Taiwan University presents a genetic variant discovery SoC performing the entire next-generation sequencing for genetics research and biomedical applications. The 12mm^2 28nm engine completes the golden PrecisionFDA benchmark in 37 minutes, at a precision of 99.6% and 0.975mW power.
- In Paper 21.2, National Taiwan University introduces a path-planning processor for 2D/3D autonomous navigation. The 2.25mm^2 40nm processor supports planning tasks with up to 32,768 nodes in each dimension at 102.6mW, and in less than 0.015-to-0.125ms/task in maps with a resolution of 100-to-32,768 nodes.
- In Paper 21.3, Mediatek describes a high-dynamic-range image processor for automotive applications. The 5.69mm^2 16nm accelerator achieves 90.8dB dynamic range in a 2Mpixel frame at 30fps under 4-exposure color component fusion, consuming an energy of 0.98nJ/pixel.

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Session 21 Highlights: Domain-Specific Processors

[21.1] A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing

Paper 21.1 Authors: Yi-Chung Wu[1], Yen-Lung Chen[1], Chung-Hsuan Yang[1], Chao-Hsi Lee[2], Chao-Yang Yu[3], Nian-Shyang Chang[3], Ling-Chien Chen[3], Jia-Rong Chang[3], Chun-Pin Lin[3], Hung-Lieh Chen[3], Chi-Shi Chen[3], Jui-Hung Hung[2], Chia-Hsiang Yang[1]

Paper 21.1 Affiliation: [1]National Taiwan University, Taipei, Taiwan, [2]National Chiao Tung University, Hsinshu, Taiwan, [3]National Chip Implementation Center, Hsinshu, Taiwan

Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA

CONTEXT AND STATE OF THE ART

- Genome sequencing is computationally heavy and relies on power-hungry computing platforms that are expensive and hard to miniaturize below a benchtop form factor.
- Innovations in specialized architectures reduce cost and form factor, making DNA sequencing services more accessible.

TECHNICAL HIGHLIGHTS

- **National Taiwan University introduces a genetic variant discovery system-on-chip performing the entire next-generation sequencing for genetics research and biomedical applications, with four orders of magnitude energy efficiency improvement over GPUs on the same process node.**
    - The proposed architecture dissipates 975mW at 400MHz from a 0.9V supply, occupies 12mm^2 in 28nm CMOS, and completes the golden PrecisionFDA benchmark in 37 mins at 99.6% precision, which is in line with commercial software packages.

APPLICATIONS AND ECONOMIC IMPACT

- Energy-efficient accelerators for genome sequencing enable lower-cost computing platforms, democratizing access to DNA analysis services.
- With power consumptions in the Watt range, genome sequencing in portable systems becomes feasible.

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Session 22 Overview: DRAM and High-Speed Interfaces

Memory Subcommittee

Session Chair: Dong Uk Lee, SK hynix, Icheon, Korea

Session Co-Chair: Seung-Jun Bae, Samsung, Hwaseong, Korea

Demand for high-performance DRAM is increasing more dramatically due to the expansion of areas such as high-performance computing, 5G mobile applications and machine learning. The new devices will have a huge impact on a very wide range of applications, from high performance servers, smartphones and IoT applications. Two HBM DRAM papers of next generation show maximum data rates of 512~640GB/s, and 12Gb LPDDR5 with 8.5Gb/s/pin in a 2nd generation 10nm process node are introduced. For next-generation DRAM interfaces, a PAM-4 transceiver with 32Gb/s/pin is proposed. GDDR6 PHY with the compensation of ISI and FEXT is presented, and a quadrature-error-corrector with error range of 106ps for a DRAM interface is also presented.

- In Paper 22.1, Samsung presents a 16GB HBM2E in a 2nd-generation 10nm class DRAM process. It achieves 640GB/s with a data bus window extension technique and a synergetic on-die ECC scheme to reliably provide large capacity.
- In Paper 22.2, Samsung presents a 12Gb LPDDR5 in a 2nd-generation 10nm class DRAM process with low power and speed-boosting techniques. The 54.8mm^2 chip achieves 8.5Gb/s/pin with 0.6UI and 0.64UI of read and write DQ valid window.
- In Paper 22.3, SK Hynix presents a 16GB (16Gb 8-High TSV) HBM2E in a 1ynm DRAM process. It achieves 512GB/s with a pseudo-quarter-bank structure, a timing-based bus flip scheme and programmable memory BIST.
- In Paper 22.4, the University of Minnesota presents a single-ended PAM-4 transceiver with a 2-tap time-based decision-feedback equalizer (DFE) in a 65nm process. It achieves 32Gb/s/pin with the energy efficiency of 0.97pJ/b due to a digital-intensive time domain comparison.
- In Paper 22.5, Samsung presents a GDDR6 PHY achieving 18Gb/s/pin in an 8nm FinFET process. It achieves 0.47UI and 0.5UI of read and write IO windows at 18Gb/s with TX bandwidth extension to compensate ISI and FEXT and RX training techniques.
- In Paper 22.6, Seoul National University presents a wide-range quadrature clock edge corrector (QEC) for high-speed DRAM interfaces. It achieves a maximum output phase error of 2.18 degrees from 0.8 to 2.3GHz in a 40nm process by setting one of the delay lines in the four clock paths to the minimum delay.

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Session 22 Highlights: DRAM and High-Speed Interfaces

[22.1] A 1.1V 16GB 640GB/s HBM2E DRAM with a Data-Bus Window-Extension Technique and a Synergetic On-Die ECC Scheme

[22.2] An 8.5Gb/s/pin 12Gb LPDDR5 SDRAM with Hybrid Bank Architecture, Skew-Tolerant Scheme, Low-Power Scheme, and Speed-Boosting Techniques in 2nd-Generation of 10nm DRAM Process

Paper 22.1 Authors: Chi-Sung Oh, Ki Chul Chun, Young-yong Byun, Yong-Ki Kim, So-Young Kim, Yesin Ryu, Jaewon Park, Sinho Kim, Sanguhn Cha, Donghak Shin, Jungyu Lee, Jong-Pil Son, Byung-Kyu Ho, Seng-jin Cho, Beomyong Kil, Sungoh Ahn, Baekmin Lim, Yongsik Park, Kijun Lee, Myung-Kyu Lee, Seungduk Baek, Junyong Noh, Jae-Wook Lee, Seungseob Lee, Sooyoung Kim, Botak Kim, Seouk-Kyu Choi, Jin-Guk Kim, Hye-in Choi, Hyuk-Jun Kwon, Jun Jin Kong, Kyomin Sohn, Nam Sung Kim, Kwang-Il Park, Jung-Bae Lee,

Paper 22.1 Affiliation: Samsung Electronics, Hwaseong, Korea

Paper 22.2 Authors: Hyung-Joon Chi, Chang-Kyo Lee, Junghwan Park, Jaehoon Jung, Younghoon Cho, Dongkeon Lee, Dae-Hyun Kim, Dukha Park, Sang-Yun Kim, Jinsol Park, Sukhyun Lim, YeonKyu Choi, Yongil Lim, Cheol Kim, Jin-Hun Jang, Kiwon Park, SeungJun Lee, Su-Yeon Doo, Chang-Ho Shin, Kil-Young Kang, Byongwook Na, Jisuk Kwon, Kyung-Roun Kim, Soobong Chang, Hyein Choi, Seouk-Kyu Choi, Won-il Bae, Hyuck-Joon Kwon, Young-Soo Sohn, Seung-Jun Bae, Kwang-Il Park, Jung-Bae Lee

Paper 22.2 Affiliation: Samsung Electronics, Hwasseng, Korea

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

CONTEXT AND STATE OF THE ART

- HBM2E is a high-speed DRAM JEDEC standard on the basis of discrete components.
- LPDDR5 is a JEDEC DRAM standard on the basis of discrete components for high-speed mobile and low-power applications.

TECHNICAL HIGHLIGHTS

- **Samsung introduces a 640GB/s HBM2E DRAM, the highest bandwidth DRAM reported so far.**
    - A data bus window extension technique to cope with reduced t_{CCD}, a power delivery network design to operate at a high speed, a synergetic on-die ECC scheme to reliably provide large capacity, and an MBIST solution to efficiently test large capacity memory at high-speed.
- **Samsung introduces a 12Gb 8.5Gb/s/pin LPDDR5, the highest speed and density mobile DRAM reported to date.**
    - Hybrid bank architecture, skew-tolerant scheme, bus-based RDBI AC and speed boosting techniques. Adopting hybrid bank architecture and skew-tolerant schemes enable power-optimization depending on bank-mode in high density memories. The speed-boosting techniques provide the improved operating speed from 7.5 to 8.5Gb/s.

APPLICATIONS AND ECONOMIC IMPACT

- HBM2E is intended for use in a large variety of high-bandwidth applications such as high-performance computing, artificial intelligence, graphics, virtual reality and autonomous driving. HBM2E promises a major boost in memory bandwidth, along with a reduction in circuit board area cost reduction as well as significantly lower power consumption per bit.
- LPDDR5 provides the performance and power efficiency for the next generation 5G communication, on-device artificial intelligence and advanced driver assistance systems (ADAS), as well as for high-resolution displays and for mobile communication devices.

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Session 23 Overview: Analog Techniques II

Analog Subcommittee

Session Chair: Yiannos Manoli, University of Freiburg, Germany

Session Co-Chair: Taeik Kim, Samsung Electronics, Korea

Subcommittee Chair: Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

This session highlights advances in state-of-the-art analog techniques for various applications. The first paper introduces a 4GS/s current-domain AFE for automotive Lidar with an inaccuracy of 0.225m at ~3.5W laser peak power. A second paper describes a resistive and capacitive sensor node having an edge-encoded PWM UWB radio to provide more robust wireless transmission. The third paper presents a coulomb counter consuming an ultra-low power of less than 1μA for small inputs. Next, two Class-D amplifiers are presented, one that proposes a hybrid ΔΣ-PWM modulation scheme for high linearity and one that achieves 0.00091% THD+N at 168kHz switching frequency consuming the lowest quiescent current of 0.41mA. The following paper presents a transimpedance amplifier for ultrasound probes. The last papers introduce two amplifiers, one that achieves 130dB CMRR and another is a new dynamic amplifier with the best SFDR at Nyquist rate.

- In Paper 23.1, Robert Bosch presents a 4GS/s 80dB DR current-domain AFE for phase-coded pulse-compression direct-time-of-flight automotive LiDAR. It achieves an inaccuracy of 0.225m (1σ) over 60m range at >10× lower TX power (~3.5W).
- In Paper 23.2, the National University of Singapore presents a 70uW 1.19mm^2 wireless sensor node that uses a CDMA-like RC-to-voltage converter to simultaneously record 16-channel capacitive and 16-channel resistive sensors for electronic skins.
- In Paper 23.3, Analog Devices presents a coulomb counter. It uses dynamic biasing and duty cycling to achieve an ultra-low power consumption of less than 1μA for small inputs.
- In Paper 23.4, Delft University of Technology presents a Class-D audio amplifier with a hybrid ΔΣ-PWM modulation scheme that enables high linearity with reduced out-of-band EMI. It achieves a peak THD of -108.9dB, a THD+N of -102.2dB and can deliver 28W peak power with 91% efficiency.
- In Paper 23.5, National Cheng Kung University presents feedforward PWM aliasing cancellation with frequency equalization proposed for Class-D audio amplifiers to achieve 0.00091% THD+N while operating at 168kHz switching frequency and consuming the lowest quiescent current of 0.41mA.
- In Paper 23.6, Delft University of Technology presents a transimpedance amplifier providing 36dB continuously-variable gain for time-gain compensation in ultrasound probes. It achieves a gain error below ±1dB and a 2pA/√Hz noise floor, and consumes 4.9mW from a ±0.9V supply.
- In Paper 23.7, the University of Electronic Science and Technology of China presents a common-mode replication technique for high-CMRR amplifier design. It achieves 130dB CMRR and 50GΩ input common-mode impedance at 50Hz.
- In Paper 23.8, Yonsei University presents a new dynamic amplifier structure for high linearity. This dynamic amplifier has the best SFDR at Nyquist with 100mV_{pp} input signal. The key to this performance is to compensate the nonlinear slope factor n of the amplifiers, which limits the linearity of the amplifier.

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Session 23 Highlights: Analog Techniques II

[23.1] A 4GS/s 80dB DR Current-Domain Analog Front-End for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive LiDAR

[23.5] A 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction

[23.6] A 2pA/√Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous Time-Gain Compensation

Paper 23.1 Authors: Mahdi Kashmiri, Behnam Behroozpour, Vladimir Petkov, Ken Wojciechowski, Christoph Lang

Paper 23.1 Affiliation: Robert Bosch, Sunnyvale CA

Paper 23.5 Authors: Tai-Haur Kuo, Hung-Yi Huang, Shih-Hsiung Chien, Hong-Bin Wang, Yi-Zhi Qiu

Paper 23.5 Affiliation: National Cheng Kung University, Tainan, Taiwan

Paper 23.6 Authors: Eunchul Kang[1], Mingliang Tan[1], Jae-Sung An[1], Zu-yao Chang[1], Philippe Vince[2], Nicolas Sénégond[2], Tony Mateo[2], Cyril Meynier[2], Michiel Pertijs[1]

Paper 23.6 Affiliation: [1]Delft University of Technology, Delft, The Netherlands; [2]VERMON, Tours, France

Subcommittee Chair: Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands, Analog

CONTEXT AND STATE OF THE ART

- Paper 23.1: LiDAR enables long distance ranging at high spatial resolution and moderate computational effort. Meeting the automotive ranging requirements requires high laser peak transmit powers and low noise, high-speed receivers.
- Paper 23.5: For battery powered applications, Class-D amplifiers need to combine low quiescent current and low switching losses for extending battery life while maintaining low THD+N.
- Paper 23.6: In-probe ASICs to interface with ultrasound transducer arrays improve signal quality and reduce cable count. Low power consumption and low noise operation are key requirements.

TECHNICAL HIGHLIGHTS

- **Robert Bosch introduces a 4GS/s 80dB DR Current-Domain Analog Front-End for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive LiDAR.**
  - This Current-domain AFE enables the use of pulse compression techniques. With >80dB no-clipping DR, its highly oversampled 4GS/s ADC output is match-filtered against phase-coded TX bursts, achieving 0.225 meter inaccuracy at >10× lower laser peak power (3.5W) in a 60 meter range.
- **The National Cheng Kung University presents a 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction.**
  - Compared with the state of the art, this work implemented in cost-effective 0.5μm CMOS technology reduces the quiescent current consumption by more than 50%, while still achieving the competitive THD+N of 0.00091%.
- **Delft University of Technology presents a 2pA/√Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous Time-Gain Compensation.**

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- The presented TIA has a 36dB linear-in-dB variable gain range. The TIA serves as an LNA with embedded time-gain compensation for miniature ultrasound probes, reducing the output DR and saving power. Compared to prior TIAs with discrete gain steps, imaging artifacts associated with gain switching are avoided.

APPLICATIONS AND ECONOMIC IMPACT

- Autonomous driving requires high spatial resolution. It is forecasted that within 10 years most cars will be equipped with enabling sensors. LiDAR is an important component in the Advanced Driver-Assistance Systems (ADAS) landscape.
- The main applications of Class-D amplifiers are in mobile/battery powered scenarios. The multichannel audio systems of most modern vehicles also rely on highly efficient Class-D amplifiers.
- Disposable ultrasound probes enable low-cost diagnostics with higher resolution.

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Session 24 Overview: RF and mm-Wave Power Amplifiers

RF Subcommittee

Session Chair: Swaminathan Sankaran, Texas Instruments, Dallas, TX

Session Co-Chair: Yves Baeyens, Nokia – Bell Laboratories, New York, NY

PAs are critical building blocks that govern the output power, energy-efficiency, and linearity of transceiver front-ends. Linear, high-efficiency, high-output-power PAs covering various frequency bands for RF/mm-wave communication and sensing are presented. The first three papers in this session cover PAs for 5G bands at 28/39GHz. The next two present sub-6GHz PAs with high P_{OUT}, low EVM, and high efficiency. The session continues with two papers showing progress in ultra-broadband (26 to 40GHz) and D-band CMOS PAs. The session concludes with an efficient, 6W W-band GaN PA operating close to 100GHz.

- In Paper 24.1, the Georgia Institute of Technology presents a watt-level, 24-to-30GHz broadband linear Doherty PA with novel power combining to support multi-Gbps 5G NR.
- In Paper 24.2, the Georgia Institute of Technology demonstrates a 39GHz reconfigurable Doherty amplifier in 45nm SOI CMOS with strong resilience to antenna impedance variations.
- In Paper 24.3, the Georgia Institute of Technology presents a 28GHz, current-mode, inverse-outphasing, 5G 64-QAM transmitter supporting 15Gbps and 40/31% at P_{sat}/6dB back-off.
- In Paper 24.4, Michigan State University demonstrates a watt-level 2.4GHz digital polar PA using 65nm CMOS. The PA achieves 30dBm peak output power and excellent EVM and drain efficiency at various back-offs.
- In Paper 24.5, Fudan University presents a wideband wireless PA based on a 15b quadrature digital PA in 55nm CMOS. The chip achieves 24.4% PAE at 23.6dBm of average output power for LTE 64-QAM modulation.
- In Paper 24.6, the Georgia Institute of Technology presents an ultra-compact, broadband linear 5G PA in 45nm SOI CMOS process that achieves >17.8dBm P_{1dB} with >36.6% PAE from 24 to 40GHz.
- In Paper 24.7, KU Leuven introduces a D-band (135GHz) power amplifier in 16nm FinFET CMOS. A peak gain of 25.6dB, P_{sat} of 15dBm, and peak PAE of 11.7% are realized.
- In Paper 24.8 Tianjin University demonstrates a W-band PA with output power of 6W and 18% PAE fabricated in a 100nm GaN HEMT technology.

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Session 24 Highlights: RF and mm-Wave Power Amplifiers

[24.2] A Reconfigurable Series/Parallel Quadrature-Coupler-Based Doherty PA in CMOS SOI with VSWR Resilient Linearity and Back-Off PAE for 5G MIMO arrays

[24.7] A 15 dBm, 12.8%-PAE Compact D-band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS

Paper 24.2 Authors: N. Sasikanth Mannem, M-Y. Huang, T-Y. Huang, H. Wang

Paper 24.2 Affiliation: Georgia Institute of Technology, Atlanta, Georgia

Paper 24.7 Authors: B. Philippe, P. Reynaert

Paper 24.7 Affiliation: [1]KU Leuven, Heverlee, Leuven, Belgium

Subcommittee Chair: Piet Wambacq, imec, Belgium

CONTEXT AND STATE OF THE ART

- High-power and efficient PAs under saturated and back-off conditions with high EVM and VSWR resilience enable optimal RF/mm-wave system performance required in existing and emerging applications, such as 5G/higher-frequency (sub 6GHz and 28/39GHz) communications and high-resolution imaging/sensing.
- VSWR unpredictability with non-ideal and variable antenna impedance resulting from antenna-array beam steering has been a fundamental limitation in achieving high performance with reliable operation.
- Techniques and innovation in alternate topologies leverage multiple efficiency peaks
- Efficient, passive and co-optimized active-passive power combining allows improvement over existing state of the art while scaling down with technology.

TECHNICAL HIGHLIGHTS

- **The Georgia Institute of Technology presents a PA with VSWR-resilient linearity and PAE in back-off suitable for 5G MIMO arrays.**
  - A reconfigurable series/parallel quadrature-coupler-based Doherty PA with 21dBm P_{OUT}, providing 3:1 VSWR resilience with <1.7dB degradation in OP_{1dB} compared to 3 to 5dB typical of traditional Doherty PAs.
- **KU Leuven introduces a D-Band (135GHz) power amplifier in 16nm FinFET CMOS demonstrating state-of-the-art performance.**
  - A 3-stage two-way power-combining power amplifier operates at 135GHz, achieves a peak gain of 25.6dB, P_{SAT} of 15dBm, and a peak PAE of 11.7%, while occupying just 0.062mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced active/passive and power-combining circuit techniques for high-power, high-efficiency PAs make many new green/efficient applications possible.
- Improved robustness to VSWR increases cost efficiency by enabling reliable operation.

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Session 25 Overview: Digital Power Delivery & Clocking Circuits

Digital Circuits Subcommittee

Session Chair: Keith Bowman, Qualcomm, Raleigh, NC

Session Co-Chair: Yvain Thonnart, CEA-Leti, Grenoble, France

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits Subcommittee

In this session, nine papers highlight developments in digital power delivery and clocking circuits. For power delivery, three digital low-dropout (DLDO) voltage-regulator papers demonstrate: 1) a distributed design with a digital supply voltage sensor and PID-based controller for a wide-load current range; 2) a comparator-triggered oscillator and droop detector for fast-transient response; and 3) an edge-chasing quantizer and a resistance randomizer for side-channel-attack tolerance. In a fourth paper, related to power delivery, an on-die power-supply noise analyzer reduces measurement time with compressed sensing. For clocking circuits, two papers demonstrate: 1) a self-calibrated synthesized fractional-N MDLL; and 2) a sub-sampling PLL with frequency shaping. The last three papers present: 1) a time-borrowing fast mux-D scan flip-flop; 2) a GALS NoC with metastability error detection and correction; and 3) a reconfigurable transient current-mode repeater for on-die global interconnects.

- In Paper 25.1, Intel presents a synthesizable distributed DLDO system with a digital supply voltage sensor and a digital PID-based controller with no external capacitor in 10nm CMOS at 0.0144mm^2 per DLDO. Measurements demonstrate stable voltage regulation for load current ranging from 0.028A to 2.74A with peak current efficiency of 98.6%.
- In Paper 25.2, Seoul National University describes a synthesizable DLDO in 28nm with a comparator-triggered oscillator and droop detector for fast-transient response in 0.049mm^2 without an external output capacitor. Measurements indicate a 112mV voltage droop for a 430mV load-current step with a 2ns rise time.
- In Paper 25.3, Rice University presents a DLDO in 65nm with an edge-chasing quantizer and a resistance randomizer for side-channel-attack tolerance. Measurements indicate an increase in the minimum traces to disclosure (MTD) of more than of 6000× with a current efficiency of 99.4% and an area of 0.018mm^2.
- In Paper 25.4, the University of Electronic Science and Technology of China describes a 20GHz on-die power-supply noise analyzer with compressed sensing to reduce the measurement time in 40nm CMOS. Measurements highlight the benefits of compressed sensing and indicate a 200× faster measurement time, while improving the sampling rate, resolution, and noise floor as compared to state-of-the-art.
- In Paper 25.5, Intel presents a 1.2-to-3.8GHz self-calibrated synthesized fractional-N MDLL with a self-calibrated DTC in 22nm FinFET CMOS. Measurements demonstrate spurs below -50dBc and the reference spur at -56dBc. Integrated RMS jitter is 2.74ps dissipating 3.19mW at 3.6GHz with an area of 0.0052mm^2.
- In Paper 25.6, National Taiwan University describes a 5.25GHz sub-sampling PLL with frequency shaping in 40nm CMOS in 0.161mm^2. Measurements demonstrate phase noise at -95.6dBc/Hz at 1MHz offset and integrated RMS jitter at 1.95ps.
- In Paper 25.7, Intel introduces a time-borrowing fast mux-D scan flip-flop in 10nm CMOS, exploiting the timing advantages of a level-sensitive scan design. Measurements demonstrate that inserting the flip-flop in critical paths improves a 2GHz processor block performance by 7.2% at 650mV.
- In Paper 25.8, Shanghai Jiao Tung University and Columbia University demonstrate a GALS NoC in 65nm CMOS with metastability error detection and correction. Measurements demonstrate the design supporting four voltage/frequency domains with a wide operating range from 0.4V at 7.3MHz to 1V at 175MHz.
- In Paper 29.9, Intel introduces a reconfigurable repeater to operate in either current mode or voltage mode in 10nm CMOS for on-die global interconnects at high-performance operation. Measurements demonstrate an 8× increase in the repeater distance, as compared to an optimally designed conventional repeater.

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Session 25 Highlights: Digital Power Delivery & Clocking Circuits

[25.1] A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS

[25.5] A Self-Calibrated 1.2-to-3.8GHz 0.0052mm² Synthesized Fractional-N MDLL Using a 2b Time-Period Comparator in 22nm FinFET CMOS

Paper 25.1 Authors: *S. Bang, W. Lim, C. Augustine, A. Malavasi, M. Khellah, J. Tschanz, V. De*

Paper 25.1 Affiliation: Intel, Hillsboro, OR

Paper 25.5 Authors: S. Kundu, L. Chai, K. Chandrashekar, S. Pellerano, B. Carlton

Paper 25.5 Affiliation: Intel, Hillsboro, OR

Subcommittee Chair: Edith Beigné, Facebook, Menlo Park, CA, Digital Circuits Subcommitee

CONTEXT AND STATE OF THE ART

- Fully synthesizable design solutions show benefits of easy portability and reduced design effort. One key challenge comes from stringent gain and linearity requirements of digital-to-time converters (DTC) or time-to-digital converters (TDC), where digital standard cells are used for analog functionality.
- Integrated LDOs cost effectively enable fine-grain voltage regulation for digital IP blocks. Large IPs create challenges for collaboration among distributed LDOs to regulate a single domain.
- Increasing speed and complexity of modern SoCs demands low-jitter clock generators. Digital multiplying delay-locked loops (MDLLs) or injection-locked phase-locked loops (IL-PLLs) using ring oscillators are preferred due to their small form factor and superior jitter performance.

TECHNICAL HIGHLIGHTS

- **Intel introduces a tileable synthesized distributed digital LDO voltage regulator in 10nm CMOS achieving fast single-cycle voltage monitoring and control compatible with automated placement and routing flows**
  - A 0.014mm² all-digital LDO unit sustaining 0.27A transients within a 0.25mm² tile is integrated in a 9-tile autonomous distributed regulation scheme with fast local recovery using a reference-less digital supply voltage sensor. The system achieves at most 200mV droop for a 1.17A transient for 98.6% peak current efficiency.
- **Intel presents a synthesized Fractional-N MDLL suppressing reference/fractional spurs without any calibration using a 2b time-period comparator for phase detection and a DTC with replica DCO for fractional-N operation.**
  - A 22nm FinFET chip shows 1.8× higher operating frequency, 2× better power efficiency, and a superior FoM compared to the state-of-the-art synthesized fractional-N clock generators.

APPLICATIONS AND ECONOMIC IMPACT

- Tight point-to-load voltage regulation on a shared power delivery network improves local IR-drop and transient droop response across small or large IP domains in a scalable scheme.
- Ring-oscillator-based fractional MDLLs suitable for modern SoCs save silicon area significantly compared to LC-based designs.
- Synthesizable solutions further provide portability and reduce design effort for reduced time-to-market.

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Session 26 Overview: Biomedical Innovations

Imagers, Medical, MEMS and Display Subcommittee

Session Chair: Jerald Yoo, National University of Singapore, Singapore

Session Co-Chair: Esther Rodriguez Villegas, Imperial College, London, UK

Both sensor and actuator systems for on-body wearable and in-body implantable usage continue to evolve towards more robust, functionally complex, and energy-efficient solutions, as well as closed-loop operation. This session presents recent biomedical innovations on multimodal sensing of physiological signals in both the wearable and implantable contexts, multimodal and closed-loop neuromodulation SoCs with stimulus artifact resiliency, and biosensors for rapid detection of drugs in whole blood.

- In Paper 26.1, MediaTek describes a multi-modal biosensing SoC for PPG, ECG, BIOZ and GSR acquisition. Targeting consumer wearable devices, the SoC in 55nm CMOS consumes 72μW, achieving 130dB dynamic range.
- In Paper 26.2, the University of Toronto presents a neuromorphic SoC that features a multiplier-less 1024-tree brain-state classifier and neuromodulator for online epileptic seizure remediation. The SoC in 65nm CMOS closes the loop with neurostimulators upon detection of a seizure onset, consuming 36nJ/classification.
- In Paper 26.3, Xi'an Jiaotong University shows an 8-channel closed-loop neuromodulation chipset for seizure detection. The two-die chipset in 0.18μm features 2-level classification with 1.5Vpp common-mode cancellation.
- In Paper 26.4, Stanford University presents a chronoamperometry biosensor to measure small molecule drugs in whole blood. Implemented in 65nm CMOS, the sensor achieves a minimum IRN of 15.2pA_{rms} at 2.5kHz bandwidth and consumes 0.22mW at 5Hz data acquisition rate.
- In Paper 26.5, Oregon State University introduces a fully integrated, battery-less heartbeat monitor that performs motion-resilient heartbeat detection from two-electrode ECG. The IC fabricated in 180nm CMOS demonstrates the self-sustaining system powered by human body heat.
- In Paper 26.6, Yonsei University describes a Continuous-Time $\Delta\Sigma$ Modulator for closed-loop neural recording. The modulator with G_m-input achieves 300mV_{pp} linear input range and 80.4dB SNDR, consuming 6.5μW with a signal BW of 10kHz, exhibiting 172.3dB FoM.
- In Paper 26.7, Case Western Reserve University presents a readout IC that integrates a dual-output regulating rectifier with a direct light-to-digital converter for implantable PPG recording. The IC features wireless capacitive powering with peak PCE of 90.7% at 5MHz. The 3×4mm^2 IC in 0.18μm CMOS consumes 15.7μW from 1.5V for subcutaneous PPG recording.
- In Paper 26.8, North Carolina State University presents a trimodal neural interface SoC with 16 optical and 8 electrical stimulation channels. A 16-channel AFE provides 55-to-70dB gain and 1-to-100Hz low cutoff with 3.46μV_{rms} input-referred noise. The SoC in 0.35μm receives >20.7mW via a 13.56MHz inductive link, which also carries forward data at 50kb/s.
- In Paper 26.9, the University of Michigan presents a 0.74μW 0.19×0.17mm^2 IC for a wireless neural recording probe with NIR-based power and data telemetry. It computes Spiking Band Power (SBP) on-chip to save power by 920× and demonstrates accurate finger position and velocity decoding.

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Session 26 Highlights: Biomedical Innovations

[26.1] A 4.5mm² Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR Acquisition in Consumer Wearable Devices

[26.2] A Neuromorphic Multiplier-Less Bit-Serial Weight-Memory-Optimized 1024-Tree Brain-State Classifier and Neuromodulation SoC with an 8-Channel Noise-Shaping SAR ADC Array

[26.6] A 6.5μW 10kHz-BW 80.4dB-SNDR Continuous-Time ΔΣ Modulator with G_m-Input and 300mV$_{pp}$ Linear Input Range for Closed-Loop Neural Recording

Paper 26.1 Authors: Yun-Shiang Shu, Zhi-Xin Chen, Yu-Hong Lin, Su-Hao Wu, Wei-Hsiang Huang, Albert Yen-Chih Chios, Chang-Yang Huang, Hung-Yi Hsieh, Fan-Wei Liao, Tneg-Feng Zhou, Ping Chen

Paper 26.1 Affiliation: MediaTek, Hsinschu, Taiwan

Paper 26.2 Authors: Gerard O'Leary[1], Jianxiong Xu[1], Liam Long[1], Jose Sales Filho[1], Camilo Tejeiro[1], Mateu ElAnsary[1], Chenxi Tang[1], Horneira Moradi[2], Prajay Shah[1], Taurinos A. Valiante[3], Roman Genov[1]

Paper 26.2 Affiliation: [1]University of Toronto, Toronto, Canada, [2]Krembil Neuroscience Center, Toronto, Canada, [3]Toronto Western Hospital, Toronto, Canada.

Paper 26.6 Authors: Changuk Lee[1], Taejune Jeon[1], MoonHyung Jang[1], Sanggeon Park[2], Yeowool Huh[3], Youngcheol Chae[1]

Paper 26.6 Affiliation: [1] Yonsei University, Seoul, Korea, [2] University of Science and Technology, Daejeon, Korea, [3] Catholic Kwandong University, Incheon, Korea.

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium.

CONTEXT AND STATE OF THE ART

- Physiological signal acquisition in wearable consumer devices suffers from degraded signal quality due to poor sensor interfaces, motion artifacts and environmental interference. These challenges result in demanding AFE specifications, under tight area and power constraints.
- Future medical brain implants for neuromodulation will require accurate, energy-efficient brain state classifiers to determine the precise instants when stimulation should be delivered to maximize the efficacy of the neuromodulation treatment.
- Closed-loop neural recording requires a front-end with wide dynamic range to record very small signals without distortion in the presence of DC electrode offset and large stimulation artifacts.

TECHNICAL HIGHLIGHTS

- **MediaTek introduces an SoC for multimodal PPG, ECG, GSR and BIOZ recording in 55nm CMOS with enhanced PPG dynamic range and resilience to interference for 2-channel ECG.**
  - Improvements with respect to the state of the art include: over 10dB larger dynamic range in PPG; 3× higher resilience to power line interference in 2-channel ECG; 10× smaller electrodes for body-fat measurements; and over 50% reduction in overall area.
- **The University of Toronto, Krembil Neuroscience Centre and Toronto Western Hospital introduce a neuromorphic 1024-tree brain state classifier and neuromodulation SoC with an 8-channel noise-shaping SAR ADC array.**

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- Neuromorphic feature extractors reduce ADC resolution requirements to 6b. The BrainForest classifier achieves a sensitivity of 96.7% in the detection of epileptic seizures, and a false detection rate of 0.8 occurrences per hour, consuming 36nJ/classification.

- **Yonsei University, the University of Science and Technology and Catholic Kwandong University present a Continuous Time ΔΣ modulator with improved linear input range for closed-loop neural recording.**
  - Using a Gm-input for the closed-loop neural recording, the modulator achieves 300mV_{pp} linear input range, in excess of 80SNDR, and 76dB CMRR, consuming 6.5μW with a signal bandwidth of 10kHz.

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APPLICATIONS AND ECONOMIC IMPACT

- Epilepsy is a neurological disease affecting up to ~1% of the population, and is characterized by debilitating seizures. The annual cost associated with epilepsy in the US is estimated to be $12.5 billion. A disproportionate amount of such cost arises as a result of poor seizure control.
- The market size of health-related wearables is estimated to be $7B USD, and expected to grow to $27.5B by 2026, driven by healthcare providers shifting towards wireless connectivity, combined with demographic trends and a higher incidence of chronic diseases.

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Session 27 Overview: IoT and Security

Digital Architectures and Systems Subcommittee

Session Chair: Hirofumi Shinohara, Waseda University, Fukuoka, Japan

Session Co-Chair: James Myers, Arm Ltd, Cambridge, UK

Pervasive IoT applications demand increasingly efficient and secure circuits and systems. The first paper is a 65nm battery-less sub-threshold microcontroller integrated into a commercial machine health-monitoring sensor node. The second paper is another 65nm sub-threshold microcontroller, this time with SIMD support and wide-range DVFS. The third and fourth papers focus on two aspects of hardware security: 1) attack resistance, and 2) key generation. The third paper offers new approaches which make EM and power attacks significantly more difficult. The fourth paper tailors a Physically Unclonable Function for low-error-rate key generation satisfying automotive reliability requirements.

- In Paper 27.1, Everactive and Analog Devices present a battery-less sub-threshold Cortex-M0 32KHz-to-7MHz 65nm microcontroller with multi-mode energy harvesting and an 83% efficient integrated voltage regulator, with -54dBm sensitivity wake-up radio, achieving average sensor node platform power of 89.1μW.
- In Paper 27.2, Arm details a sub-threshold Cortex-M33 65nm 0.8-to-38MHz microcontroller with 10nW shutdown power and down to 10.9pJ/cycle active energy, demonstrating keyword spotting at 47μW.
- In Paper 27.3, Purdue University addresses both EM and power side-channel attacks in a 0.15mm^2 AES-256 implementation with a current-domain signature attenuation circuit and local lower metal routing in 65nm CMOS.
- In Paper 27.4, Samsung Electronics presents a Physically Unclonable Function for a secure 256b key generation in a 28nm FDSOI process achieving error rate of 1.41E-64 across conditions of -40 to 150°C and 15 years aging, satisfying AEC-Q100 Grade 1 reliability and ISO26262 ASIL-B assessment with 97.76% fault coverage.

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Session 27 Highlights: IoT and Security

[27.1] A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an 89.1µW Continuous Machine Health Monitoring Wireless Self-Powered System

[27.4] Physically Unclonable Function in 28nm FDSOI Technology Achieving High Reliability for AEC-Q100 Grade 1 and ISO26262 ASIL-B

Paper 27.1 Authors: Jonathan K. Brown[1], David Abdallah[2], Jim Boley[3], Nicholas Collins[1], Kyle Craig[2], Greg Glennon[2], Kuo-Ken Huang[3], Christopher J. Lukas[2], William Moore[3], Richard K. Sawyer[2], Yousef Shakhsheer[2,4], Farah B. Yahya[2], Alice Wang[3], Nathan E. Roberts[2], David D. Wentzloff[1], Benton H. Calhoun[2]

Paper 27.1 Affiliation: [1]Everactive, Ann Arbor, MI, [2]Everactive, Charlottesville, VA, [3]Everactive, Santa Clara, CA, [4]Analog Devices, Fort Collins, CO

Paper 27.4 Authors: Yunhyeok Choi, Bohdan Karpinskyy, Kyoungmoon Ahn, Soonkwan Kwon, Yongsoo Kim, Jieun Park, Yongki Lee, Mijung Noh

Paper 27.4 Affiliation: Samsung Electronics, Hwaseong, Korea

Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA

CONTEXT AND STATE OF THE ART

- Energy harvesting may be used to extend or replace batteries in Internet-of-Things (IoT) applications, such as industrial monitoring, precision agriculture, home automation and smart cities, but has not yet seen wide adoption due to system challenges of operating from variable and limited output power.
- Security is a key requirement of both IoT and automotive applications, and Physically Unclonable Functions (PUFs) for secure key generation are gaining attention, but require bit-error-rate reductions to almost zero, while satisfying the high reliability requirements needed for automotive applications.

TECHNICAL HIGHLIGHTS

- **Everactive and Analog Devices introduce an energy-harvesting SoC for battery-less health monitoring of industrial machinery used in a commercial sensor node.**
    - A sub-threshold Cortex-M0 and 256kB SRAM operate from an 83% efficient integrated voltage regulator at 32kHz-to-7MHz, with a -54dBm sensitivity wake-up radio, achieving average platform power of 89.1µW.
- **Samsung Electronics introduces a low-bit-error rate and high-reliability PUF in 28nm FDSOI technology.**
    - The PUF satisfies both AEC-Q100 Grade 1 reliability and ISO26262 ASIL-B assessment with 97.76% fault coverage using safety mechanisms, while achieving a bit error rate of 1.41E-64 across conditions of -40 to 150°C and 15 years aging.

APPLICATIONS AND ECONOMIC IMPACT

- Frequent battery replacements pose an economic obstacle to trillions of IoT devices, which must be overcome by extreme energy efficiency and/or energy harvesting.
- Exploits of automotive security vulnerabilities have been widely publicized and present a high risk of theft and to driver safety.

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Session 28 Overview: User Interaction and Diagnostic Technologies

IMMD Subcommittee

Session Chair: Masayuki Miyamoto, Wacom Co, Ltd., Tokyo, Japan

Session Co-Chair: Johan Vanderhaegen, Google, Mountain View, CA

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium, IMMD

Capacitive touch sensing is one of the key evolving user-interaction technologies. The first paper introduces a technique to resolve the signal saturation problem inherent to mutual-capacitance sensing using multiple frequencies. The second paper proposes a simple circuit architecture for self-capacitance sensing of in-cell touch displays. In the third paper, a wafer-scale X-ray detector stitched from detector and read-out sub-chips is presented, with applications in medical and industrial diagnostics. The session finishes with a combined electrochemical and impedance characterization array IC.

- In Paper 28.1, Delft University of Technology, SK Hynix, and Leading UI propose a capacitive touch analog front-end which employs an amplitude-modulation technique to reduce charge overflow associated with multi-frequency excitation by 33.9dB. The measured SNR is 41.7dB for a 1mm metal pillar and 61.6dB for a 10mm finger.
- In Paper 28.2, Sentron introduces a simple shunts-sensing analog front-end achieving 51dB SNR at 120Hz for segmented-VCOM LCD in-cell touch-display.
- In Paper 28.3, Yonsei University presents a 12-inch CMOS X-ray detector with a 5.2Mpixel array and 16b column-parallel continuous-time incremental $\Delta\Sigma$ ADCs. The detector achieves 88.4dB dynamic range at 30fps.
- In Paper 28.4, Georgia Institute of Technology presents a CMOS multi-modality electrochemical and impedance cellular sensing array, for synthetic exoelectrogen characterization.

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Session 28 Highlights: User Interaction and Diagnostic Technologies

[28.3] A 5.2Mpixel 88.4dB-DR 12in CMOS X-Ray Detector with 16b Column-Parallel Continuous-Time ΔΣ ADCs

Paper Authors: Sangwoo Lee, Jinwoong Jeong, Taewoong Kim, Chanmin Park, Taewoo Kim, Youngcheol Chae

Paper Affiliation: Yonsei University, Seoul, Korea

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

CONTEXT AND STATE OF THE ART

- X-ray detectors are used in medical and industrial applications, such as Computed Tomography (CT), non-destructive test, and radiography.

TECHNICAL HIGHLIGHTS

- **The detector combines an area- and energy-efficient 3rd-order incremental ΔΣ ADC with a voltage-controlled storage capacitor.**
    - The detector array is realized in a 1P4M 65nm CMOS technology. The 5.2Mpixel array achieves 88.4dB DR at 30fps, consuming 3.9W.
- **The pixel array is implemented with 12×12 sub-chips, each containing 192×188 pixels. 12 readout sub-chips provide the 4608 readouts. In total, 169 sub-chips are stitched on a wafer and constitute a single detector. A scintillator is realized on the detector using a direct growth technology. The detector size is 20.7×20.7cm^2.**

APPLICATIONS AND ECONOMIC IMPACT

- The X-ray detector functionality has been demonstrated using a hand phantom for Computed Tomography (CT), an automotive part for non-destructive test, and radiography.

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Session 29 Overview: Emerging RF and THz Techniques

RF Subcommittee

Session Chair: Hua Wang, Georgia Institute of Technology, Atlanta, GA

Session Co-Chair: Shuhei Amakawa, Hiroshima University, Hiroshima, Japan

The papers of this session highlight diverse circuit techniques that advance the state of the art in RF and THz. A highly integrated 8×8 radiator array for THz imaging with a single-pixel camera is presented. The following three papers describe THz radiator arrays. The session continues with a magnet-free isolator, a notch filter, a chip-scale molecular clock that locks onto the rotational transition of carbonyl sulfide (OCS), a THz receiver based on frequency-locked loops (FLL) with a wide acquisition range, and a cryptographic ID tag operating at 260GHz.

- In Paper 29.1, the University of Wuppertal describes an 8×8-pixel computational THz imaging source array. The source is reconfigurable with spatial and frequency modulation diversity, and it radiates up to 9.2dBm power at 0.42THz with a 2MHz pattern repetition rate.
- In Paper 29.2, KU Leuven presents a 0.59THz beam-steerable coherent radiator array in 40nm CMOS. It combines 36 coherent radiators within $0.68mm^2$, achieving 1mW radiated power, and 24.1dBm EIRP at 586.7GHz with a ±15° beam-steering range in the E-plane.
- In Paper 29.3, Columbia University shows a 1GHz circulator in 0.18µm SOI CMOS that exhibits 2.07/2.49dB TX-ANT/ANT-RX insertion loss and +34dBm TX-ANT P_{1dB} of 104mW power consumption using a switched-capacitor clock-boosting technique. It includes built-in antenna-tuning circuitry that provides isolation across 2.33:1 ANT VSWR.
- In Paper 29.4, Columbia University reports an N-path switched-capacitor notch filter with 50dB maximum rejection and an RF isolator with 1.1-to-2dB insertion loss, both over 0.2 to 1GHz.
- In Paper 29.5, MIT introduces a 70mW, chip-scale molecular clock (CSMC) probing the 231.06GHz rotation transition of carbonyl sulfide (OCS). Using high-order dispersion curve locking, the CSMC achieves a temperature stability of ±3ppb over 27 to 65°C and a magnetic sensitivity of ±2.9ppt/Gauss.
- In Paper 29.6, KU Leuven describes a 4×2 array of THz self-oscillating sources in 40nm CMOS. It operates across 660 to 676GHz and achieves a maximum EIRP of 7.4dBm and -93dBc/Hz phase noise at a 10MHz offset, while consuming 99.7mW.
- In Paper 29.7, KAIST presents a 490GHz receiver in 65nm CMOS with a dual-locking FLL. The receiver only dissipates 32mW from a 1.2V supply.
- In Paper 29.8, MIT presents a $1.6mm^2$ 260GHz cryptographic ID tag with 30° beam-steering capability. A light harvester powers the chip via on-chip photodiodes. The tag includes a low-power (14.4 µJ/ECSM) elliptic curve cryptography (ECC) accelerator supporting private identification protocols.
- In Paper 29.9, Princeton University demonstrates a 4×4 source array in 65nm CMOS with a distributed oscillating network at 69.3GHz. Local harmonic generation produces -3dBm radiated power and +14dBm EIRP at 416GHz. The array chip achieves ±30° beam-steering in both X- and Y-planes.

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Session 29 Highlight: Emerging RF and THz Techniques

[29.1] A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging

Paper Authors: Ritesh Jain, Philipp Hillger, Janusz Grzyb, Ullrich R. Pfeiffer

Paper Affiliation: University of Wuppertal, Wuppertal, Germany

Subcommittee Chair: Piet Wambacq, imec, Heverlee, Belgium, RF

CONTEXT AND STATE OF THE ART

- Various applications, such as sensing and 5G+/6G communication, are driving the need for high-power, efficient, and small-form-factor sub-mm-wave and THz signal sources in commercially available technologies.
- THz sensing and imaging applications also demand novel and simple system configurations.

TECHNICAL HIGHLIGHTS

- **A highly integrated THz radiator array supports imaging with a single-pixel detector.**
  - The 8×8 source array is fully reconfigurable with spatial and frequency modulation diversity, enabling the application of compressed sensing techniques.
  - The source array radiates up to 9.2dBm power and 32.8dBm EIRP at 0.42THz with a 2MHz pattern repetition rate.

APPLICATIONS AND ECONOMIC IMPACT

- Potentially enabling portable or even handheld THz imaging devices for a wide variety of applications, including non-destructive evaluation, material characterization, and medical diagnostics.

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Session 30 Overview: Efficient Wireless Connectivity

Wireless Subcommittee

Session Chair: Yao-Hong Liu, imec-Netherlands, The Netherlands

Session Co-Chair: Yuu Watanabe, Waseda University, Japan

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR

Wireless connectivity remains the key enabler for various Internet of Things (IoT) applications. The first paper describes a 27.6nW temperature-robust wake-up receiver. The following two papers present highly integrated narrowband-IoT (NB-IoT) transceiver SoCs for long-range IoT connectivity, while the short-range connectivity with diverse requirements (low-power, low-voltage, accurate ranging and cost-efficient crystal-less) is addressed by four Bluetooth Low Energy (BLE) radios. Finally, an area-efficient miniature Medical-Implantable-Communication-Services (MICS) transceiver showcases the in-body connectivity.

- In Paper 30.1, the University of Virginia presents a temperature-robust 27.6nW wakeup receiver at 9.6GHz X band. It achieves -65dBm sensitivity with <2dB degradation across the temperature range.
- In Paper 30.2, Samsung Electronics reveals an NB-IoT and GNSS all-in-one System-on-Chip, integrating RF transceiver, 23dBm CMOS power amplifier, power management unit, and clock management system for a low-cost solution.
- In Paper 30.3, Hong-Kong Applied Science and Technology shows a SAW-less NB-IoT RF transceiver with hybrid polar and on-chip switching PA supporting Power Class 3 multi-tone transmission.
- In Paper 30.4, the University of Twente and Analog Devices present a 370µW, 5.5dB NF BLE/BT5.0/IEEE 802.15.4-compliant receiver with >63dB adjacent channel rejection at >2 channels offset in 22nm FDSOI.
- In Paper 30.5, Sony introduces a 0.5V BLE transceiver with a 1.9mW RX achieving -96.4dBm sensitivity and 4.1dB adjacent channel rejection at 1MHz offset in 22nm FDSOI, consuming 1.9mW.
- In Paper 30.6, imec-Netherlands and Renesas Electronics describe a low-power BLE transceiver with support for phase-based ranging, featuring 5µs PLL locking time and 5.3ms ranging time, enabled by a staircase-chirp PLL with sticky-lock channel-switching.
- In Paper 30.7, the University of Michigan and the University of Virginia describe a crystal-less BLE Transmitter with a -86dBm frequency-hopping back-channel wakeup receiver and over-the-air clock recovery from a GFSK-modulated BLE packet.
- In Paper 30.8, imec-Netherlands and University College Dublin show a 3.5mm×3.8mm crystal-less MICS transceiver featuring coverages of ±160ppm carrier frequency offset and 4.8-VSWR antenna impedance for insertable smart pills.

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Session 30 Highlights: Efficient Wireless Connectivity

[30.2] NB-IoT and GNSS All-in-One System-on-Chip Integrating RF Transceiver, 23dBm CMOS Power Amplifier, Power Management Unit and Clock Management System for Low-Cost Solution

[30.5] A 0.5V BLE Transceiver with a 1.9mW RX Achieving -96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI

[30.8] A 3.5mm×3.8mm Crystal-Less MICS Transceiver Featuring Coverages of ±160ppm Carrier Frequency Offset and 4.8-VSWR Antenna Impedance for Insertable Smart Pills

Paper 30.2 Authors: Jongsoo Lee, Jaeyeol Han, Chilun Lo, Jongmi Lee, Wan Kim, Seungjin Kim, Byoungjoong Kang, Juyoung Han, Sangdon Jung, Jongwoo Lee, Thomas Byunghak Cho, Inyup Kang

Paper 30.2 Affiliation: Samsung Electronics, South Korea

Paper 30.5 Authors: Masahisa Tamura[1], Hideyuki Takano[1], Satoru Shinke[1], Hiroaki Fujita[1], Hironori Nakahara[1], Norihito Suzuki[1], Yutaka Nakada[1], Yusuke Shinohe[1], Shinichirou Etou[1], Tetsuya Fujiwara[2], Yasushi Katayama[1]

Paper 30.5 Affiliation: [1]Sony Semiconductor Solutions, Japan ; [2]Sony LSI Design, Japan

Paper 30.8 Authors: Minyoung Song[1], Ming Ding[1], Evgenii Tiurin[1], Kai Xu[1,2], Erwin Allebes[1], Gaurav Singh[1], Peng Zhang[1], Stefano Traferro[1], Hannu Korpela[1], Nick van Helleputte[3], Robert Bogdan Staszewski[2], Yao-Hong Liu[1], Christian Bachmann[1]

Paper 30.8 Affiliation: [1]imec-Netherlands, The Netherlands; [2]University College Dublin, Ireland; [3]imec, Belgium

Subcommittee Chair: Stefano Pellerano, Intel Corporation, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- Low standby power, operation at low supply voltages available from energy harvesting, and small form factor are vitally important for IoT and insertable medical devices.

TECHNICAL HIGHLIGHTS

- **Samsung Electronics introduces an NB-IoT and GNSS all-in-one system-on-chip, integrating the RF transceiver with a 23dBm CMOS power amplifier and the power management unit**
    - Linear 23dBm PA operation is enabled by on-chip Buck-Boost converters and adaptive biasing while low-cost dual system integration is made possible by judicious sharing of circuit blocks between the two modes.
- **Sony introduces a 0.5V BLE transceiver with -96.4dBm sensitivity and 4.1dB adjacent channel rejection while dissipating 1.9mW.**
    - Operation at 0.5V supply is made possible by an all-digital PLL incorporating an asynchronous SAR-ADC-based TDC and a current-reuse transformer-based gate-boosting LNA.
- **imec-Netherlands and University College Dublin introduce a 3.5mm×3.8mm crystal-less MICS transceiver for insertable smart pills**
    - Form factor is substantially reduced using a phase-tracking receiver that eliminates the crystal, and sharing the on-chip matching network that is capable of self-antenna impedance tuning.

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APPLICATIONS AND ECONOMIC IMPACT

- The fully integrated IoT transceiver SoCs will reduce costs and enable widespread deployment of IoT devices.
- Wireless transceivers that can operate at low supply voltage will be essential for IoT devices powered by energy harvesters, which leads to autonomous battery-free operation.
- Next generation medical implants will require extreme volume-constrained wireless transceivers, which will reduce patient discomfort, recovery time or even enable new types of in-body health monitoring.

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Session 31 Overview: Digital Circuit Techniques for Emerging Applications

Digital Circuits Committee

Session Chair: Alicia Klinefelter, NVidia, Durham, NC

Session Co-Chair: Mijung Noh, Samsung Electronics, Hwasung, Korea

Application-specific accelerators must leverage novel architectures and circuit techniques to achieve dramatic performance and power efficiencies to improve upon general-purpose processor implementations. This session presents: 1) a neuromorphic (rat-brain inspired) spiking-neural-network chip, accelerating visual self-location and mapping in a mobile robot; 2) a scalable in-memory annealing processor using register-based spins; and 3) an elastic clocking technique that leverages instruction and operand-based dynamic timing enhancement for an array of processing elements (PEs).

- In Paper 31.1, Georgia Institute of Technology presents an ultra-low-power mixed-signal oscillator-based neuroSLAM accelerator implementing a biologically inspired localization and mapping algorithm. The authors demonstrate a 65nm testchip integrated on a mobile robot that explores and maps indoor arenas at 23.82mW with a net energy efficiency of 8.97TOPS/W.
- In Paper 31.2, Nanyang Technological University shows a 0.5-to-1.2V scalable digital CMOS annealing processor based on compute-in-memory spin operators using register-based spins achieving 0.18-to-0.75μW power and 2.85-to-11.75fJ energy-per-spin in 65nm CMOS. A key feature of the work is the compute-in-memory architecture, requiring no SRAM read/write operations, reducing energy-per-spin by more than 10× compared to prior combinatorial optimization accelerators.
- In Paper 31.3, Northwestern University presents an elastic clock-chain technique for a multi-PE architecture. This paper takes advantage of instruction predictability and known changes in bit precision in order to apply an in-situ dynamic timing detection and enhancement scheme. The technique provides up to a 19% performance gain and saves up to 34% energy when running machine-learning applications.

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Session 31 Highlights: Digital Circuit Techniques for Emerging Applications

[31.1] A 65nm 8.79TOPS/W 23.82mW Mixed-Signal Oscillator-Based NeuroSLAM Accelerator for Applications in Edge Robotics

Paper Authors: Jong-Hyeok Yoon, Arijit Raychowdhury

Paper Affiliation: Georgia Institute of Technology, Atlanta, GA

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits Subcommittee

CONTEXT AND STATE OF THE ART

- Emerging systems and applications in edge robotics and augmented/virtual reality require ultra-low-power localization and mapping.
- Existing computational methods for SLAM based on filtering or keyword techniques are complex and high-power. A new biologically inspired algorithm based on rodents' abilities to re-localize using a sequence of visual cues allows for an energy-efficient implementation.

TECHNICAL HIGHLIGHTS

- **Georgia Institute of Technology presents design and measurement results for a mixed-signal neuromorphic vision-based SLAM accelerator in 65nm to map and track a robot within an environment.**
    - The highly integrated 2.0×2.5mm^2 testchip consumes 23.82mW with a peak energy efficiency of 8.79TOPS/W while continuously generating experience maps.
    - The accelerator contains a 7×7 spiking-neural-network (SNN)-based pose-cell array with digital head-direction computations performed in linear time.
    - The authors demonstrate a mobile robot performing the NeuroSLAM SNN across multiple indoor benchmark arenas.

APPLICATIONS AND ECONOMIC IMPACT

- With the increasing pervasiveness of mapping applications, including robotics and autonomous driving, acceleration of SLAM algorithms has become an important issue. A biologically inspired algorithm for ultra-low-power localization and mapping makes many new applications possible and efficient.
- Map generation and correction functionality demonstrated in a real-world environment during robot exploration.

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Session 32 Overview: Power Management Techniques

Power Management Subcommittee

Session Chair: *Chan-Hong Chern, TSMC, Taiwan*

Session Co-Chair: *Li Geng, Xi'an Jiaotong University, China*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management Subcommittee*

The first paper in this session focuses on a current-mode wireless power and data receiver for loosely coupled implantable devices. The next two papers are focusing on energy harvesting. The final two papers present new techniques for LDOs.

- In Paper 32.1, Sookmyung Women's University of Korea presents a current-mode (CM) wireless power and data receiver. The proposed RX uses an efficient power-extracting controller that fully drains energy of the LC tank. The RX achieves a high efficiency of 92.6% even at a resonance frequency of 13.56MHz. In addition, by adopting energy shift keying, the proposed RX can receive the data stream even with a small RX coil of 6×6mm^2. The IC is implemented using a 0.18µm CMOS process.
- In Paper 32.2, CEA-LETI-MINATEC presents a 7b phase-shifted synchronous electrical-charge-extraction (SECE) piezoelectric harvesting IC that self-adjusts and converges to the maximum power point in 0.6µm CMOS. This work achieves 328 and 282% energy-extraction gains compared to the full-bridge rectifier and non-tunable SECE, respectively. It achieves 94% conversion efficiency at low acceleration level (0.08g). It enables 454% bandwidth improvement, which is 3 to 10× larger than the published tunable strategies.
- In Paper 32.3, CEA-LETI-MINATEC presents an electromagnetic mechanical-energy harvester IC with one switching period maximum-power-point tracking achieving 95.9% efficiency. Fabricated in 0.6µm CMOS, the chip demonstrates 210 and 460% energy-extraction gains compared to a full-bridge rectifier during periodic vibrations and shock conditions, respectively, which does not require any off-chip inductor nor input decoupling capacitor.
- In Paper 32.4, Seoul National University presents a ring-amplifier-based LDO that achieves a wide input range from 0.4 to 1.2V and a PSRR over 20dB at 10MHz. Fabricated in a 40nm CMOS process, the chip occupies 0.0057mm^2 and provides a fast transient response to a 200mA/10ns load current step with a settling time of 25ns and a voltage droop of 45mV.
- In Paper 32.5, Arizona State University and Texas Instruments present a PCB-friendly, low-cost, daisy-chain solution to parallelize LDO regulators. Fabricated in a 0.18µm CMOS process with the area of 1.8225mm^2, it achieves thermal equilibrium at 2A of output current per-stage with a current sharing accuracy of 2.613%.

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Session 32 Highlights: Power Management Techniques

[32.1] A 13.56MHz Current-Mode Wireless Power and Data Receiver with Efficient Power-Extracting Controller and Energy-Shift-Keying Technique for Loosely Coupled Implantable Devices

Paper Authors: *Sung-Wan Hong*

Paper Affiliation: *Sookmyung Women's University, Seoul, Korea*

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management Subcommittee*

CONTEXT AND STATE OF THE ART

- Wireless power transfer is an attractive solution to supply power to implantable systems.
- In some implantable systems the RX should receive a data stream along with the power from the TX. The data stream and power can be received through a single power channel by adopting amplitude-shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK), but these methods are only workable when the coils are strongly coupled.

TECHNICAL HIGHLIGHTS

- Sookmyung Women's University present a current-mode wireless power and data receiver (RX) with loosely coupled coils.
  - The receiver uses a power-extracting controller that is able to fully drain the LC tank energy. At the resonance frequency of 13.56MHz, the RX achieves the efficiency of 92.6%
  - By adopting energy-shift keying (ESK), the proposed RX can receive a data stream even with an RX coil as small as 6×6mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- Wireless power delivery to implantable devices
- Data communication via inductive coupling

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Session 33 Overview: Non-Volatile Devices for Future Architectures

Technology Directions Subcommittee

Session Chair: Munehiko Nagatani, NTT Corporation, Japan

Session Co-Chair: Nick van Helleputte, imec, Belgium

Non-volatile devices are enabling new architectures with energy and area efficiencies. The first two papers describes RRAM(ReRAM)-based energy-efficient in-memory computing chips. The final paper shows the first implementation of via-switch FPGA achieving excellent computation density.

- In Paper 33.1, Stanford University describes a 74TOPS/W CMOS-RRAM neurosynaptic core with dynamically reconfigurable dataflow and in-situ transposable weights for probabilistic graphical models.
- In Paper 33.2, Tsinghua University presents a fully integrated 158.8Kb analog ReRAM based 78.4TOPS/W computing-in-memory chip with fully-parallel MAC computing.
- In Paper 33.3, Osaka University shows a 65nm area and power-optimized FPGA utilizing via-switches as programmable cross-points achieving up to 64% and 91% area reduction compared to atom-switch FPGA and SRAM FPGA, respectively.

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Session 33 Highlights: Non-Volatile Devices for Future Architectures

[33.1] A 74TOPS/W CMOS-ReRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-Situ Transposable Weights for Probabilistic Graphical Models

[33.3] A Via-Switch FPGA: 65nm CMOS Implementation and Architecture Extension for AI Applications

Paper 33.1 Authors: Weier Wan[1], Rajkumar Kubendran[1], S. Burc Eryilmaz[1], Wenqiang Zhang[2], Yan Liao[3], Dabin Wu[3], Stephen Deiss[2], Bin Gao[3], Priyanka Raina[1], Siddharth Joshi[4], Huaqiang Wu[3], Gert Cauwenberghs[2], H.-S. Philip Wong[1]

Paper 33.1 Affiliation:[1]Stanford University, Stanford, CA, [2]University of California, San Diego, CA, [3]Tsinghua University, Beijing, China, [4]University of Notre Dame, Notre Dame, IN

Paper 33.3 Authors: Masanori Hashimoto[1], Xu Bai[2], Naoki Banno[2], Munehiro Tada[2], Toshitsugu Sakamoto[2], Jaehoon Yu[1], Ryutaro Doi[1,2], Yusuke Araki[3], Hidetoshi Onodera[3], Takashi Imagawa[4], Hiroyuki Ochi[4], Kazutoshi Wakabayashi[5], Yukio Mitsuyama[6], Tadahiko Sugibayashi[2]

Paper 33.3 Affiliation: [1]Osaka University, Suita, Japan, [2]NEC, Tsukuba, Japan, [3]Kyoto University, Kyoto, Japan, [4]Ritsumeikan University, Kusatsu, Japan, [5]NEC, Kawasaki, Japan, [6]Kochi University of Technology, Kami, Japan

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan

CONTEXT AND STATE OF THE ART

- Non-volatile memory (NVM) based compute-in-memory architectures have significant advantages in area and energy efficiency.
- Compelling need for low-energy and parallel data path operations for evolving AI applications.

TECHNICAL HIGHLIGHTS

- **Stanford University describes a CMOS-ReRAM neurosynaptic core with dynamically reconfigurable dataflow and in-situ transposable weights for probabilistic graphical models.**
    - A 256 CMOS neuron, 65K ReRAM synapse compute in memory chip in 0.13µm CMOS/HfOx/TaOx ReRAM achieves 74TOP/W energy efficiency in matrix vector multiplication.
- **Osaka University presents the first implementation of an area and power-optimized FPGA that utilizes via-switch as programmable cross-points in a cross bar.**
    - A via-switch FPGA in 65nm CMOS achieves 61.4% and 91.7% area reduction compared to atom-switch FPGA and SRAM FPGA, respectively.

APPLICATIONS AND ECONOMIC IMPACT

- Enables highly integrated neural network processors for intelligent AI workloads with improved energy efficiency and potentially larger workloads.
- Enables area and power-efficient, reconfigurable, next-generation FPGA implementations with dramatically higher compute density.

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Session 34 Overview: Biomedical Sensing, Stimulation, and Harvesting

Technology Directions Subcommittee

Session Chair: Rabia Tugce Yazicigil, Boston University, Boston, MA

Session Co-Chair: Edoardo Charbon, EPFL, Lausanne, Switzerland

This session covers a wide range of emerging biomedical systems for wearables and implantable components. The first paper introduces a real-time, single-particle, dosimeter array for cancer therapy, followed by neuromorphic retinal prosthesis SoC and an implantable neurostimulator utilizing magnetoelectric power and data transfer. Deep tissue ultrasonic oxygen monitor using luminescence sensing comes next, followed by an ambient energy harvesting and a body-coupled power delivery system. The final paper showcases a wireless concurrent EEG recording and body-coupled communication with a concentric electrode.

- In Paper 34.1, the University of California at Berkeley presents a millimeter-scale real-time single-particle 64×64 dosimeter array for cancer therapy.
- In Paper 34.2, National University of Singapore shows a 1225-channel neuromorphic retinal prosthesis SoC with localized 49-point temperature regulation and 56.3nW/channel image processor.
- In Paper 34.3, Rice University presents an 8.2mm^3 implantable neurostimulator using magnetoelectric power and data transfer.
- In Paper 34.4, the University of California Berkeley introduces a 4.5mm^3 implantable real-time dissolved oxygen monitoring system combining ultrasound technology and luminescence sensing.
- In Paper 34.5, National University of Singapore presents an ambient energy harvesting and body-coupled power delivery system with full-body area coverage in a 40nm CMOS technology.
- In Paper 34.6, National University of Singapore introduces a 1.6mm^2 chip for concurrent EEG signal recording and body-coupled data transmission with a concentric electrode fabricated in a 0.18μm CMOS technology.

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Session 34 Highlights: Biomedical Sensing, Stimulation, and Harvesting

[34.1] A 64×64 Implantable Real-Time Single-Charged Particle Radiation Detector for Cancer Therapy

Paper 34.1 Authors: Kyoungtae Lee[1], Jessica Scholey[2], Eric B. Norman[1], Inder Daftari[2], Kavita K. Mishra[2], Bruce Faddegon[2], Michel M. Maharbiz[1], Mekhail Anwar[2]

Paper 34.1 Affiliation: [1]University of California at Berkeley, Berkeley, CA, [2]University of California, San Francisco, CA

Subcommittee Chair: Rabia Tugce Yazicigil, Boston University, Boston, MA

Subcommittee Co-Chair: Edoardo Charbon, EPFL, Lausanne, Switzerland

CONTEXT AND STATE OF THE ART

- *In vivo* dosimeters have been essential for enabling effective and safer cancer treatment through reporting *in situ* radiation doses to clinicians.
- Conventional *in vivo* dosimeters with a single large detector are often limited in spatial resolution and they cannot distinguish between a single high energy particle depositions and combined several lower energy depositions.

TECHNICAL HIGHLIGHTS

- **A mm-scale real-time single-particle dosimeter array with a size of 64×64 for charged particle cancer therapy**
  - Diodes are utilized for detecting incident charged particles by sensing the pulse width and leveraging the relationship between the voltage drop linked with the amount of energy deposited in the depletion region and the length of time it takes for returning the baseline voltage.
  - A 64×64 array capable of single particle detections over a wide detection area in real-time is implemented and demonstrated in experiments using proton beams generated by the particle accelerator.

APPLICATIONS AND ECONOMIC IMPACT

- Technology demonstrated has a significant potential in enhancing the dosage accuracy, and hence safety during clinical proton treatment for cancer patients.

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ISSCC 2020
TRENDS

Conditions of Publication

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2020 in February in San Francisco

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 67th appearance of ISSCC, on February 16th to February 20th, 2020, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2020, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 16 - February 20, 2020,

at the San Francisco Marriott Marquis Hotel.

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HISTORICAL TRENDS IN TECHNICAL THEMES

ANALOG SYSTEMS

ANALOG SUBCOMMITTEE

POWER MANAGEMENT SUBCOMMITTEE

DATA CONVERTERS SUBCOMMITTEE

Analog – 2020 Trends

Subcommittee Chair: *Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands*

At ISSCC 2020, new analog circuit techniques are enabling improved performance and reduced power for temperature sensors, frequency references, voltage references, and amplifiers. Co-packaged bulk-acoustic wave (BAW) technology with better than +/-30ppm stability enables crystal-less radio applications. Gallium Nitride (GaN) technology provides the ability to realize voltage references that span the very wide temperature range of -50ºC to 200ºC. Class-D amplifiers achieve the highest total harmonic distortion (THD) to date by utilizing Delta-Sigma techniques.

In the case of integrated temperature sensors, both bipolar and resistor-based designs continue to dramatically improve in energy efficiency as revealed by Figure 1. In addition, the accuracy of single-trim resistor-based temperature sensors is now approaching that of their BJT counterparts.

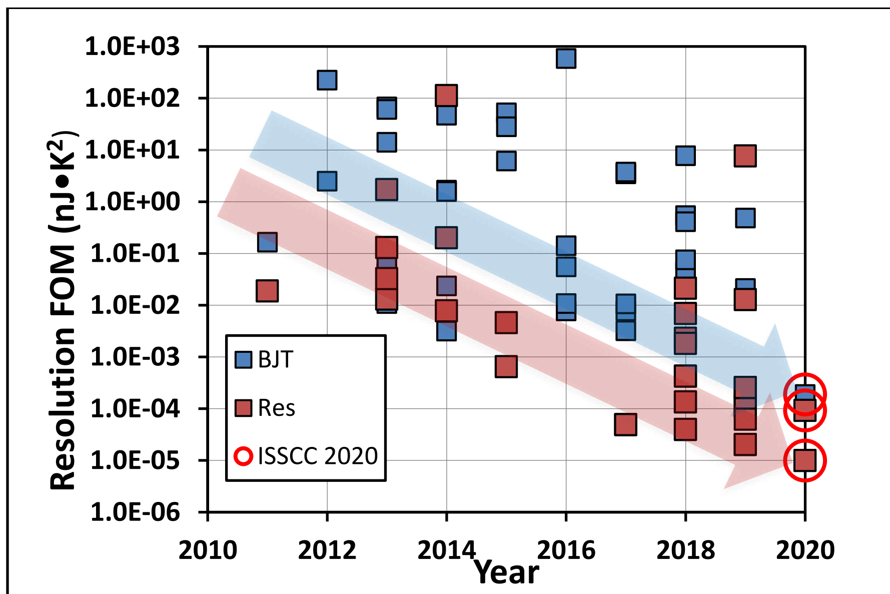

Figure 1: Trends in Energy Efficiency of Integrated Temperature Sensors: Resolution FoM versus Time

Non-crystal oscillators continue to improve power efficiency, while achieving accuracies below +/-500ppm, as indicated in Figure 2.

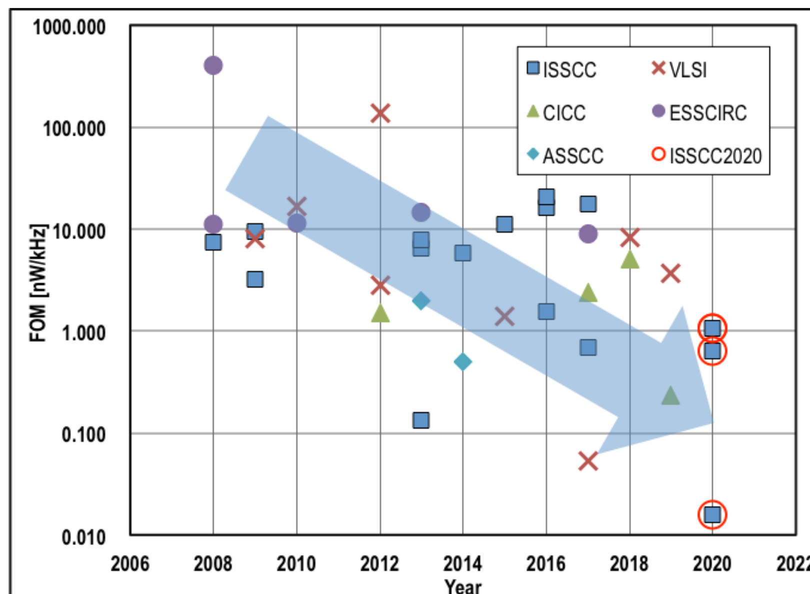

Figure 2: Trends in Power Efficiency of Non-Crystal Oscillators Versus Time

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Power Management – 2020 Trends

Subcommittee Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA*

Power and energy management are important for a number of applications spanning embedded and performance computing, communications systems, consumer devices, automotive/industrial sensing, and control. Over the past decade, new topologies, semiconductor technologies, and control paradigms have driven fundamental changes both at the architecture and system level. Hybrid and resonant switched-capacitor topologies which promise better utilization of both active semiconductors and passive components are beginning to mature and spread into diverse applications (from LED and display drivers to high-conversion load power delivery). At lower voltages, hybrid approaches are pushing toward higher integration with all passive components integrated on chip. The need for higher-voltage power conversion is also growing, with more designs targeting 48 to 400V line, power delivery, and cross-domain isolation interfaces. Gallium Nitride (GaN) semiconductor technologies are improving in both integration levels and functionality, with power devices, gate-driver, instrumentation, and interface circuitry now starting to share the same die. In addition to high-voltage isolated power delivery, data transmission across galvanic isolation boundaries is increasingly important in many applications. Energy harvesting continues to mature for a variety of piezoelectric, electromagnetic, and optical transducer systems.

Perhaps the most important observable trends in power-management integrated circuits pertain to the diversification of applications, voltage, and power ranges. The following trends are observed at ISSCC 2020:

- As GaN gains greater capability for high-level integration, a variety of circuit techniques are emerging that can improve EMI, efficiency, and reliability of high-voltage high-frequency switching power converters. These circuit techniques resemble ‘old school’ NMOS only techniques of many decades ago yet add new and important capabilities.
- Hybrid and resonant switched-capacitor converter techniques are increasingly leveraged in a wide range of topologies to reduce voltage stress on switches, shrink passive component size, and enable higher switching frequency.
- The number and diversity of high-voltage IC designs is increasing to deal with challenges related to grid interface, signal and power isolation, and powering embedded and sensor interface systems from high DC-voltage domains.

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Data Converters – 2020 Trends

Subcommittee Chair: *Michael Flynn, University of Michigan, Ann Arbor MI*

Data converters are a critical link between the analog physical world and the world of digital computing and signal processing prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and linearity while continuing to increase power efficiency. This year, ISSCC 2020 continues the trend of highly energy-efficient analog-to-digital converters (ADCs) with a combination of successive-approximation-register (SAR), noise-shaping SAR, and delta-sigma-based designs. Time-interleaved pipeline architectures are pushing the speed limits of converter design!

The three figures below represent traditional metrics that capture the innovative progress in ADC design. The first figure plots power dissipated relative to the Nyquist sampling rate (P/f_{snyq}), as a function of signal-to-noise and distortion ratio (SNDR), to give a measure of ADC power efficiency. Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 1fJ/conversion-step. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Designs published from 1997 to 2019 are shown in circles. ISSCC 2020 designs are shown in black dots, which continue moving towards the lower right of the figure.

The second figure plots signal fidelity vs the Nyquist sampling rate normalized to power consumption. At low sampling rates, converters tend to be limited by thermal noise, independent of the sample rate. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner, indicated by the roll-off vs frequency in the dashed line. The past ten years have resulted in an improvement of over 10dB in power-normalized signal fidelity, or a 10× improvement in speed for the same normalized signal fidelity. Of note in this year's ISSCC is that two designs are pushing towards thermal noise limited efficiency, using both delta-sigma and noise-shaped SAR architectures. A pipelined SAR architecture delivers record-setting performance in the speed vs efficiency corner of the graph.

The final figure plots ADC bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. While ten years ago, a state-of-the-art data converter showed an aperture error of approximately $1ps_{rms}$, in recent years, designs with aperture errors below $100fs_{rms}$ have been published. ISSCC 2020 further advances the state-of-the-art with an extremely high performing time-interleaved pipeline architecture, which surpasses the $100fs_{rms}$ aperture line.

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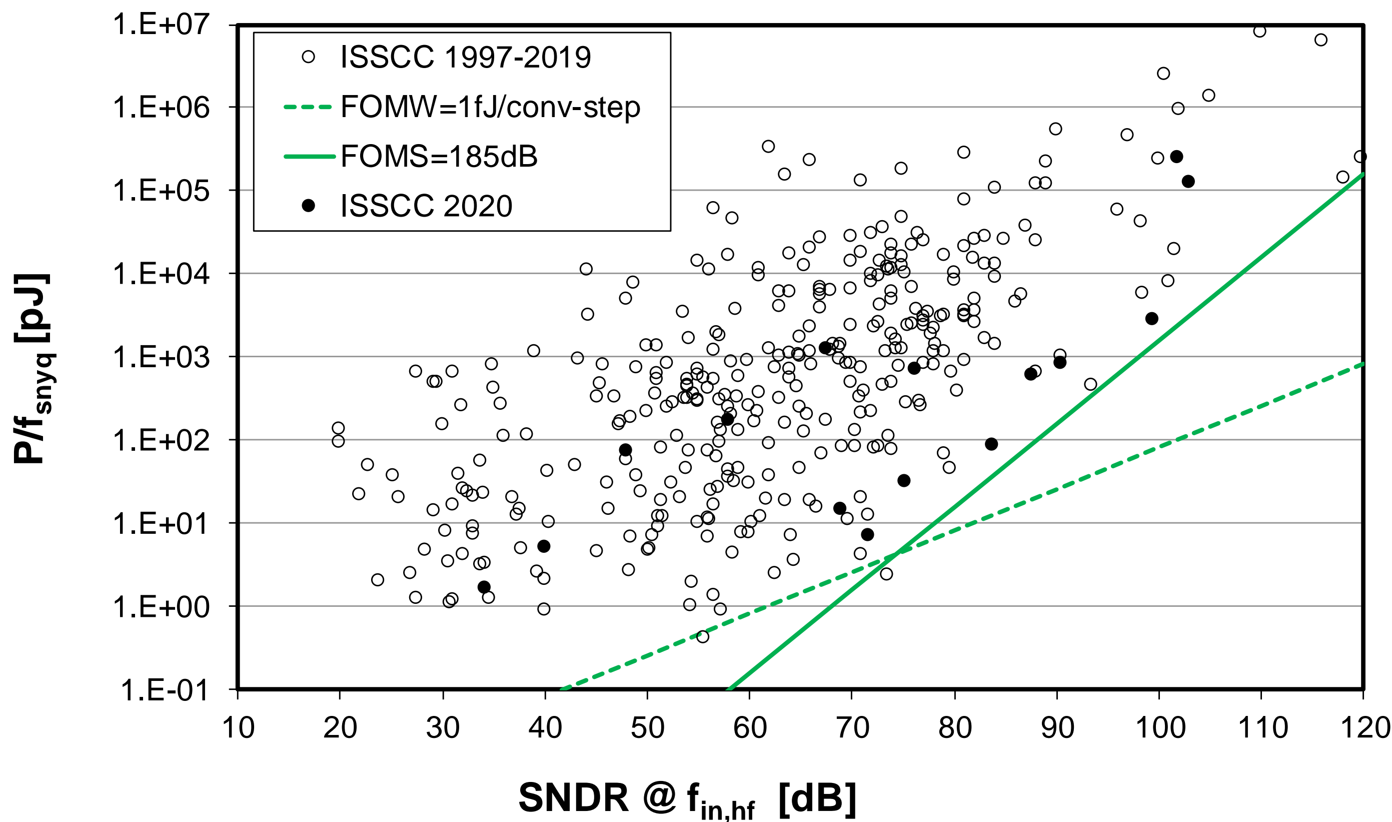

Figure 4: ADC power efficiency (P/f_{snyq}) as a function of SNDR.

ISSCC 1997-2019
Envelope
ISSCC 2020
190
180
170
160
150
140
130
120
1.E+02 1.E+04 1.E+06 1.E+08 1.E+10 1.E+12
$FOM_{S,hf}$ [dB]
f_{snyq} [Hz]

Figure 5: Power normalized noise and distortion vs Nyquist sampling rate.

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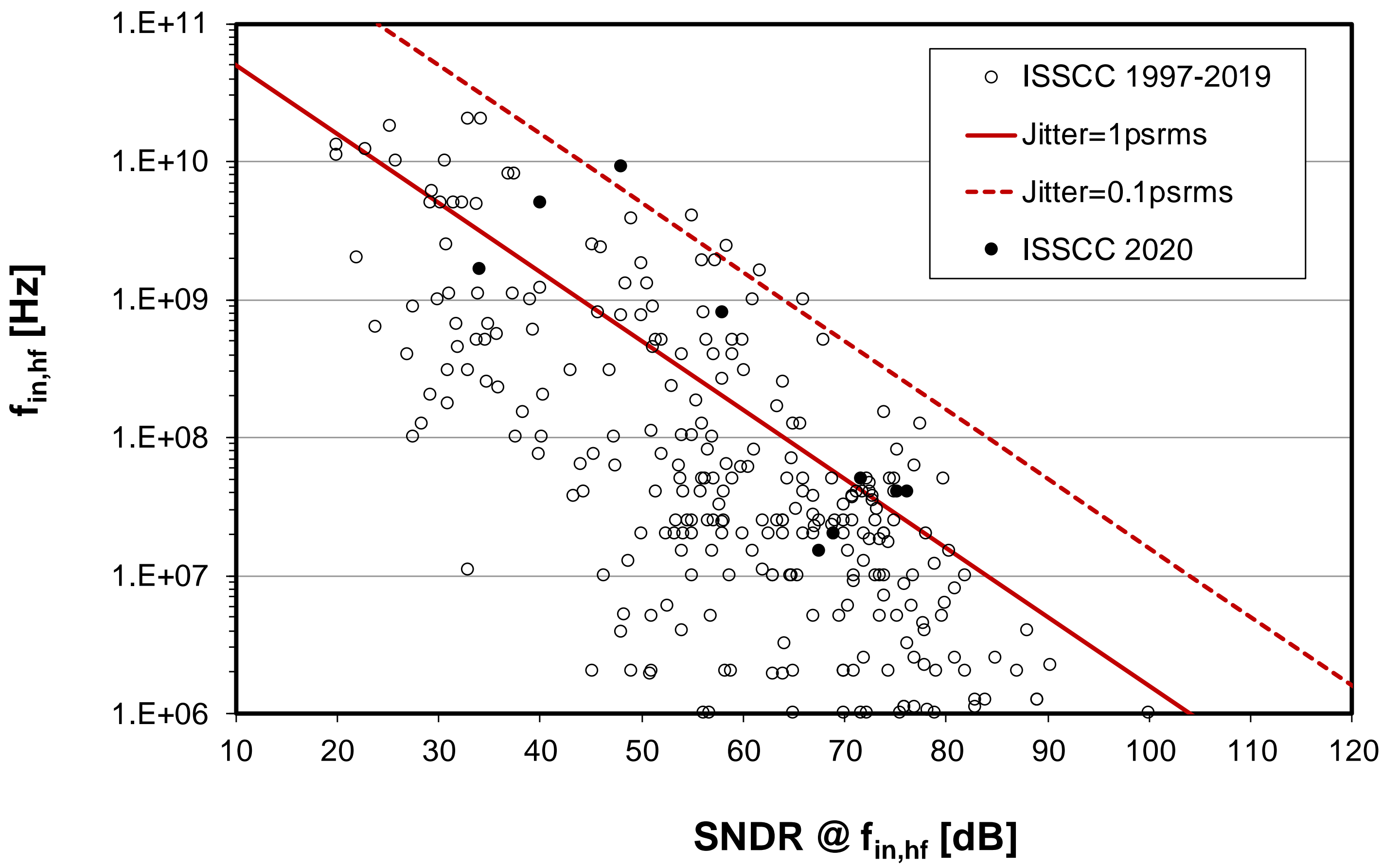

Figure 6: Bandwidth vs SNDR.

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HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

RF SUBCOMMITTEE – WIRELESS SUBCOMMITTEE

WIRELINE SUBCOMMITTEE

RF Subcommittee – 2020 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

ISSCC 2020 features terahertz (THz) imaging demonstrators, CMOS power amplifiers, and phase-locked loop (PLL) prototypes. Applications driving advances in the field of RF integrated circuits in silicon technologies are: 1) broadband and fifth-generation (5G) communications using massive multiple input/multiple output (MIMO) and millimeter-wave (mm-wave) technologies, 2) the Internet of Things (IoT), and 3) sensing and imaging at sub-millimeter-wave (sub-mm-wave) frequencies.

Phase-Locked Loop Synthesizers: Visible highlights are phase-locked loops (PLLs) generating mm-wave frequency carriers directly or via on-chip multipliers, synthesizers offering lower integrated jitter and power consumption (for example,, -250dB jitter-power FoM), and wideband frequency-modulated continuous-wave (FMCW) radar chirp generation. Overall, sub-sampling PLLs continue to trend lower in power consumption and integrated timing jitter, with all-digital PLLs continuing to displace traditional analog designs. Fractional-N bang-bang, all-digital, and hybrid fractional-N/integer synthesizers are also demonstrating continuing innovations in more traditional PLL designs. The trend in FoM for PLLs, which depends on integrated jitter (jitter variance) and power consumption, are illustrated in Figure 7. ISSCC 2020 presents two fractional-N PLLs with outstanding timing jitter performance: 1) a 12.8-to-15.2GHz digital bang-bang PLL that realizes 66fs-rms jitter and perform a 1GHz hop to within 0.1% of the steady-state frequency in 18.55μs, and 2) 12.5GHz fractional-N sampling PLL in 28nm CMOS that incorporates a digital background phase-error correction to enable 58fs integrated jitter (fractional mode) and 51fs (operating in integer mode). The overall FoM for these PLLs is consistent with previous designs, as seen on the figure.

Advanced voltage-controlled oscillator and mm-wave-output frequency-generation circuit designs operating with greater stability at lower power consumption redefine the state-of-the-art in CMOS designs, ensure that advances in frequency synthesis will continue for the forseeable future!

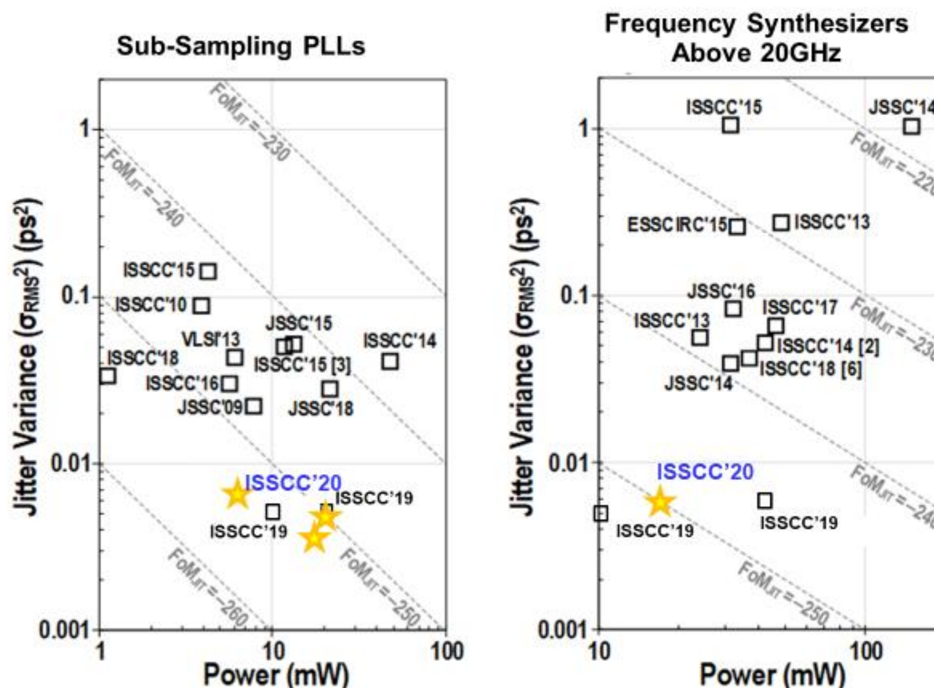

Figure 7: Oscillator trends

RF and mm-Wave PAs: Doherty-type power amplifiers (PA) integrated in CMOS are demonstrating improved power-added efficiency (PAE) at the higher peak-to-average power ratios demanded by advanced modulation formats, such as 5G NR. A 24-to-30GHz, watt-level, Doherty PAs fully integrated in 45nm SOI CMOS employs a multi-primary distributed-active-transformer (DAT) power combiner

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and is capable of supporting 5G NR transmissions. Both multi-way power combing and active load modulation are achieved simultaneously. A digital polar PA prototype operating in class-G mode also operates above 1W, but in the 2.4GHz ISM band. Remarkably, when the output power is reduced by 18dB, this PA is still capable of drain efficiencies approaching 50% of peak performance. Signal quality under 1024-QAM modulation is excellent at -44.5dB EVM for 23.2dBm RF power output. ISSCC 2020 will also feature the first D-Band power amplifier in 16nm CMOS (FinFET). It demonstrates a peak gain of 25.6dB, saturated output power of 15dBm, and peak PAE of 11.7%. Active chip area for this 135GHz PA is just 0.062mm^2.

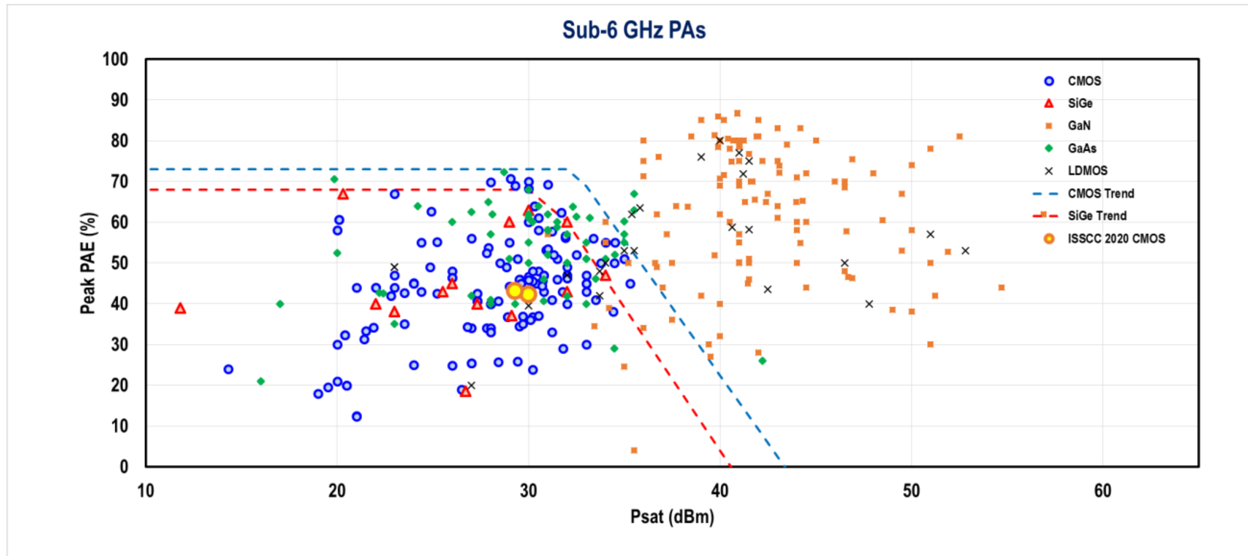

Figure 8: Under 6GHz power-amplifier trend

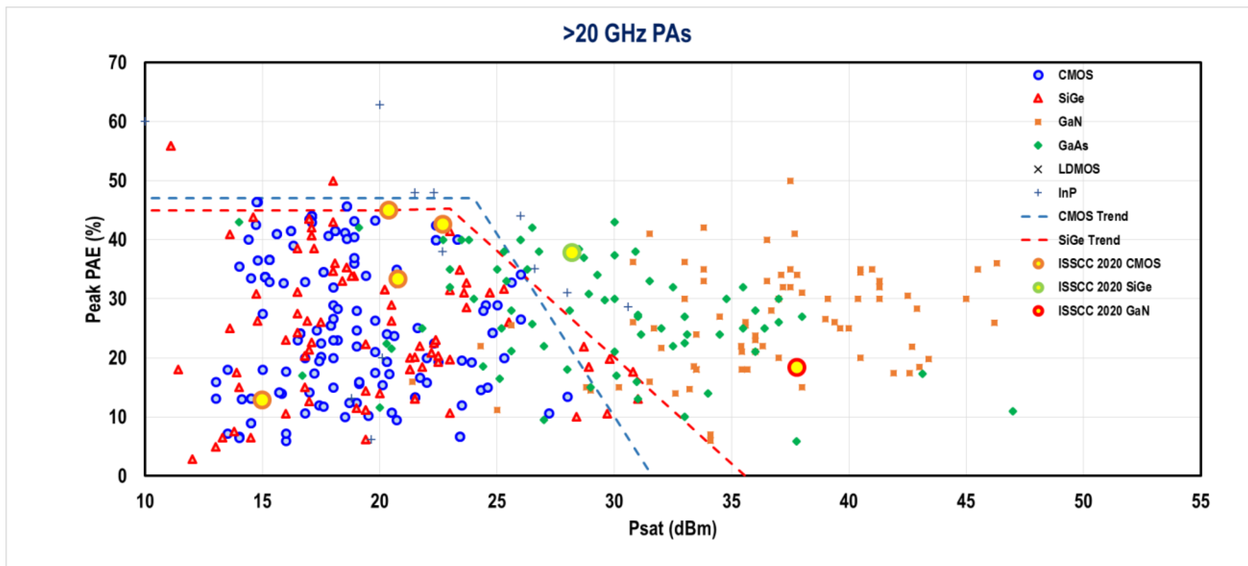

Figure 9: Over 20GHz power-amplifier trend

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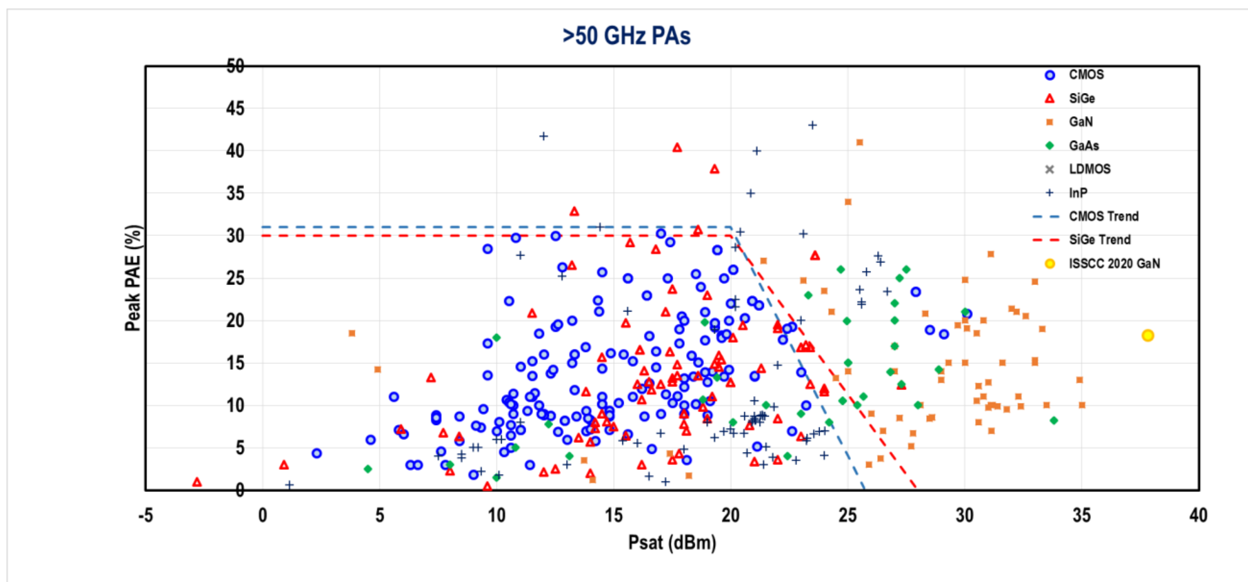

Figure 10: Over 50GHz power-amplifier trend

Emerging Technologies for Communication and Terahertz Sensing/Imaging: At ISSCC 2020, terahertz-frequency imaging and sensing chips, demonstrating higher levels of complexity and power outputs than ever before, and radio front-end circuits, enabling full duplex communication, are important developments. Computational terahertz imaging debuts at ISSCC 2020 with an 8×8 pixel source array system on a chip (SoC) with on-chip built-in self test (BIST) radiates up to 9.2dBm at 0.42THz and can support imaging up to 30,000 frames per second. The highest radiated power for silicon-based sources above 0.35THz is produced by a beam-steerable array implemented in 40nm CMOS. It combines 36 coherent radiators producing 24.1dBm Equivalent Isotropically Radiated Power (EIRP) and a beam-steering range of 30° at a frequency of 0.59THz.

Future low-latency radio access networks demand clocks with 0.1parts/billion (ppb) stability. A 70mW chip-scale molecular clock probing the 231.06GHz transition of carbonyl sulfide demonstrates a stability of +/-3ppb with changing temperature. Finally, a sub-THz back-scattering wireless tag operating at 260GHz has a 5cm range for bidirectional communication via an on-chip antenna array capable of beam-steering across 30°.

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Wireless – 2020 Trends

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR*

The continuing demand for faster wireless data rates in the context of mobile battery limitations drives the development of high-throughput and power-efficient transceivers. This year, at ISSCC 2020 both WiFi and cellular standards continue to evolve with 5G-NR and WiFi-6/802.11ax to deliver ever increasing data throughput by using dense 1024-QAM modulation, a wide bandwidth of up to 200MHz and multiple parallel data-streams using uplink and downlink MIMO. Furthermore, carrier aggregation and concurrent operation allow cellular and WiFi radios to obtain larger spectrum resources when a single contiguous frequency range is not available.

Figure 11 shows the trend in the number of downlinks for recent cellular SoC implementations, as well as the shift in process nodes. It indicates an increasing interest in carrier aggregation to support higher data rates. This year, an advanced cellular transceiver features 10 downlinks in 12nm FinFET CMOS. The transceiver extends carrier aggregation to support up to 6 inter-band 3G, 4G, and 5G carriers while also enabling NR and LTE protocols with dual connectivity (EN-DC).

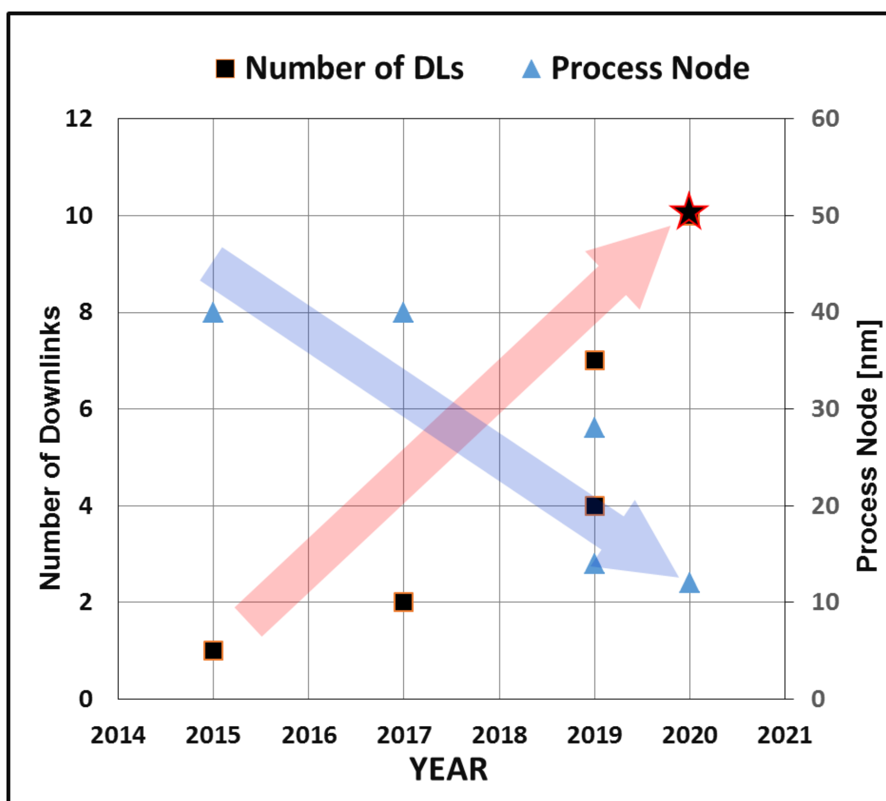

Figure 11: Trends In the number of downlinks and process nodes for recent cellular SoC implementations

Operation at low supply voltages available from energy harvesting and small form factor are vitally important for IoT and insertable medical devices. A low-voltage BLE transceiver that is capable of operating with energy harvesting is introduced at ISSCC 2020 with -96.4dBm sensitivity and 4.1dB adjacent channel rejection while dissipating 1.9mW. Furthermore, a small form factor crystal-less MICS transceiver for insertable smart pills is presented with 3.5mm×3.8mm footprint.

Figure 12 shows the trend in energy efficiency for 60GHz and beyond 80GHz receivers. A receiver presented at ISSCC 2020 leverages both dual-polarization and circuit techniques to demonstrate <2pJ/b efficiency, while achieving throughputs >50Gb/s at mm-wave frequencies, achieving 64Gb/s data rate. This is the first 60GHz phased-array receiver with >50Gb/s throughput!

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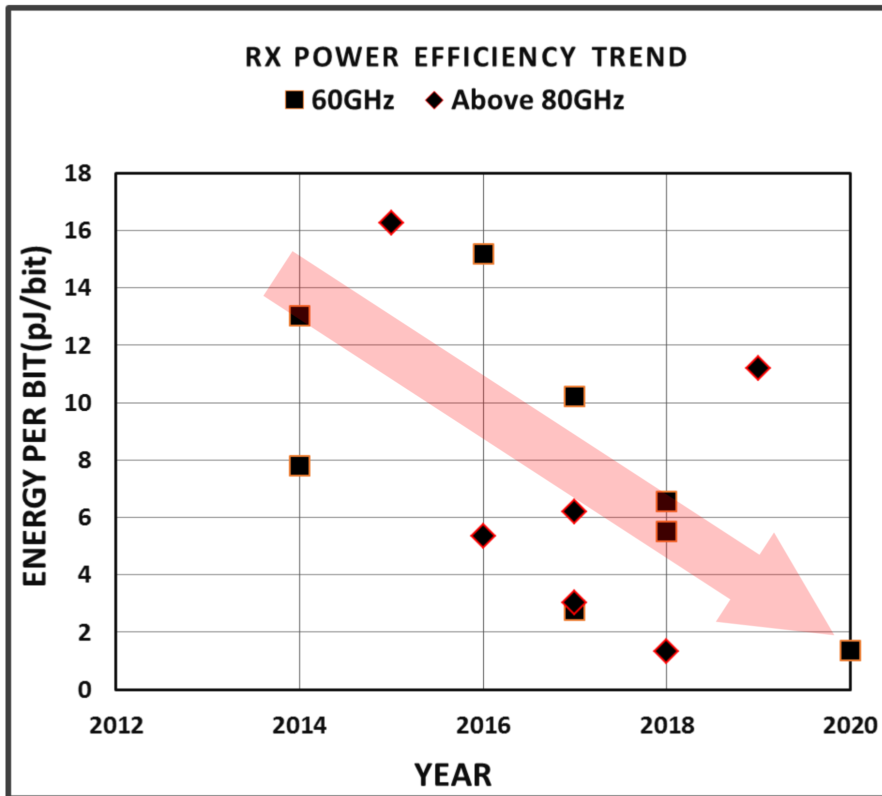

Figure 12: RX power efficiency trend

Increasing demands on high data-rate transceivers are also reflected in cellular communications with the developments of millimeter-wave systems for 5G NR in the 28 and 39GHz bands.

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Wireline – 2020 Trends

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR

Over the past few decades, electrical and optical interconnects have been the key components bridging the gap between the exponentially growing demands for data bandwidth across electronic components/systems and the relatively gradual increase in pin/cable density. Ranging from handheld electronics to supercomputers, wireline data communication bandwidth must also grow exponentially to avoid limiting the performance scaling of these systems. By increasing the data per pin or cable of various electronic devices and systems, such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN, wireline I/O has fueled incredible technological innovation in electronic devices and systems over the past few decades. Figure 13 shows that data rate per pin has approximately doubled every four years across various I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 14 shows that the data rates for published transceivers have kept pace with these standards while taking advantage of CMOS scaling. Figure 15 shows published transceiver energy efficiency vs channel losses at Nyquist frequency in the 40-to-50dB range. In part, this incredible improvement is enabled by the power-performance benefits of process technology scaling. However, sustaining this exponential trend for I/O bandwidth scaling requires more than just transistor scaling. Significant advances in energy efficiency, channel equalization and clocking must be made to enable the next generation of low-power and high-performance computing systems. ISSCC 2020 includes examples of short-reach electrical interconnects operating up to 25Gb/s, long-reach copper interconnect transceivers operating up to 112 Gb/s, and optical transceivers and components operating up to 112Gb/s (direct modulation) and 640Gb/s (coherent). New techniques for noise reduction, power reduction, channel equalization, and clock recovery are reported. These transceivers and transceiver building blocks are implemented in both CMOS and BiCMOS technologies.

Scaling Electrical Interconnects to 100Gb/s

Bandwidth requirements in data centers and telecommunication infrastructure continue to drive the demand for ultra-high-speed wireline communication. Over the past few years, complete transceivers operating up to 56Gb/s were demonstrated across a variety of channel lengths. Two notable trends in these transceivers, especially for long-reach channels, are the adoption of PAM-4 modulation and a transition to DAC/ADC architectures with DSP-based equalization. Although PAM-4 provides twice the data rate at the same baud rate as conventional NRZ to relax channel loss requirements for bandwidth doubling, it also comes with more stringent requirements for linearity, noise and multi-level signaling. This trend has motivated development of low-power data converters, digital equalization, and clock recovery, along with linear high-bandwidth TX and RX analog front ends. Over the past two years, the first transceiver components were demonstrated to extend these transceivers to 112Gb/s. This year at ISSCC 2020, a 56Gb/s DAC/ADC-based transceiver, a 100GBaud DAC-based transmitter, and the first descriptions of complete 112Gb/s PAM-4 long-reach transceivers in 7nm CMOS will be presented. Xilinx will describe a 112Gb/s PAM-4 transceiver for long-reach copper interconnects employing a 36-way time-interleaved 56GS/s 7b ADC. MediaTek will present a complete 4-lane 112Gb/s DAC/ADC-based transceiver. Both transceivers exhibit flexible equalization capability and consume <5pJ/b (not including DSP power).

Silicon Photonic Bandwidth Scaling and Integration

The explosive growth of data and data-centric computing places stringent demands on the bandwidth and energy efficiency of data center interconnects, spurring the development of several 200-to-400G Ethernet standards. Although within the rack much of the interconnect bandwidth is provided by electrical links over copper interconnects, optical interconnects are increasingly used to bridge longer distances. Silicon-photonics-based solutions are of particular interest for low cost 50+Gb/s/λ optical transceivers. Furthermore, multi-level modulation schemes such as PAM-4 improve the trade-off between circuit bandwidth, power consumption, data rate, and optical link range compared with NRZ optical signaling. Since many such modules are packed side-by-side in networking and computing infrastructure, low-power consumption is required to prevent overheating the equipment. The highly-integrated silicon photonic approaches presented this year at ISSCC 2020 will address this need by communicating at 50-to-100Gb/s over each fiber using PAM-4 modulation with low-power consumption, reducing the need for expensive cooling and on the edge of pushing classical discrete implementation toward obsolescence. Intel will describe a PAM-4 microring-based optical transmitter using a 3D-integrated silicon photonic and CMOS circuit assembly with robust 112Gb/s operation. The thermal variability and nonlinearities that usually plague such modulators are addressed with nonlinear equalization and closed-loop thermal control. STMicroelectronics will demonstrate a transceiver

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for the IEEE802.3bs 200GBASE-DR4 standard. The 4-channel electro-optical transceiver provides an aggregate bandwidth of 200Gb/s using a 55nm BiCMOS technology that is 3D-assembled onto a silicon photonic front-end IC through copper pillars. Data rate scaling for coherent optics for longer-reach optical interconnects are also highlighted at ISSCC 2020. NTT will also demonstrate a four-channel MZM driver capable of transmitting 640Gb/s over a single fiber using dual-polarization (DP) 32QAM modulation while consuming only 1.4pJ/b

Continuing to aggressively scale I/O bandwidth is essential for the industry but the tradeoffs between bandwidth, power, area, cost ,and reliability are extremely challenging. Advances in circuit architecture, interconnect topologies, transistor scaling, and integrated silicon photonics are changing how I/O will be done over the next decade. The most exciting and promising of these emerging technologies for electrical and optical interconnects will be highlighted at ISSCC 2020.

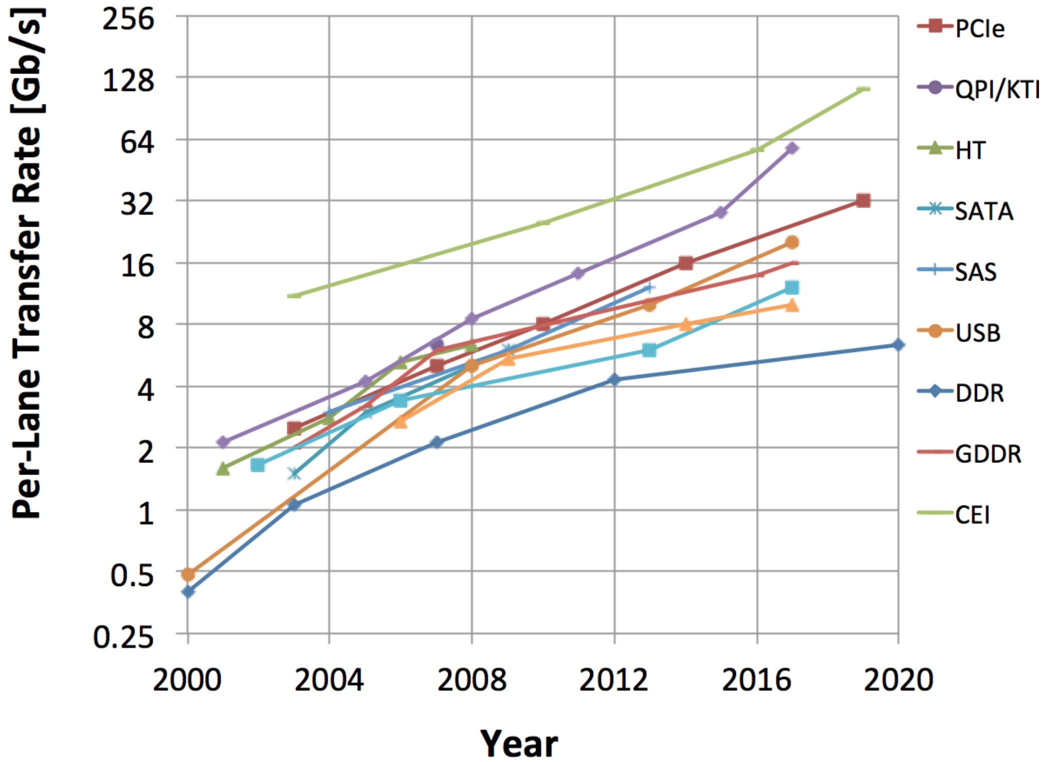

Figure 13: Per-pin data rate vs. Year for a variety of common I/O standards.

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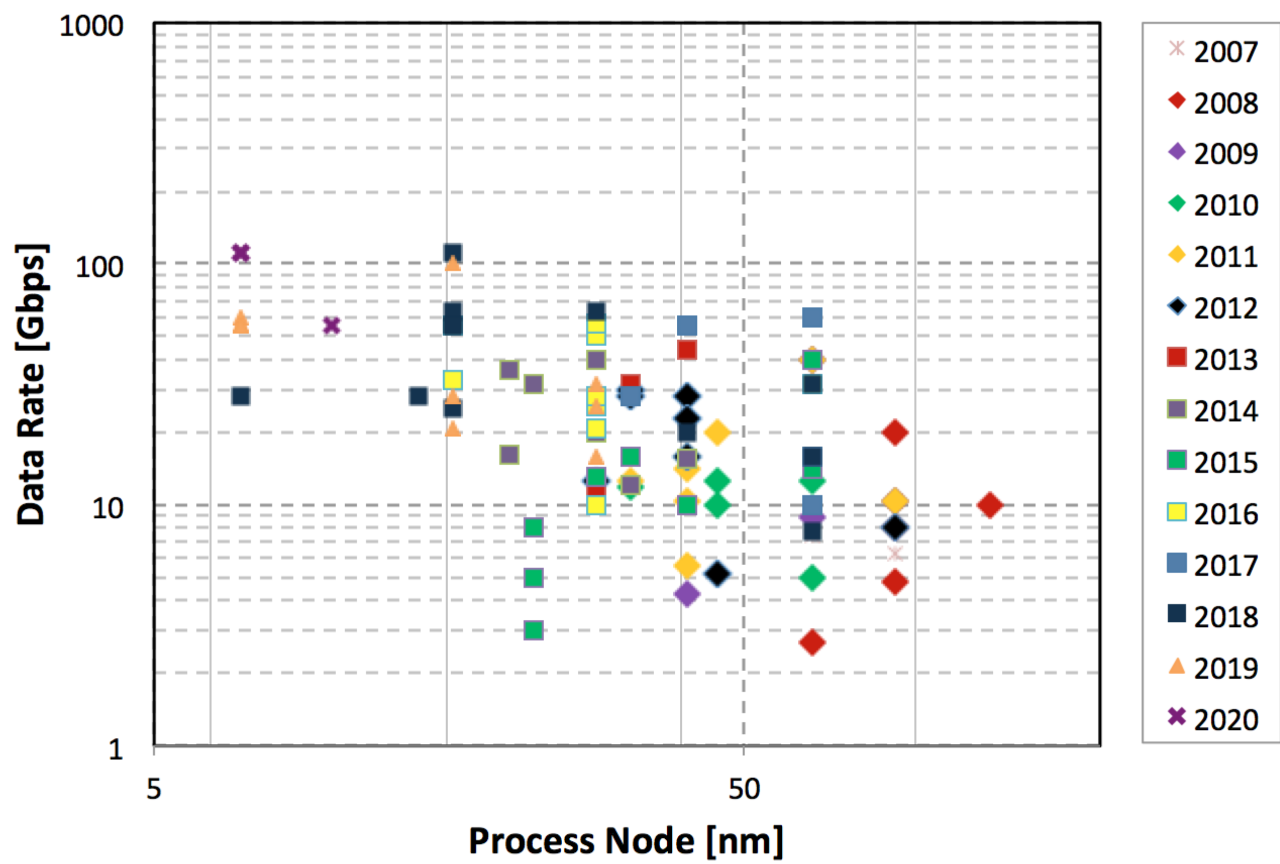

Figure 14: Data-rate vs process node and year.

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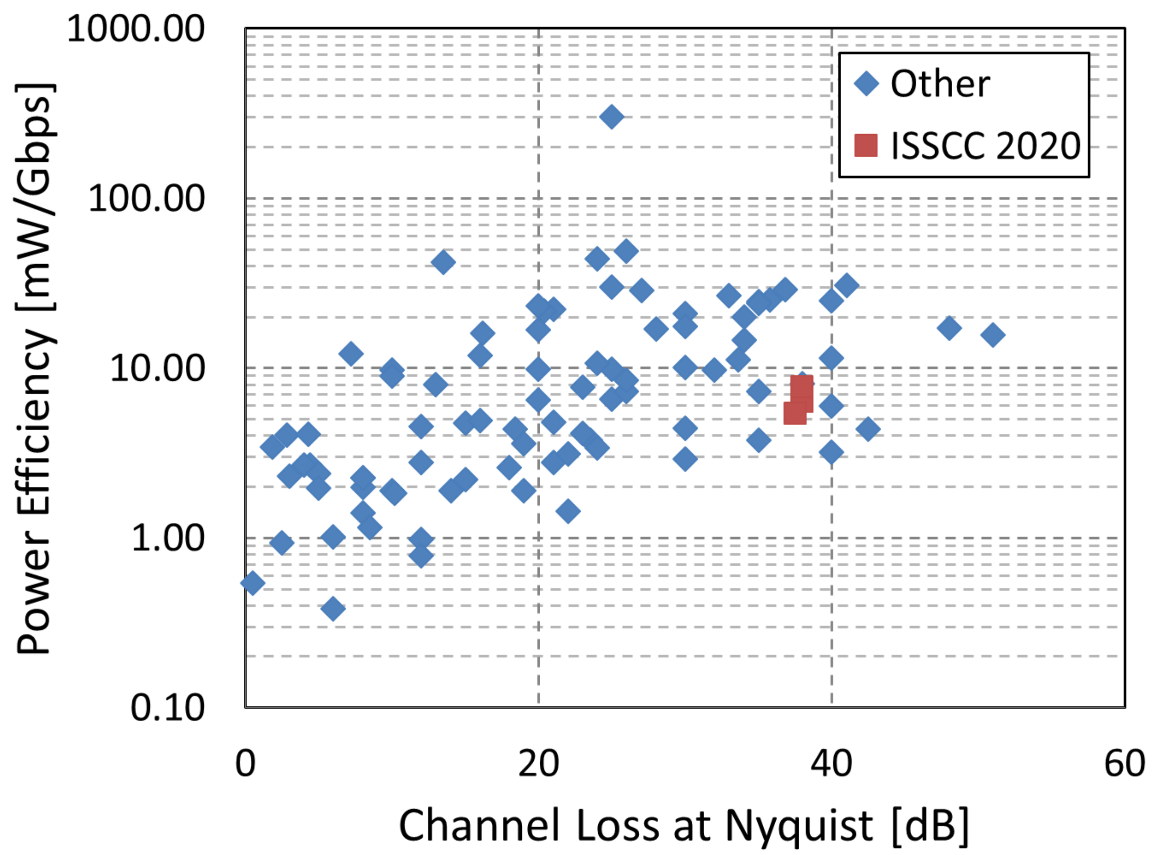

Figure 15: Transceiver power efficiency vs channel loss.

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HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE

DIGITAL CIRCUITS SUBCOMMITTEE

MACHINE LEARNING & AI SUBCOMMITTEE

Digital Architectures & Systems (DAS) – 2020 Trends

Subcommittee Chair: Thomas Burd, *Advanced Micro Devices, Santa Clara, CA*

This year, ISSCC 2020 features a plethora of flagship industry processors, covering the range of servers, desktops, mobile application processors, and automotive processors ranging from 28nm to 7nm CMOS. Additionally, there are invited industry papers on GPUs (a first for ISSCC), an FPGA, an industry full-3D mobile processor, and a next-generation high-performance ARM core. The trend continues to\`exploit multi-chip integration technologies to drive core count and on-die cache.

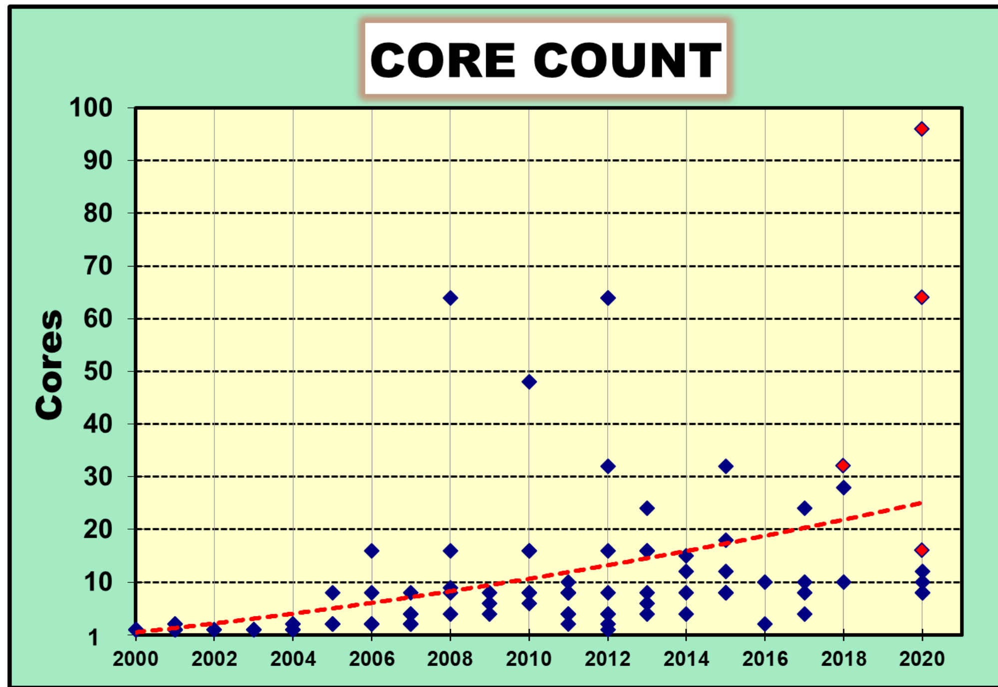

Figure 16: Core-count trends (red diamond designates multi-chip module).

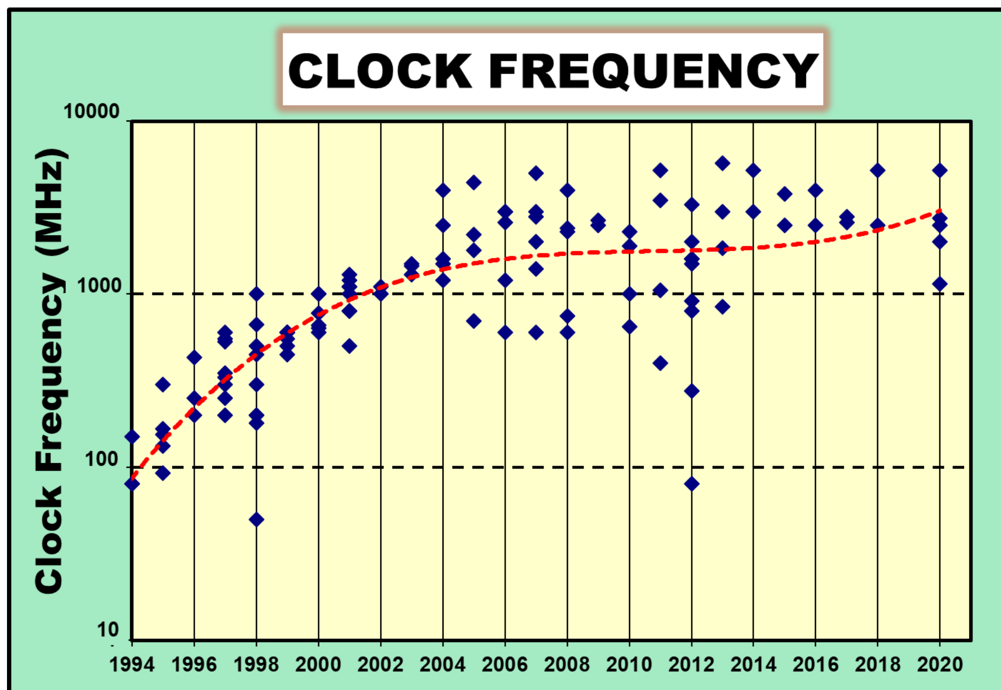

Figure 17: Clock-frequency-scaling trends.

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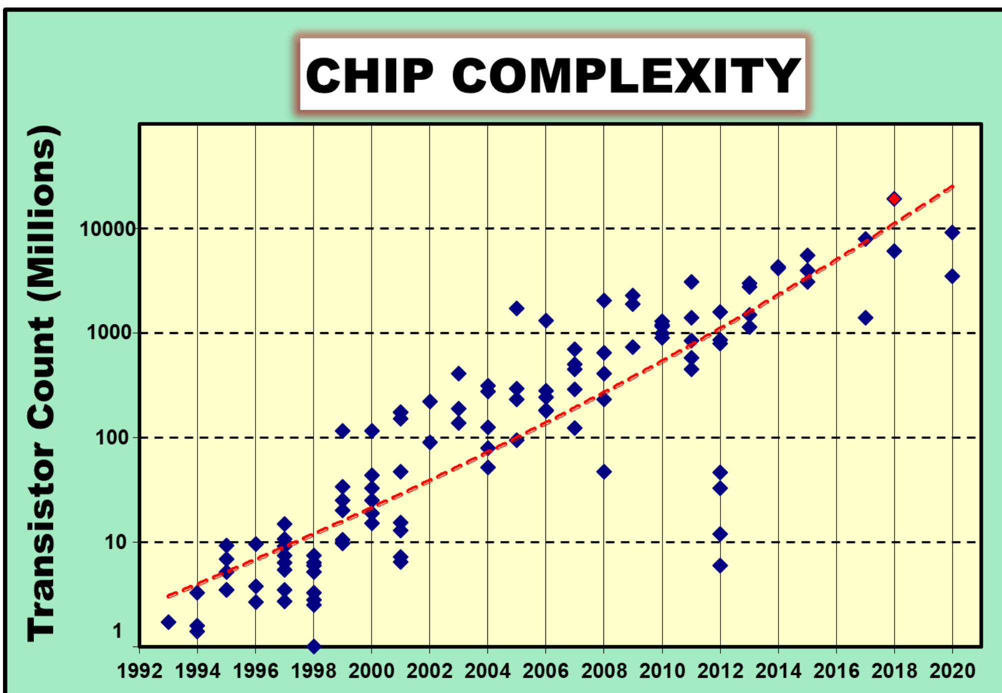

Figure 18: Chip-complexity-scaling trends (red diamond designates multi-chip module).

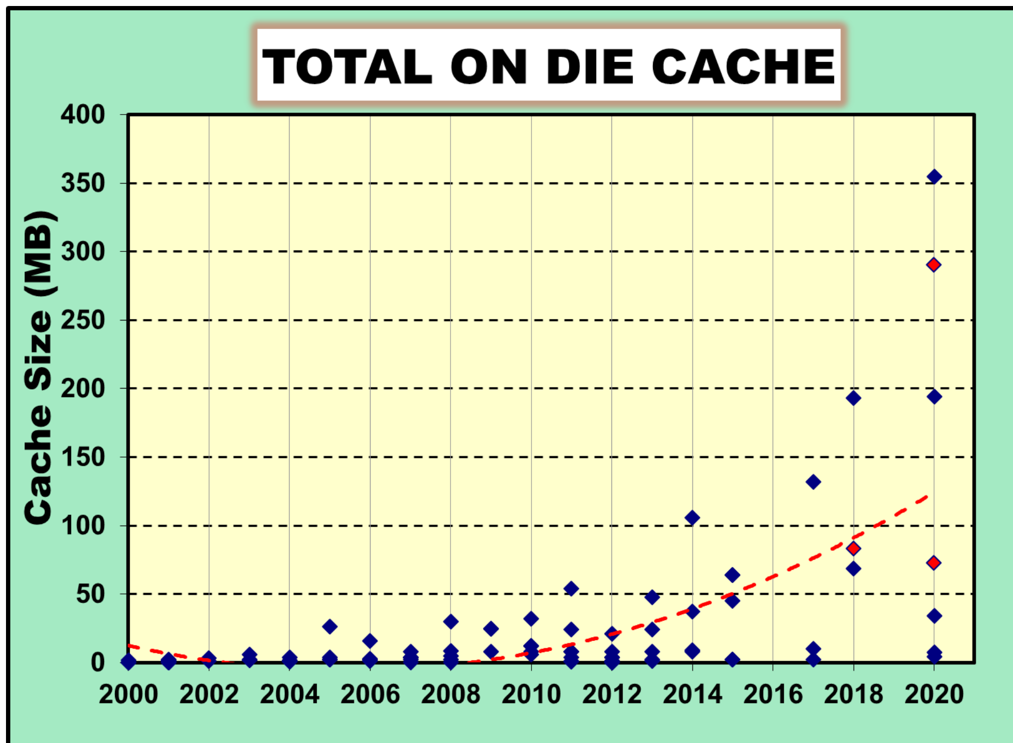

Figure 19: On-die cache-size trends (red diamond designates multi-chip module).

The computational performance of mobile AP (Application Processor) SoCs has historically grown, as silicon process technology advances. AP SoCs continue to add more features, including 5G modems, multimedia IP cores and accelerators on-chip to enhance functionality. Mobile phones continue to add additional camera sensors which drives additional complexity onto SoCs. Dedicated neural-network accelerators execute machine-learning functions faster and with higher-energy efficiency than generic CPUs and GPUs. Neural-network processing units (NPUs) will be adopted in most future AP SoCs, establishing an important future direction, where an efficient software solution utilizes heterogeneous computing combining CPUs, GPUs, and NPUs. On-device training features continue to be incorporated for security of private data and device personalization.

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Category	Entries (in chronological order)
Graphics	OpenGL (ES1.1) / OpenGL/VG/MAX (ES2.0) / AR (Augmented Reality) / VR (Virtual Reality) Vulkan
Display	VGA / WVGA @ 60fps / SXGA @ 60fps / WQXGA/WQXGA+ @ 60fps / WQXGA/WQXGA+ @ 60fpsx2 (VR) / WQXGA/WQXGA+ @ 120fps
Camera	5~8M / 10M / 16M / 20M / 24M / 12MxDual 360° VR / 16MxDual 3D Depth / AR / 80M Tripple
Image/Video	H.264/AVC (VGA) / H.264/AVC (D1) / H.264/AVC (Full HD) / H.264/MVC H.264/SVC / H.265/VP9 / H.265/VP9 HDR / AV1 HDR10+
Audio	AAC / AAC Plus / WMA Dolby 5.1 / Dolby TrueHD/Digital+ / DSD Dolby Atmos / TWS Truly Wireless
Accelerator	FPU / SIMD Multi core (2-4) / Multi core (4-8) / Heterogeneous Multi-Processing / Neural-net Processor / 5 TOPS
downlink [Mb/s]	UMTS 0.4- 2 / HSPA 1.8 - 7 / HSPA+ 7 - 42 / LTE 100 / LTE-A 150-750 / LTE-A 1600 / LTE-A 2000 / 5G 5000
CPU [MIPS]	300 500 / 500 800 / 800 2400 / 2400 6000 / 6K 12K / 12K 100K / 13K 112K / 19K 162K / 22K 180K
Year	2007 / 2008 / 2009 / 2010 / 2011 / 2012 / 2013 / 2014 / 2015 / 2016 / 2017 / 2018 / 2019 / 2020

Figure 20: Application-processor trends in smart phones.

Wired and wireless links continue to increase in bandwidth with a trend of 10× higher data rates every five years. Changes are modest this year at ISSCC 2020 relative to last year. mm-wave and massive MIMO technologies are being actively studied to realize 5G communication. The first 5G mobile device will be commercialized in 2019. The explosion of IoE devices will require the evolution of narrow-band wide-area networks.

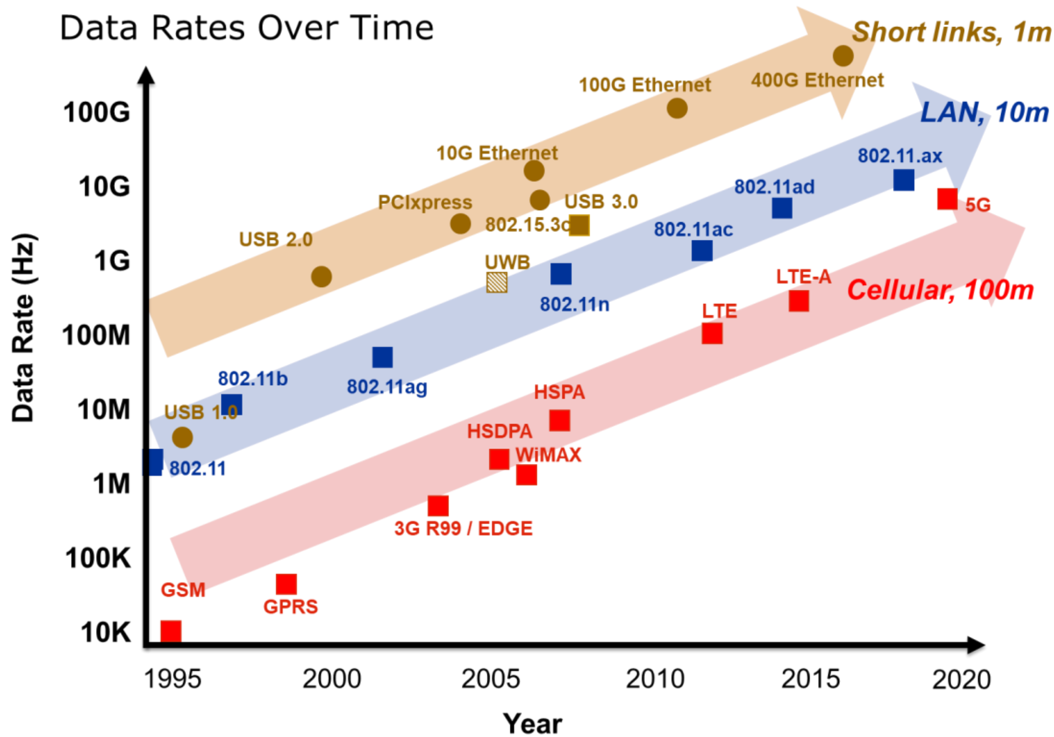

Figure 21: Data-rate trends in wired, wireless, and cellular.

Circuits for Hardware Security: With the increasing risk and cost of information theft, hardware-implemented security has become a common circuit component. Though focus on cryptographic implementation continues, cost-effective PUFs (Physically Unclonable Functions) are now a focus area, such as in smart cards, consumer devices, and automotive applications. TRNGs (True Random-Number Generators) are also commonly leveraged to strengthen secret key generation in cryptographic applications.

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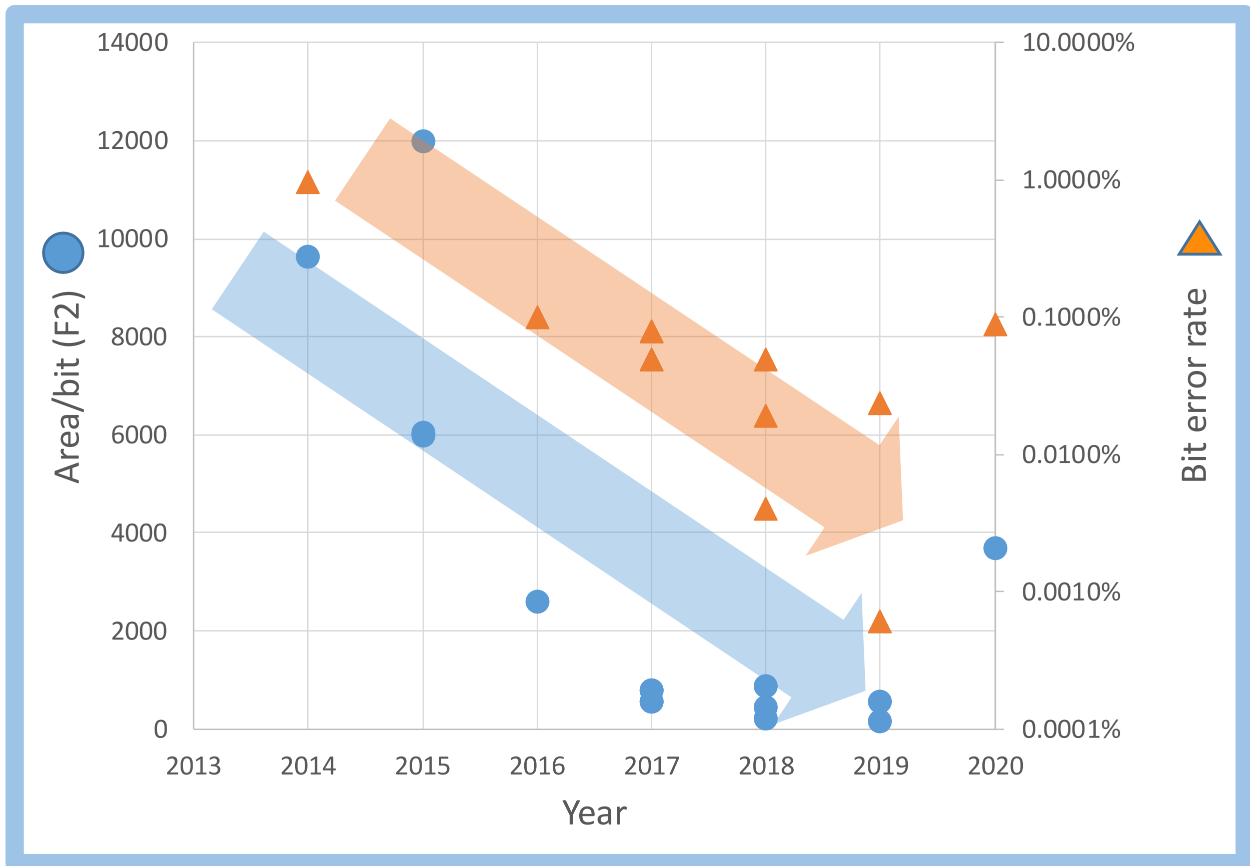

Figure 22. Area/bit and bit-error-rate trends for physically unclonable functions (PUFs) published recently at ISSCC

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Digital Circuits – 2020 Trends

Subcommittee Chair: *Edith Beigne, Facebook, Menlo Park, CA*

Demand for higher performance across ubiquitous, connected, and energy-constrained platforms, ranging from Internet of Everything (IoE) to cloud data-centers, continues to drive innovations in all CMOS digital-circuit building blocks, with goals of improving energy efficiency and performance, lowering cost/design effort, and enhancing security. Classic technology scaling has slowed and circuit design efforts are exploiting technology features, such as body biasing and passive-device advancements, to enable circuit innovation. In addition, variation mitigation has become a major trend in digital circuits in order to improve robustness and power efficiency across Process, Voltage, and Temperature (PVT). Specifically, all-digital sensors and adaptive (clocking) techniques continue to be proposed to mitigate these effects on-chip, with the goal of reducing PVT margins and enable circuit-driven chip-level performance gains.

A trend towards application-specific accelerators is leading to the development of new circuit techniques that benefit a range of emerging applications, such as navigation in micro-robotics, DNA sequencing engines, and annealing processors for solving large combinatorial problems. Some of these accelerators leverage compute-in-memory strategies, while others rely on circuit operation in non-conventional modes/domains, such as time-domain or charge-domain computation.

Integrated Voltage Regulators: At ISSCC 2020, energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off-chip, have increasingly been integrated on-chip to reduce cost. Low-dropout (LDO) linear regulators, switched-capacitor voltage regulators (SCVR), and even inductor-based buck voltage regulators (LCVR) are integrated in scaled process nodes to enable faster and fine-grain dynamic voltage and frequency scaling (DVFS) of individual functional blocks. In turn, the low voltages supported in DVFS systems necessitate a move from analog-based LDOs to digital implementations. There is a recent movement towards making these digital LDOs synthesizable, reducing design effort and easing portability. Another trend is towards hybrid LDOs that incorporate the best features of both analog and digital designs. Figure 23 shows the conversion efficiency and current density of these integrated voltage regulators, which continues to improve.

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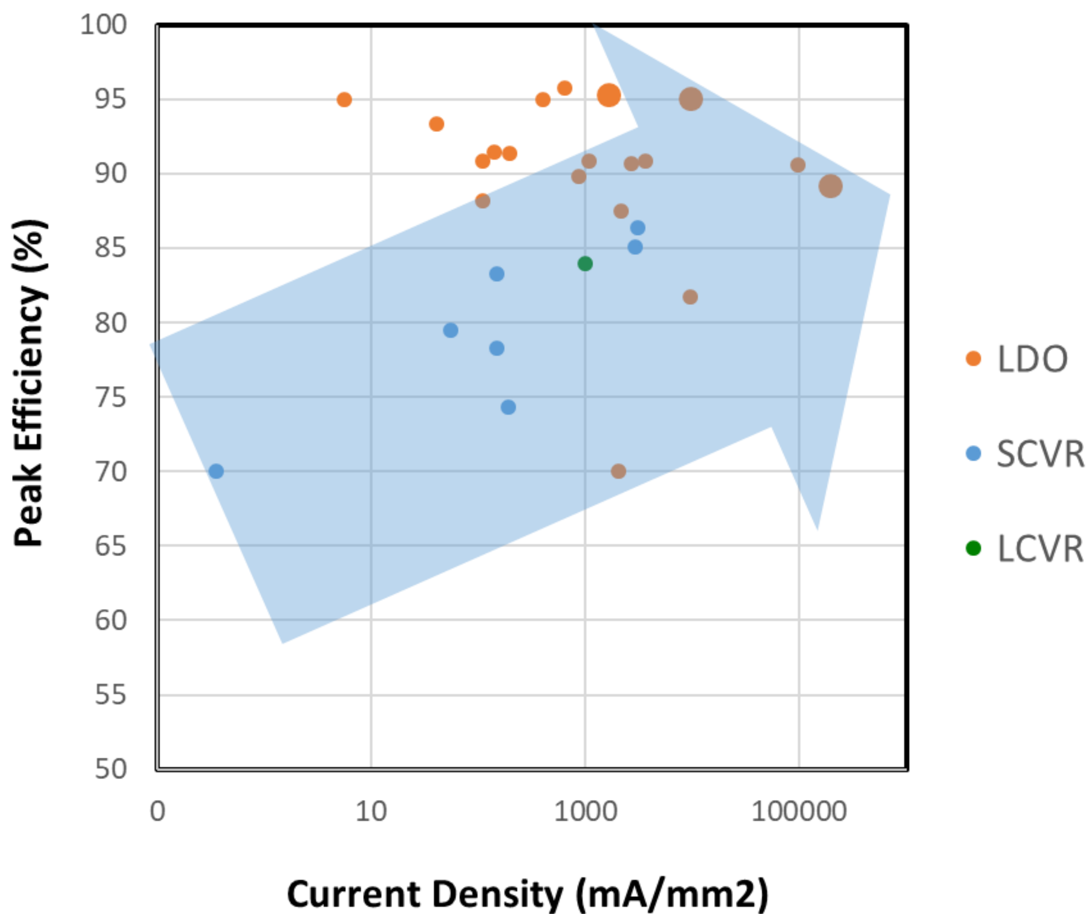

Figure 23. Integrated voltage regulators (large LDO symbols represent 2020 papers).

Synthesizable Digital PLLs for Low-Jitter Applications: PLL trends include migration from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for compact low-jitter PLLs is increasing. The use of more-automated digital design flows (such as synthesis and automated placement and routing) dramatically reduces development costs, but can degrade jitter, requiring new techniques to compensate. Figure 24 highlights metrics for PLLs and DPLLs published at ISSCC over the past ~10 years. The plot shows the relationship between reference (input) frequency and figure-of-merit, demonstrating the tradeoff between cost (higher-reference frequency) and overall PLL performance.

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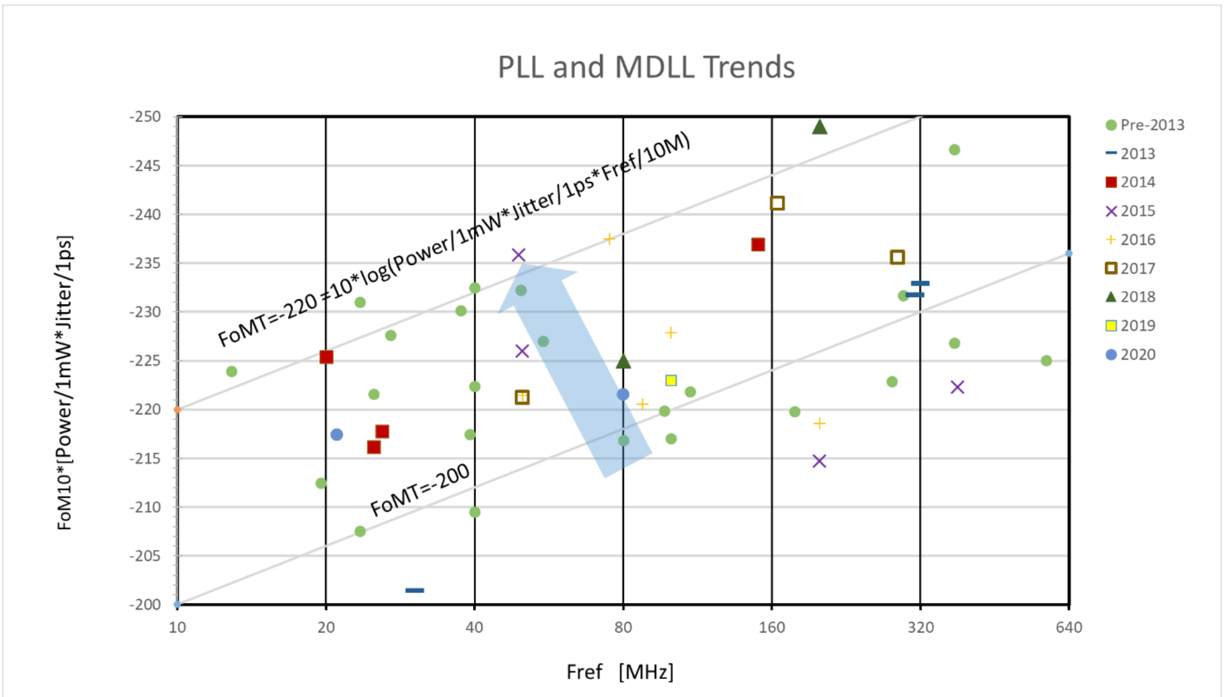

Figure 24. PLL and Multiplying-Delay-Locked Loop (MDLL) trends.

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Machine Learning (ML) & AI – 2020 Trends

Subcommittee Chair: Marian Verhelst, KU Leuven, *Heverlee, Belgium*

Owing to the world-wide trend of deep learning enthusiasm in recent years, ISSCC 2020 has established a dedicated subcommittee to machine learning and AI. As deep-neural networks succeed in getting better accuracy on a wide variety of tasks, their computational complexity also keeps rising. Both for datacenter, mobile, and IoT workloads, this results in continuous demand for more-energy-efficient and higher-throughput neural-network computing. This year's submissions have targeted these objectives across a broad power spectrum, ranging from 0.5μW always-on accelerators to 276W datacenter AI processors.

It is important to note that the metrics that matter at the system level are energy/inference and inference/s for a specific task and a given inference accuracy. This year's submissions again significantly push the state-of-the-art of these efficiency and throughput numbers, by combining multiple enhancement techniques in tandem within a single chip, implemented in the most-advanced technology (Figure 25):

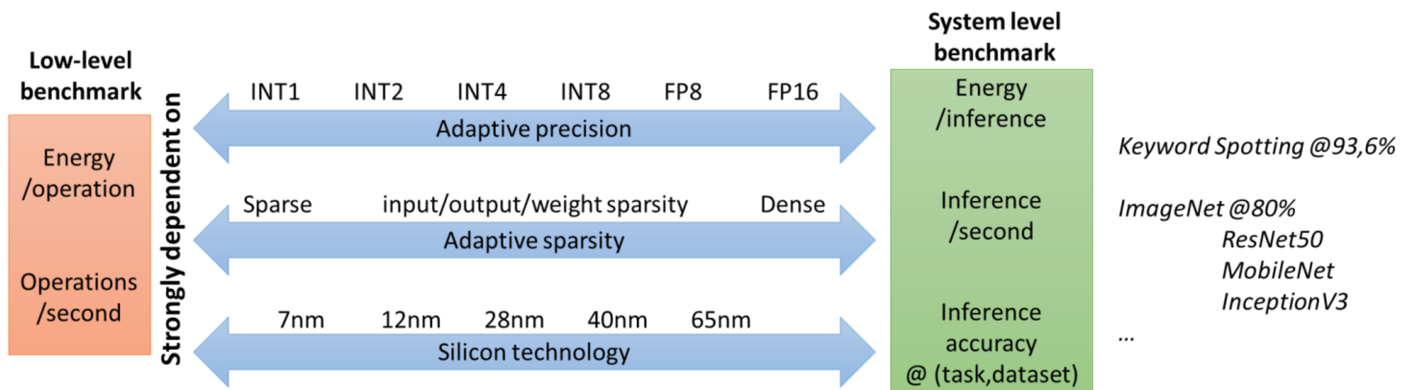

Figure 25: Various parameters impacting low level and system-level benchmarking metrics.

1.) Support for different levels of computational precision is almost omnipresent now, in order to efficiently support multiple tasks. In addition to fixed-point accuracies between 2b-to-8b, some architectures also support FP8 and FP16 for training, as well as pixel manipulation workloads.

2.) It is clear that the exploitation of sparsity has become a common theme, which boosts throughput between 2×-to-4× and energy efficiency up to an order-of-magnitude. In fact, more than 50% of the techniques at ISSCC 2020 specifically leverage input, output, and/or weight sparsity as one of the key innovations. We further see an increase in the number of approaches concerned with multi-bit in-memory computing, gradually perfecting the resolution and accuracy, as well as energy efficiency. A particular challenge in that context is to combine the exploitation of sparsity with in-memory computing, a topic that will also be addressed.

3.) At ISSCC 2020, it can be noted, in general that machine learning processors are increasingly realized in the most-advanced technology, with chips exploiting 7nm and 12nm.

As different chipsets are often characterized on a different set of tasks, network topologies, and accuracy levels, comparing the true system-level benchmarking metrics, such as energy/inference and inference/s, is not always straightforward. It is therefore interesting to look at the achieved low-level metrics of operations/s and energy/operation within the neural network, as illustrated in Figure 26 for the new datapoints of ISSCC 2020, compared to the state-of-the-art in 2018 and 2019. Yet, one should be well aware that these TOPS/W and TOPS/s are strongly dependent on the exercised neural-network topologies, computational precision, and network sparsity. Going forward, as the field matures, we believe that a common benchmarking methodology must be established, accounting for the application context. Yet, without any doubt, the clever combination of sparsity, variable precision, and in-memory computing technologies enables continued enhancement of deep-learning processor efficiency and throughput.

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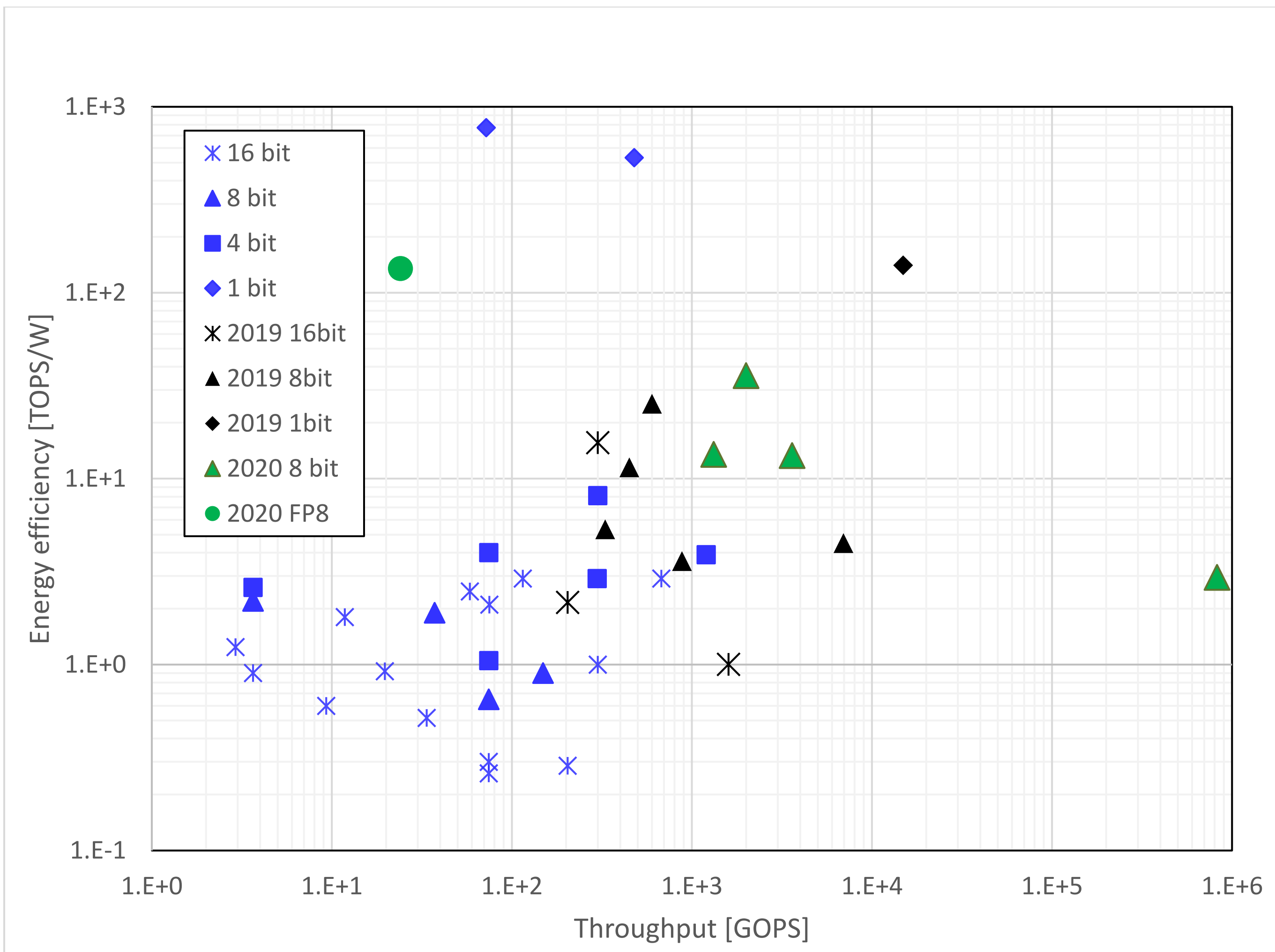

Figure 26: Deep-learning processor throughput and efficiency.

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Memory – 2020 Trends

Subcommittee Chair: *Jonathan Chang, TSMC, Hsinchu, Taiwan*

The demand for high-density, high-bandwidth, and low-energy memory systems continues to grow everywhere from high-performance computing to SoC, wearables, and IoT.

This year, ISSCC 2020 presents the first 5nm FinFET SRAM. Compute-In-Memory (CIM) boosts the performance and energy efficiency of multiplication-and-accumulation (MAC) operations in 7nm SRAM, as well as in a leading-edge 22nm ReRAM. In DRAM the performance of HBM2E is extended to 640GB per cube, and to 8.5Gb/s for LPDDR5 components. For NAND, the lowest latency is reported as well as a QLC NAND with the highest program bandwidth ever reported. For STT-MRAM the highest read bandwidth ever, is shown, as well as the first near-memory STT-MRAM. The increasing number of papers on high-speed memory interfaces emphasizes the trend to push memory bandwidth limits further.

Papers of note at ISSCC 2020 include:

- A 5nm 135Mb SRAM in EUV and high-mobility-channel FinFET technology with metal coupling and charge sharing write-assist circuitry schemes for high-density and low-V_{MIN} applications.
- A 351TOPS/W and 372.4GOPS compute-in-memory SRAM macro in 7nm FinFET CMOS for machine-learning applications.
- A 1.1V 16GB 640GB/s HBM2E DRAM with a data-bus-extension technique and a synergetic on-die scheme.
- A 8.5Gb/s and /pin 12Gb LPDDR5 SDRAM with hybrid bank architecture, skew-tolerant scheme, low-power scheme, and speed-boosting techniques.
- A 128Gb 1bit/cell 96-word-line-layer 3D flash memory to improve random-read latency with t_{PROG}=75µs and t_R=4µs.
- A 32Gb/s digital-intensive single-ended PAM-4 transceiver for high-speed memory interfaces with a 2-tap time-based decision feedback equalizer.
- An 8nm 18Gb/s/pin GDDR6 PHY with TX bandwidth extension and RX training technique.
- A 22nm 2Mb ReRAM computing-in-memory macro with 121-28 TOPS/W for multibit MAC computing for tiny AI edge devices.
- A 22nm 1Mb 1024b-read and near-memory-computing dual-mode STT-MRAM macro with 42.6GB/s read-bandwidth for security-aware mobile devices.

SRAM

Scaling in SRAM continues and the first 5nm FinFET EUV SRAM is presented. Innovations in SRAM continue to support highest density, compute-in-memory (CIM), highest energy efficiency, and applications with very-low latency requirements. Shifting computation inside the memory array (CIM) is a leading approach enabling breakthroughs in energy efficiency and throughput. Four SRAM (with CIM) papers are presented, with the potential of enabling further breakthroughs for AI and deep-learning (DL) applications, featuring low-power and/or high-performance operation, high-accuracy in-memory, multi-bit MAC operation, and the ability to run forward as well as backward calculations for inference and training. Figure 26 shows the SRAM bit-cell area and V_{MIN} scaling trend.

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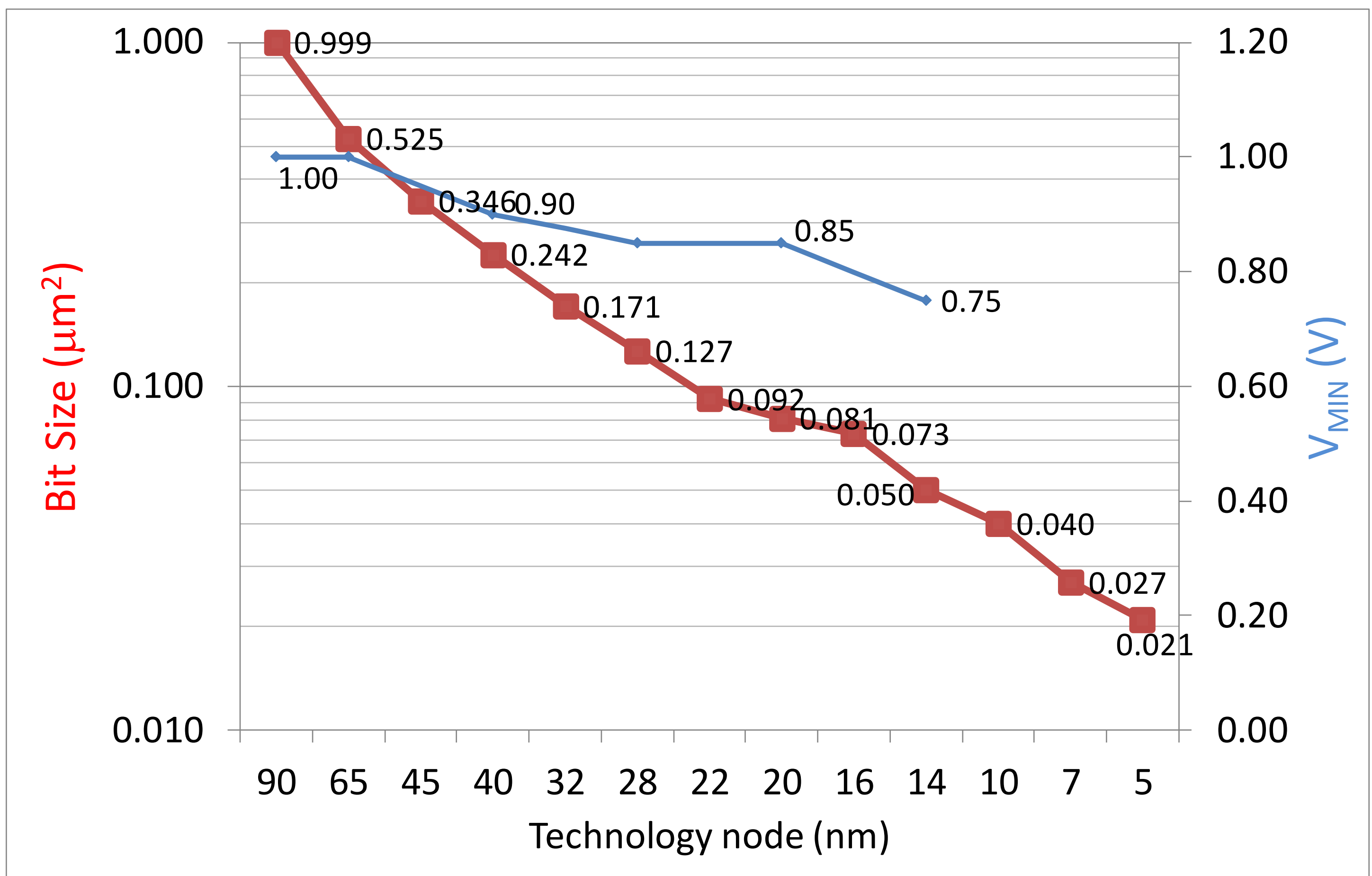

Figure 27: Bit-cell area and V_{MIN} scaling trend for SRAM.

HIGH-BANDWIDTH AND LOW-POWER DRAM

In order to keep pace with the ever-increasing performance requirements in various applications from mobile to super-computing, DRAM continues to scale density, form factor, and bandwidth. This year, ISSCC 2020 include benchmarks for the latest interface standards, such as a 8.5Gb/s LPDDR5 for high-speed mobile and a 640GB/s HBM2E for highest-performance applications (cloud or AI). Three papers focus on improvements for very-high-speed interfaces, such as a PAM4 32Gb/s transceiver and a 18Gb/s GDDR6 PHY. Figure 28 shows DRAM Bandwidth scaling over the last 12 years.

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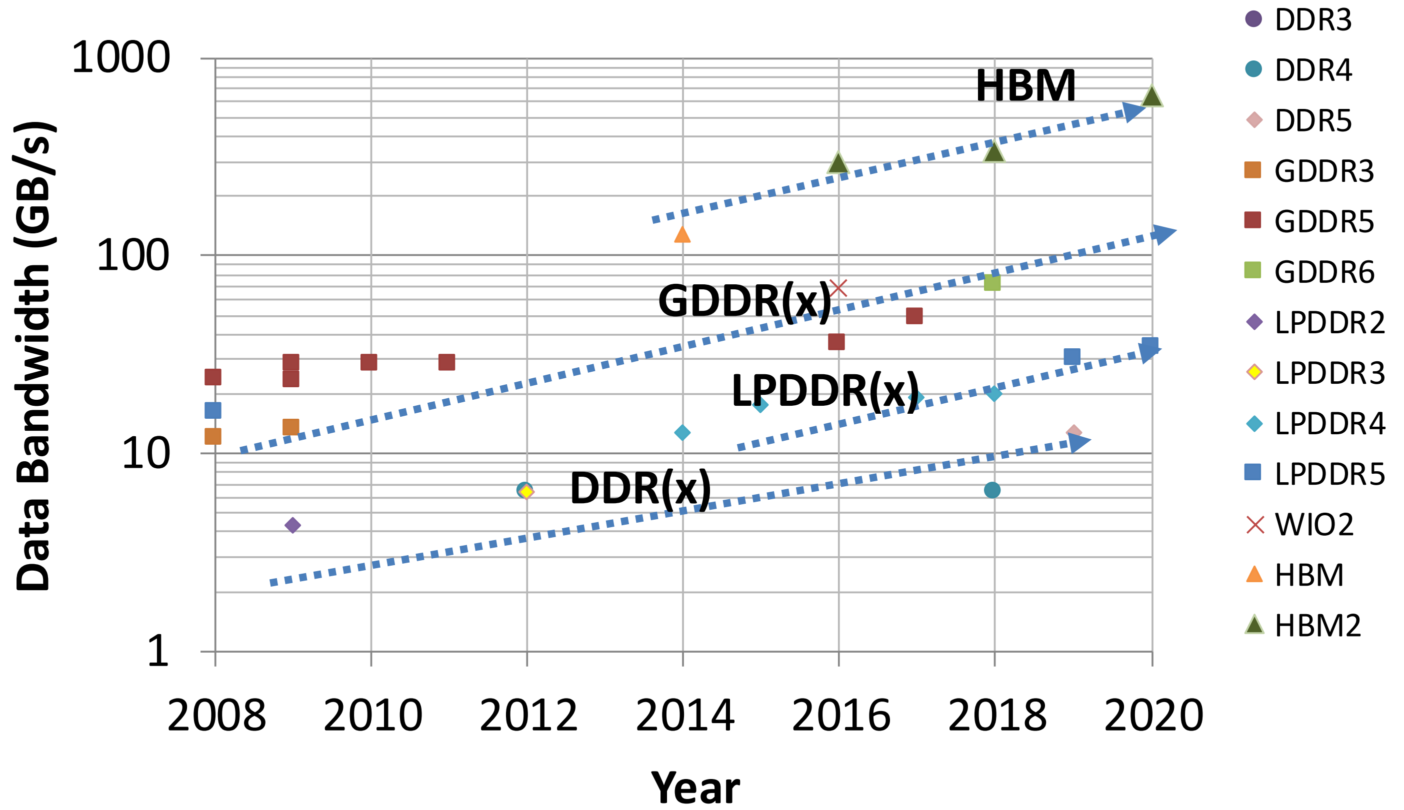

Figure 28: DRAM data bandwidth trends.

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NONVOLATILE MEMORY (NVM)

In the past decade, significant investment has been put into the emerging memories field to find an alternative to floating-gate-based nonvolatile memory. The emerging NVMs, such as phase-change memory (PCM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations.

This year at ISSCC 2020, a 22nm 1Mb STT-MRAM macro demonstrates high-read bandwidth of 42.67GB/s, while a 4b/cell NAND improved the write bandwidth up to 30MB/s.

Figure 29 highlights the achievement of MRAM read bandwidth, as well as the improvement of the 4b/cell (QLC) NAND flash write throughput. Such high densities are achieved through advancements in 3-dimensional vertical bit-cell stacking and multi bits (2-4bits) per bit-cell technologies.

Figure 30 shows the trend of the nonvolatile memory capacity.

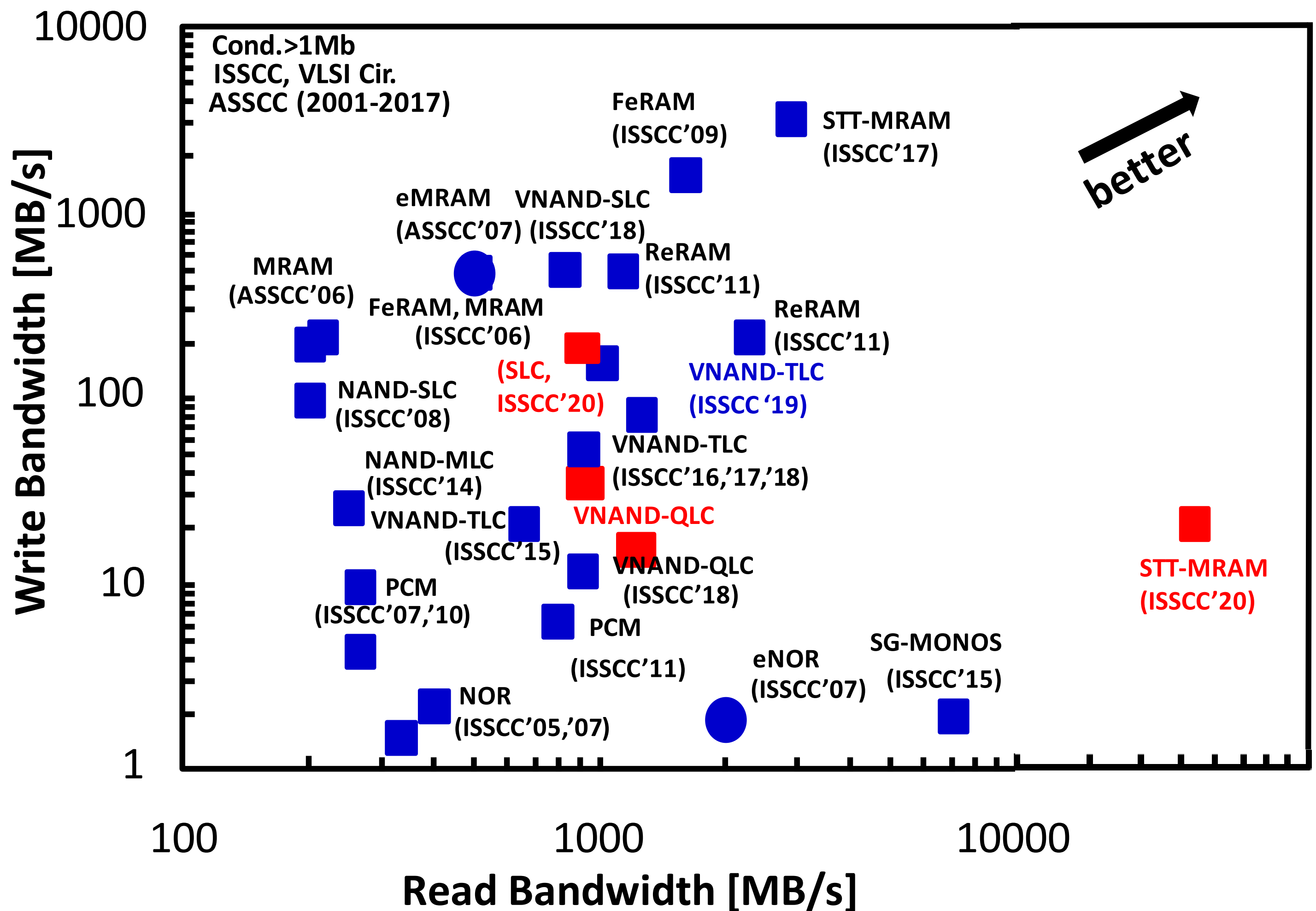

Figure 29: Read/write bandwidth comparison of nonvolatile memories.

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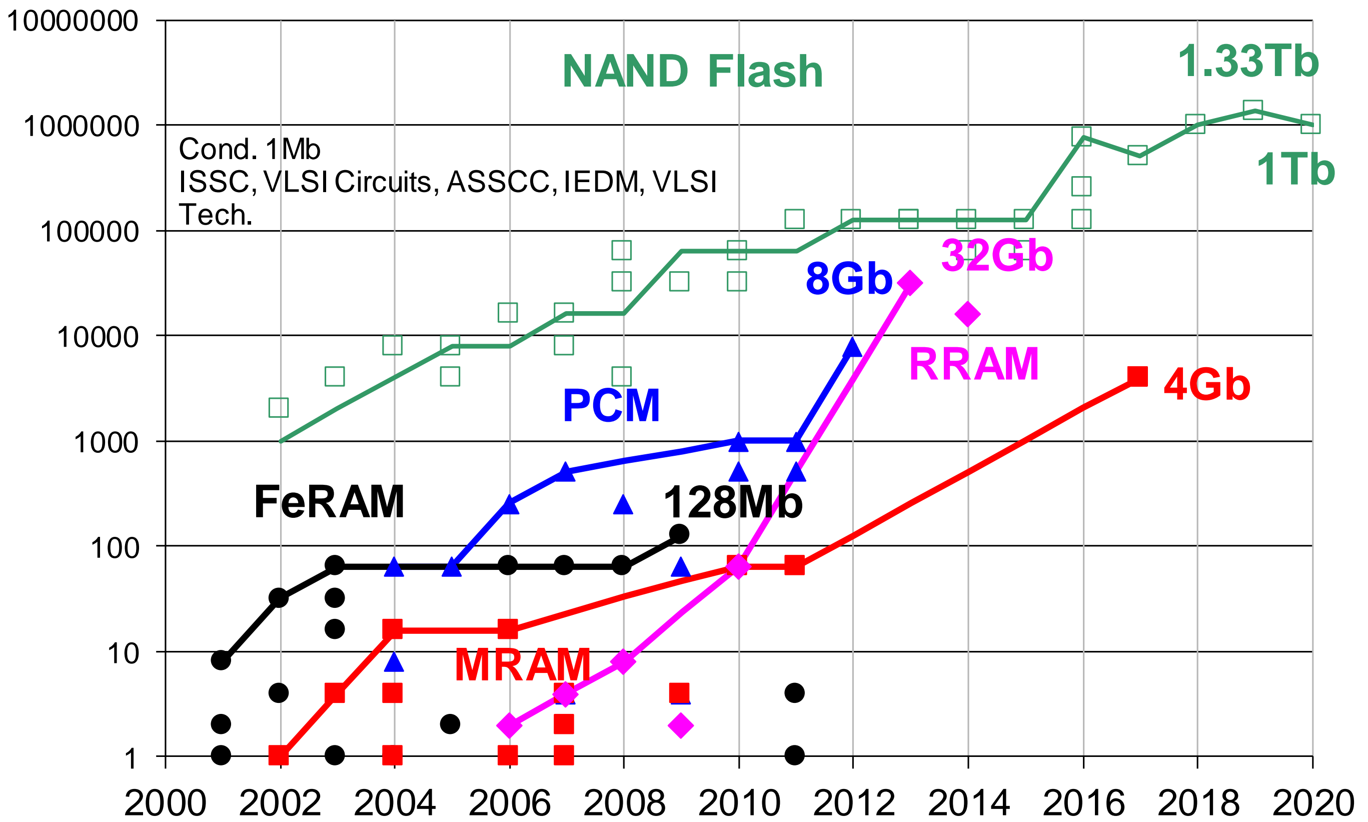

Figure 30: Memory capacity trend of emerging nonvolatile memories.

NAND FLASH MEMORY

NAND flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs).

3D memory technology has been the mainstream for NAND flash memory in mass-production in the semiconductor industry. This year at ISSCC 2020, two papers improving the write bandwidth of 4b/cell 3D NAND flash are demonstrated at 1Tb capacities. One is a 92-stacked-WL 3D V-NAND flash memory featuring 5th-generation technology with 1.2Gb/s high-speed interfaces. Another exhibits 30MB/s program throughput utilizing the highly area-efficient technology of peripheral circuits under the memory cell array which achieves an 8.4Gb/mm^2 area capacity.

On the other hand, fast speed 3D NAND with 75µs program time and 4µs read latency was developed. With a flexible suspend operation for program and erase, a smaller random read latency of under 50µs is achieved.

Figure 31 shows the observed trend in NAND Flash capacities at ISSCC over the past 20 years.

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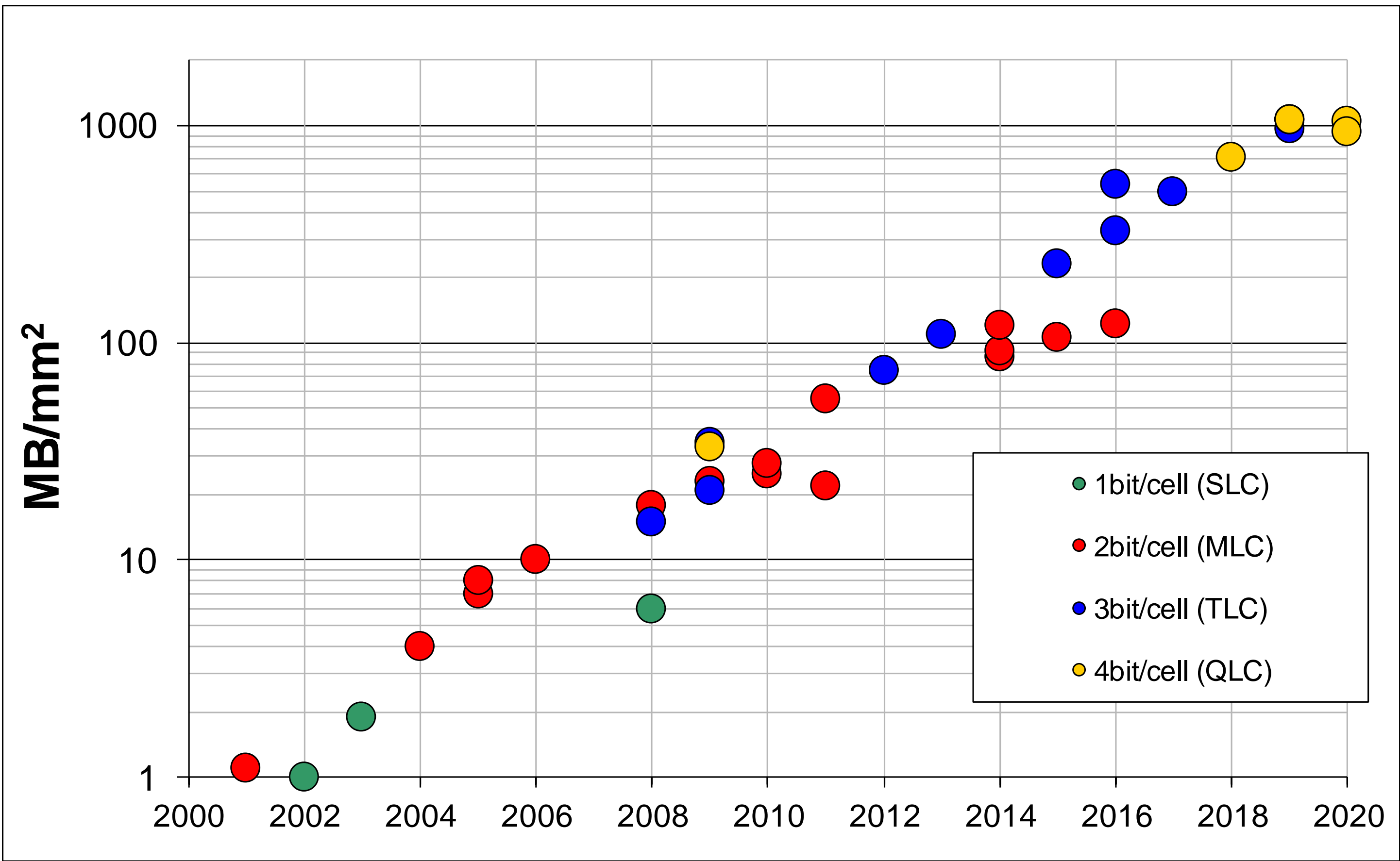

Figure 31: NAND flash memory trends.

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HISTORICAL TRENDS IN TECHNICAL THEMES

Innovative Topics

Imagers/MEMS/Medical/Displays Subcommittee

Technology Directions Subcommittee

IMMD – 2020 Trends (Medical)

Subcommittee Chair: *Chris Van Hoof, IMEC, Leuven, Belgium*

As illustrated at ISSCC 2020, both sensor and actuator systems for on-body wearable and in-body implantable use continue to evolve toward more robust, functionally complex, and energy-efficient solutions, as well as closed-loop operation. Wearable and implantable SoCs record weak biopotential signals in the presence of real-life interference and under stringent power and size constraints. These new SoCs and corresponding techniques for wireless power/data transfer pave the way toward robust microdevices that involve direct sensing, multi-sensor fusion, and implantable closed-loop sensor/actuator systems. These advancements enable multimode physiological recordings from nearly every major organ system.

The state-of-the-art in biomedical integrated circuits and systems has further advanced this year at ISSCC 2020 with miniaturization, higher sensitivity, higher dynamic range, and interference mitigation as major trends in both implantable and *in vivo* diagnostic devices, while continuing to improve power efficiency. High-dynamic-range sensing systems (>100dB) improve tolerance to large-amplitude interference and motion artifacts, while new techniques are introduced to sense physiological signals such as PPG and ECG. Miniaturization combined with a high level of integration enables minimally invasive implants with low tissue displacement for interfacing with the body.

Multi-modal physiological sensors have the potential to offer improved monitoring and diagnosis of a number of chronic conditions. The form factor of a low cost, easy to use, wearable device will enable continuous monitoring of multiple vital signs, allowing health tracking outside the hospital. These advances offer tremendous market potential in both the medical and consumer market spaces.

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IMMD – 2020 Trends (Imagers)

Subcommittee Chair: *Chris Van Hoof, IMEC, Leuven, Belgium*

The CMOS image-sensor business remains one of the fastest-growing segments of the semiconductor industry, expected to reach $18 billion USD in 2024 from $11.8 billion in 2018. Image sensors are essential components in mobile devices and found in many consumer electronics products. Strong demand for automobile driver assistance and autonomy has continued to drive progress in Time-of-Flight sensors, as well as high-performance 2D imagers. BSI and 3D-stacked processing continue to offer improved performance with increased on-chip functionality and new features being integrated at the pixel level.

At ISSCC 2020, four out of the ten image sensors were designed for direct and indirect Time-of-Flight imaging. Progress has been made in both the spatial and depth resolution over previous designs, leading to longer range and higher accuracy. In Toshiba's LiDAR chip, circuit optimizations facilitate 2× higher channel density in the same die size. Another four image sensors target mainstream applications with improvements in pixel size, global shutter, low noise and high dynamic range. Samsung has scaled down pixel pitch to 0.7μm, while improving or maintaining critical performance parameters. Robust backside illuminated global shutter pixels with -105dB parasitic light sensitivity have been reported. Sony reports noise level improvements with selectable in-pixel gain without adding transistors. A single exposure 132dB dynamic range that maintains high SNR over the full range is presented. Finally, two of the image sensors are intended for low-power low-data-rate applications, with always-on imaging and event-based dynamic vision. Improvements in architecture and data conversion have continued to drive down power consumption, while providing the necessary compression, image quality, and detection for targeted applications.

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Technology Directions – 2020 Trends

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan*

Technology innovations bring the promise of enabling new system functionalities or substantially increasing the efficiency of existing ones. Harnessing such innovations for solving tangible real-world problems requires novel system-level solutions. With a focus on envisioning the future, emerging trends in Technology Directions this year at ISSCC 2020 covers a wide range of topics including quantum engineering, embedded non-volatile memory-based computing devices for next-generation AI architectures, low-power circuits for IoT and health technologies, and biomedical sensing, stimulation, and harvesting. ISSCC 2020 features four sessions representing the latest technological innovations in the following areas:

Quantum engineering: Quantum technologies are emerging as a major multi-disciplinary research topic, including computing, sensing, telecommunications, information technology, and security. Common to these technologies are properties typical of quantum mechanics, such as superposition and entanglement. Recently, engineers have developed techniques to exploit these properties using solid-state circuits, which are employed to control and observe a growing number of quantum devices. Since most quantum devices must be operated at deep cryogenic temperatures, circuits must also operate at these or comparable temperatures, so as to ensure compact, reliable, and, especially, scalable systems. Leveraging over 60 years of CMOS technology development, researchers are increasingly engaged in cryogenic CMOS (cryo-CMOS) circuits and systems to fill this gap. Cryo-CMOS technologies will serve a range of quantum devices that can be used in several quantum engineering problems. ISSCC 2020 will feature a session devoted to some of these topics, including a cryo-CMOS controller for spin and superconducting qubits and an integrated system for the control of a double-quantum-dot, also integrated in CMOS.

Next-Generation Nonvolatile Devices: Nonvolatile devices are enabling novel architectures with improved energy and area efficiencies. A relentless push to intersect evolving artificial intelligence (AI) applications embodies larger scale nonvolatile memory (NVM) based compute-in-memory (CIM) implementations, featuring neural-network processors. The trend continues this year with CIM support for multibit inputs/weights/outputs and low-power parallel data path operations. ISSCC 2020 highlights two resistive random-access memory (ReRAM/RRAM)-based energy-efficient silicon using analog in-memory operation, one with reconfigurable dataflow and the second a fast, parallel multi-bit computation enabled by a signed-weighted ReRAM array.

Low-Power Circuits for IoT & Health: The papers from ISSCC 2020 in this area push the frontiers of lower power solutions in IoT and health applications. One paper presents an ultra-low power IC designed for communicating with commodity WiFi transceivers via backscattering. Another introduces a nano-watt class (54nW) always-on wake-up chip for general-purpose IoT devices. A third describes an electronic nose with very accurate limit-of-detection. In addition, advances in silicon for 3D localization based on magnetic field gradient sensing for surgical implants is presented.

Biomedical Sensing, Stimulation, and Harvesting: ISSCC 2020 includes innovative and emerging biomedical systems for wearables and implantable components for timely medical intervention. The developing trends encompass advances in implantable sensors and stimulators, human-body coupled communication, ambient energy harvesting and utilizing novel magnetoelectric effects for power and data transfer. The technologies demonstrate the promise to advance cancer therapy, neurostimulation, retinal prosthesis, and diagnostic devices.

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INDEX

INDEX

A paper number mentioned in this section follows the convention S.P, where S is the session number and P is the paper number. For example 23.2 will be the second paper in the twenty-third session. You can refer back to the TECHNICAL SESSION OVERVIEWS in this Press Kit for additional details on any given paper. Some of the papers will also be available in the "not-so-technical" SESSION HIGHLIGHTS part of this Press Kit. All sessions and papers are in ascending order in both the Session Overviews and the Session Highlights sections of the Press Kit.

Technical Topics Mapped to Papers

Technical Topic	All papers in the following Sessions
Communication Systems includes Wireless, RF, and Wireline Subcommittees	**4, 6, 10, 12, 17, 18, 24, 29, 30**
Analog Systems includes Analog, Power Management and Data Converter Subcommittees	**3, 9, 11, 16, 23, 32**
Digital Systems includes Memory, Digital Circuits, Machine Leaning and AI, Digital Architectures and Systems Subcommittees	**2, 7, 13, 14, 15, 21, 22, 25, 27, 31**
Innovative Topics includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees	**5, 19, 20, 26, 28, 33, 34**

Selected Presenting Companies/Institution Mapped to Papers

Chart 4.1

Affiliation	Paper Numbers
Advanced Institute of Information Technology of Peking University	20.2
Alibaba	7.2
AMD	2.1, 2.2, 8.4
Analog Devices	16.1, 16.6, 23.3, 29.8, 30.4
Anhui University	14.2
Arizona State University	32.5
ARM	8.3, 27.2
Artilux	5.3

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Bionic Sciences	26.8
Boston University	29.8
Broadcom Inc.	20.1
California Institute of Technology	20.4
Carnegie Mellon University	4.4
Case Western Reserve University	26.7
Catholic Kwandong University	26.6
CEA-IRIG	19.2
CEA-LETI-MINATEC	2.3, 19.2, 32.2, 32.3
Chosun University	29.7
CoilEasy Technologies	18.4
Columbia University	4.3, 14.1, 25.8, 29.3, 29.4
Dartmouth College	11.2
Delft University of Technology	3.4, 3.6, 19.1, 19.3, 23.4, 23.6, 28.1
Emory University	28.4
EPFL	14.1, 19.1, 19.3
ETH Zürich	3.3, 26.9
Everactive	27.1
Fudan University	24.5
Georgia Institute of Technology	4.2, 15.2, 24.1, 24.2, 24.3, 24.6, 26.8, 27.3, 28.4, 31.1
Hangzhou Nuowei Medical Technology	26.3
Hitachi	7.3, 9.7
Hokkaido University	7.3
Hong Kong Applied Science and Technology Research Institute	30.3
Hong Kong University of Science and Technology	4.7
IBM Systems and Technology	2.7
IBM T. J. Watson Reseach Center	2.7

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imec	16.3, 17.7, 30.6, 30.8
imec - Ghent University	12.4
Indian Institute of Technology Madras	16.6
Industrial Technology Research Institute	15.2
Infineon Technologies	17.2, 17.5
Intel	4.5, 8.1, 10.5, 12.1, 19.1, 19.3, 25.1, 25.5, 25.7, 25.9, 27.3, 28.4
Intel Labs	27.3
KAIST	7.4, 11.8, 17.1, 17.3, 17.8, 29.7
KIOXIA	13.5
KIOXIA Systems	13.5
Kochi University of Technology	33.3
Krembil Neuroscience Center	26.2
KU Leuven	24.7, 29.2, 29.6
Kyoto University	33.3
Lawrence Berkeley National Laboratory	28.4
Leading UI	28.1
Leibniz University Hannover	11.3, 18.2
M31 Technology	15.5
Massachusetts Institute of Technology	4.8, 29.4, 29.5, 29.8
MediaTek	2.5, 6.2, 7.1, 9.1, 10.3, 10.4, 10.6, 21.3, 26.1
Mentor	2.3
Michigan State University	10.7, 24.4, 26.8
Microelectronic Circuits Centre Ireland	17.6
N.1 Institute for Health	34.2, 34.5, 34.6
Nanyang Technological University	31.2
National Cheng Kung University	16.4, 23.5
National Chiao Tung University	3.8, 21.1

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National Taiwan University	21.1, 21.2, 25.6
National Tsing Hua University	5.9, 13.4, 14.3, 15.2, 15.4, 15.5, 33.2
National University of Singapore	23.2, 34.2, 34.5, 34.6
NEC	33.3
North Carolina State University	26.8
Northwestern University	31.3
now with Analog Devices	27.1
NTT	12.3
NVIDIA	6.6
NXP Semiconductors	9.8, 23.4
Oregon State University	4.3, 10.7, 26.5
Osaka University	33.3
Panasonic	5.2
Peking University	20.2
Pi2star Technology	14.2, 14.3
Politecnico di Milano	17.2, 17.5
Princeton University	4.6, 29.9
PROPHESEE	5.10
Purdue University	27.3
Qualcomm	17.8
Rambus	6.3
Rayence	28.3
Realtek Semiconductor	3.8
Renesas Electronics	9.7, 30.6
Rice University	4.2, 25.3, 28.4, 34.3
Richtek	18.5
Ritsumeikan University	33.3
Robert Bosch	23.1

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Samsung Electronics	2.4, 4.1, 5.5, 5.6, 6.4, 11.7, 11.8, 13.1, 18.6, 20.3, 22.1, 22.2, 22.5, 23.8, 27.4, 30.2, 34.6
San Jose State University	6.3
Science and Technology on Monolithic Integrated Circuits and Modules Laboratory	24.8
Sentron	28.2
Seoul National University	6.5, 6.7, 18.6, 22.6, 25.2, 32.4
Shanghai Jiao Tong University	25.8
Sharif University of Technology	4.7
SiTime	3.2
SK hynix	13.2, 22.3, 22.6, 28.1
Sony Electronics	5.10
Sony LSI Design	30.5
Sony Semiconductor Manufacturing	5.7
Sony Semiconductor Solutions	5.10, 5.7, 5.8, 30.5
Sookmyung Women's University	11.6, 32.1
Sorbonne University	2.3
South China University of Technology	11.5
Southeast University	14.1
Stanford University	26.4, 33.1
STMicroelectronics	2.3, 12.2
Sungkyunkwan University	5.4
Taiwan Semiconductor Research Institute	3.8, 21.1
Teletrx	6.8
Texas Instruments	2.6, 3.1, 11.1, 18.2, 18.3, 32.5
Tianjin University	24.8
TNO	19.1
Tokyo Institute of Technology	7.3

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Toronto Western Hospital	26.2
Toshiba	5.1, 18.7, 18.8
Toshiba Electronic Devices & Storage	5.1
Tsinghua University	9.3, 9.5, 14.2, 14.3, 16.5, 33.1, 33.2
TSMC	13.3, 15.1, 15.3
Ulsan National Institute of Science and Technology	5.4, 17.1, 17.3, 17.8
Universidad Politécnica de Madrid	4.8
Université Savoie-Mont Blanc	32.2
University College Dublin	17.6, 30.8
University of Alberta	6.3
University of California	4.7, 33.1, 34.1, 34.4
University of California, San Diego	20.1
University of Electronic Science and Technology of China	15.5, 17.4, 18.4, 23.7, 25.4
University of Illinois	3.5, 3.7
University of Lisboa	9.6, 10.1, 11.5, 16.2, 16.3, 17.9
University of Macau	9.6, 10.1, 11.5, 16.2, 16.3, 17.9
University of Michigan	3.3, 9.4, 26.9, 30.7
University of Minnesota	22.4
University of Notre Dame	33.1
University of Science and Technology	26.6
University of Southern California	10.2, 16.7
University of Texas	9.3, 9.5, 11.1, 11.4, 16.5, 18.1
University of Tokyo	7.3
University of Toronto	26.2
University of Twente	30.4
University of Utah	10.7
University of Virginia	30.1, 30.7
University of Wuppertal	29.1

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VERMON	23.6
Vrije Universiteit Brussel	17.7
Washington State University	10.8
Western Digital	13.5
Wisol	20.3
WPI	26.8
Xi'an Aerosemi Technology	26.3
Xi'an Jiaotong University	4.6, 26.3
Xilinx	6.1, 8.2
XINYI Information Technology	20.2
Yonsei University	9.2, 23.8, 26.6, 28.3
Yuan Ze University	6.8

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