2017

PRESS KIT

ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of October 9, 2016, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.

ISSCC 2017
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

Table of Contents

Preamble

FAQ on ISSCC

What is ISSCC?

ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US$335.2 billion in sales in 2015 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Who Attends ISSCC?

Attendance at ISSCC 2017 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%**.

Where is ISSCC?

The **64th ISSCC** will be held at the San Francisco Marriott Marquis on February 5th through February 9th 2017.

Are there Keynote Speakers?

After a day devoted to educational events, ISSCC 2017 begins formally on Monday, February 6, 2017 with four exciting plenary talks:

- Cliff Hou, Vice President, Research & Development, TSMC, Hsinchu, Taiwan
- Ahmad Bahai, Chief Technology Officer, Texas Instruments, Santa Clara, CA
- Jonathan Rothberg, Founder, 4Catalyzer and Adjunct Professor of Genetics, Yale School of Medicine, New Haven, CT
- Lieven Vandersypen, Antoni van Leeuwenhoek Professor, QuTech and Kavli Institute of NanoScience, TU Delft, The Netherlands

What is the Technical Coverage at ISSCC?

ISSCC covers a full spectrum of design approaches in advanced technical areas broadly categorized as: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovations including micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking developments that may take three or more years for commercialization.

How are ISSCC Papers Selected?

Currently around 600 submissions are received each year across the broad spectrum of specified topics. Review is by a team of over 150 scientific and industry experts from the Far-East, Europe, and North America. These experts are organized into 10 Sub-Committees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline Subcommittees
- **Analog Systems** includes Analog and Data Converter Subcommittees
- **Digital Systems** includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees

What Companies are Presenting this year?

Companies presenting papers at ISSCC 2017 include AMD, Broadcom, IBM, Intel, Marvell, MediaTek, Panasonic, Samsung, and Toshiba, just to name a few. A more complete list can be found in the Index.

Are there educational sessions?

ISSCC features a variety of educational events which include:

- Ten Tutorials (targeted toward participants looking to broaden their horizon)
- Six Forums (targeted toward experts in an information sharing context)
- One Short Course (targeted toward in-depth appreciation of a current hot topic)

Are There Other Events?

A more complete list of all activities at ISSCC 2017:

- Four Plenary Presentations
- One Invited Talk on System Issues
- Technical Sessions (29 distinct sessions)
- Six Evening Sessions and Panels
- Educational Sessions Featuring:
    - Ten Tutorials
    - Six Forums
    - One Short Course
- Student Research Preview (for the introduction of graduate-student research-in-progress)
- Demonstration Sessions from Academia and Industry
- Networking Social Events
- Author Interview Sessions
- Women's Networking Luncheon
- A Number of University Alumni Events
- Book Display

How Do I Use this Press Kit?

The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes SESSION OVERVIEWS AND HIGHLIGHTS of all 29 technical sessions into which the 206 papers are grouped, together with brief descriptions and context for each. As well, there is an abstract for each of the Plenary talks. For your convenience, the Kit includes two structural charts in the INDEX section: (a) a list of the 4 Technical Topics and their associated Subcommittees (10) and Sessions (29); (b) a list of contributing companies and institutions with their associated papers. Thus, to located information of interest you can access Chart 4.1 to identify sessions of interest, after which you might logically access its Session's Overview or Highlight section. Alternatively, if your interest is in particular organization then Chart 4.1 will direct you immediately to papers of interest each of which is detailed in its corresponding Session Overview and possibly in the Highlights section. For anyone's interest it is useful to use Chart 4.1 to access the appropriate Trend information which provides a broad historical view of the context of your interest and often includes reference to current ISSCC 2017 papers.

Anything New This Year?

Again, this year, embedded in a regular session, an invited paper focuses on system-driven technology: It is that the increasing need for more more-power-efficient data centers, requires rethinking of intricate multi-level co-design strategies for building services down to nanoscale devices [26.1].

At ISSCC 2017, transistor counts continue to rise at 14nm with an 8 billion transistor 24-core POWER9 processor [3.1] and a 17 billion transistor FPGA [3.3]; FinFet applications abound [3.1, 3.2, etc]; 10nm has descended to implement an ARM processor [3.4]; high-efficient neural networks (CNN/RNN) implementations proliferate [Session 14]

Overview: ISSCC 2017 – Intelligent Chips for a Smart World

Advancements in solid-state circuits and systems continue to propel the ongoing fusion between the physical and virtual worlds. With the resulting growth in sensor deployment, data traffic and data center workloads, future systems must employ "intelligent" chips at all levels of the system stack to improve the efficiency at which we acquire, network, store, and process information. Modern applications centered around the Internet of Everything (IoE) and real-time data analytics are driving circuit and system designers toward new ways of leveraging the immense device density and processing power of modern technology.

Plenary Session (Session 1)

The Plenary Session on the morning of Monday, February 6, 2017, will feature four renowned speakers:

- Cliff Hou, Vice President, Research & Development, TSMC, Hsinchu, Taiwan will give his insights into "A Smart Design Paradigm for Smart Chips"
- Ahmad Bahai, Chief Technology Officer, Texas Instruments, Santa Clara, CA, will discuss the "Dynamics of Exponentials in Circuits and Systems".
- Jonathan Rothberg, Founder, 4Catalyzer and Adjunct Professor of Genetics, Yale School of Medicine, New Haven, CT, will present on "The Development of High-Speed DNA Sequencing: Jurassic Park, Neanderthal, Moore, and You".
- Lieven Vandersypen, Antoni van Leeuwenhoek Professor, QuTech and Kavli Institute of NanoScience, TU Delft, The Netherlands, will explore "Quantum Computing – The Next Challenge in Circuit and System Design".

Highlights of these Plenary talks are provided in the following section.

ISSCC 2017

PLENARY SESSION – INVITED PAPERS

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** Massachusetts Institute of Technology, Cambridge, MA

ISSCC Conference Chair

Associate Chair: ***Boris Murmann***, Stanford University, Stanford, CA

ISSCC International Technical-Program Chair

1.1 A Smart Design Paradigm for Smart Chips

Cliff Hou*, Vice President, Research & Development, TSMC, Hsinchu, Taiwan*

The world requires more specialized smart chips for connecting people intelligently at all times. Requirements for such chips in computing capability, power consumption, and form factor are becoming ever more demanding, while the market window is significantly shrinking. This talk explores the trends in chip innovation from costly multi-chip and SoC solutions to separated chips combined with wafer-stacking or 3-D packaging. These trends are further driving system-level integration for improved chip and systems performance, cycle time, and costs.

To capitalize on such mega-trends, innovations extending Moore's Law and efforts on specialty technologies for advancing connectivity are discussed. The ultimate goal is to optimize system performance through system-level integration of functionalities in advanced 3-D packaging. These will introduce new design challenges, where possible solutions are further gated by learning curves and cycle times.

Smart-chip designers are increasingly looking for opportunities where others can supply expertise and assets, whether as single-chip designs or system-level integrations. We highlight the emergence of a new collaborative paradigm, which is moving from technology-centric options to total platform-centric solutions sufficiently broad to address the unique challenges of the next big things, particularly in mobile, IoT, automotive, high-performance computing.

1.2 Dynamics of Exponentials in Circuits and Systems

***Ahmad Bahai**, Chief Technology Officer, Texas Instruments, Santa Clara, CA*

Astonishing progress in semiconductor devices, circuits, and manufacturing has prompted an unprecedented revolution in electronics. "Things" are getting smarter and more connected, with higher semiconductor content. Smart personal electronics, autonomous systems, and smart factories are prime examples.

These impressive developments are fueled by the power of exponentials: CMOS scaling, efficiency of semiconductor manufacturing, the bandwidth efficiency of communication systems, and total network capacity have all been doubling almost every two years! The sheer scaling of CMOS has dominated the challenges and promises of advanced IC design. Advanced digital-intensive designs count on denser, faster, and cheaper switches. Along the way, analog and RF designs have creatively embraced the challenge of implementing analog topologies on digitally-optimized processes.

The present slowdown of the CMOS scaling trend brings exciting opportunities for "multi-dimensional innovations" in circuits and systems: The continuing demand for higher performance, in many applications, will further tilt solutions toward creative system and circuit topologies. Many emerging complementary technologies such as MEMS-based sensors and timing references, III-V devices, high-performance SiGe devices, and silicon photonics, will not necessarily integrate with CMOS monolithically. However, they enable opportunities for system repartitioning and new circuit topologies in applications such as sensing, power, high voltage, high-performance RF, and precision timing.

CMOS is here to stay for the foreseeable future! It will simply coexist synergistically with emerging technologies. This talk will discuss opportunities in "multi-dimensional innovation" that will make the future of the field less predictable.....but even more interesting and exciting!

1.3 The Development of High-Speed DNA Sequencing: Jurassic Park, Neanderthal, Moore, and You

***Jonathan Rothberg**, Founder, 4Catalyzer and Adjunct Professor of Genetics, Yale School of Medicine, New Haven, CT*

Since Watson and Crick's 1953 landmark discovery that biological information was encoded in DNA as a sequence of chemical building-block "letters", developing technology for reading (or sequencing) this chemical code has been fundamental to advances in biology and medicine.

Techniques that first enabled this were invented by Sanger in 1978, and were taken to massively parallel form by '454 Life Sciences' in 2003. This ushered in the current or "next-gen" era of genome sequencing technologies for research, medicine, and the emerging field of Genomic Personalized Medicine, in which healthcare is more fully informed by the individual's personal genetic makeup. If Sanger was the mainframe of sequencing, '454' was the minicomputer – smaller and faster and establishing the key guiding technical principals.

To further scale, reduce cost, and democratize the technology, I turned back to the developments of Noyce and Moore, and developed the first semiconductor-based sequencing technology to make it truly personal. We demonstrated this by sequencing the genome of Gordon Moore of Moore's Law fame.

This talk will discuss the evolution of semiconductor devices capable of performing DNA sequencing, and how the use of a scalable CMOS chip architecture allows for radical levels of economic scaling, and convenient new formats (from desktop to portable).

1.4 Quantum Computing – The Next Challenge in Circuit and System Design

***Lieven Vandersypen**, Antoni van Leeuwenhoek Professor, QuTech and Kavli Institute of NanoScience, TU Delft, The Netherlands*

Quantum computers have the potential to tackle problems in materials science, chemistry, and mathematics that are well beyond the reach of supercomputers. Their power derives from the use of quantum bits, which can exist in arbitrary combinations of 0 and 1. This leads to a computing power that doubles with every additional quantum bit.

The challenge of quantum computing is that quantum bits are extremely fragile and their state is easily perturbed by environmental fluctuations. However, recent theoretical and experimental advances have made it clear that the resulting errors can in-principle be corrected. What it takes is a system containing thousands or millions of quantum bits operating at ultra-low temperatures, that must be interfaced using complex classical mixed-signal and microwave circuits for read-out and control. By comparison, today's practical demonstrations involve no more than a dozen quantum bits controlled by bulky instrumentation that is not scalable.

This talk will introduce the basic concepts behind quantum computing, summarize the state-of-the-art of solid-state implementations, and present the major open challenges in the realization of large-scale quantum circuits, including the design of dedicated classical control circuits and systems.

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EVENING PANELS AND SESSIONS

Evening Panels and Sessions

ISSCC 2017 will continue the popular tradition of evening panels and evening sessions, where experts, often of opposing views, discuss topics which range from the lighthearted to the controversial (but always informative and entertaining!).

This year's panels are "Quantum Engineering: Hype, Spin, or Reality?", "When Will We Stop Driving our Cars?", and "Return of Survey Says!" – an interactive panel modelled after the US game show "Family Feud". This year's evening sessions are "Intelligent Machines: Will the Technological Singularity Happen?" and "Semiconductor Economics: How Business Decisions are Engineered".

ES2 Intelligent Machines: Will the Technological Singularity Happen?

Sunday, February 5

EP1 Quantum Engineering: Hype, Spin, or Reality?

Monday, February 6

ES3 Semiconductor Economics: How Business Decisions are Engineered

Monday, February 6

EP2 When Will We Stop Driving Our Cars?

Tuesday, February 7

EP3 Return of Survey Says!

Tuesday, February 7

ISSCC 2017

SESSION OVERVIEWS AND HIGHLIGHTS

Conditions of Publication

PREAMBLE

The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2017 in February in San Francisco

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- That you will maintain at least one reference to ISSCC 2017 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.
- That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 64th appearance of ISSCC, on February 5th to February the 9th, 2017, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2017, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 5 - February 9, 2017,

at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: Power Amplifiers

RF Subcommittee

Session Chair: *Kohei Onizuka, Toshiba, Kawasaki, Japan*

Session Co-Chair: *Abbas Komijani, Qualcomm, San Jose, CA USA*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF*

Improving efficiency at back-off power levels has become an active area of research to support spectrally efficient modulation schemes with high peak-to-average power ratios. Doherty power-amplifier topology and envelope-tracking supply modulation are key enablers to improve the back-off efficiency of transmitters. Increasing signal bandwidths for applications such as carrier-aggregation LTE and WiFi 802.11ac poses challenges for supply modulation. Implementing the Doherty topology for 5G applications operating at mm-wave frequencies is an active area of research.

- In Paper 2.1, Georgia Institute of Technology presents an offset-line-based transformer Doherty combiner to enhance the efficiency and bandwidth of a PA. A power-dependent uneven-feeding scheme is introduced to further improve back-off efficiency. The Doherty PA achieves a maximum 1.92× PA efficiency improvement at 6dB power back-off over a Class-B PA at 37GHz.
- In Paper 2.2, Broadcom describes a current-mode hysteresis comparator and a combination of core devices cascoded with high-voltage LDMOS transistors to enable a wide-bandwidth supply modulator. Efficiency improvements for a 20MHz signal at 2GHz and a 40MHz signal at 5GHz are 28% and 34%.
- In Paper 2.3, National Chiao Tung University and Realtek Semiconductor describe a single-inductor dual-output supply modulator with cross regulation. The modulator achieves 86% efficiency and delivers up to 2W of output power with a bandwidth of 20MHz.
- In Paper 2.4, Hong Kong University of Science and Technology presents an envelope-tracking system that achieves high efficiency for 20MHz LTE at supply voltages as low as 2.4V. The envelope tracking and the PA system achieve 24dBm of output power, 36% PAE and -32dBc ACLR for a 20MHz signal at 2.4GHz.
- In Paper 2.5, MediaTek presents two CMOS LTE PAs with Class-F matching network. The Class-F matching network allows for high efficiency and high linearity for these PAs with 2.2dB/3.9dB power back-off for a WCDMA/LTE signal. The PAs achieve 37%/34% PAE, 27dBm/28dBm output power with ACLR of -32dB at 0.83GHz/1.88GHz band for a 20MHz LTE 16-QAM signal.
- In Paper 2.6, Huawei and University of Pavia present a SiGe power amplifier at 80GHz. A common-base output stage causes the DC current to track the signal current and improve efficiency at back-off power. Realized prototype shows OP_{1dB} of 18dBm with P_{sat} of 19dBm. The efficiency at OP_{1dB} and at 6dB are 22% and 8.5%, respectively.
- In Paper 2.7, Texas A&M University, Silicon Laboratories, and Qualcomm describe a 28GHz CMOS PA that supports 8×100MHz 64-QAM OFDM carrier aggregation at 6.7dBm P_{out} with 11% PAE. The PA uses a dual-resonance transformer matching network to increase the bandwidth.
- In Paper 2.8, University of California, San Diego, combines voltage-mode Doherty and Class-G switched-capacitor techniques to improve the efficiency of a PA at both 6dB and 12dB back-off. The CMOS PA achieves 25dBm P_{sat} with 30%/24%/17% PAE at peak power and 6dB/12dB back-off at 3.6GHz.

Session 2 Highlights: Power Amplifiers

[2.1] A 28GHz/37GHz/39GHz Multiband Linear Doherty Power Amplifier for 5G Massive MIMO Applications

[2.2] A Fully Integrated Reconfigurable Wideband Envelope-Tracking SoC for High-Bandwidth WLAN Applications in a 28nm CMOS Technology

[2.8] A Class-G Voltage-Mode Doherty Power Amplifier

Paper 2.1 Authors: *S. Hu, H. Wang*

Paper 2.1 Affiliation: *Georgia Institute of Technology, Atlanta, GA*

Paper 2.2 Authors: *D. Chowdhury, S. Mundlapudi, A. Afsahi*

Paper 2.2 Affiliation: *Broadcom, San Diego, CA*

Paper 2.8 Authors: *V. Vorapipat, C. Levy, P. Asbeck*

Paper 2.8 Affiliation: *University of California, San Diego, CA*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF*

CONTEXT AND STATE OF THE ART

- Improving efficiency at the back-off power levels has become an active area of research to support spectrally efficient modulation schemes with high peak-to-average power ratios. Doherty power-amplifier topology and envelope-tracking supply modulation are key enablers to improve the back-off efficiency of transmitters. Increasing signal bandwidths for applications such as carrier-aggregation LTE and WiFi 802.11ac poses challenges for supply modulation.
- Implementing Doherty topology for 5G applications operating at mm-wave frequencies is an active area of research.

TECHNICAL HIGHLIGHTS

Triple-band Doherty power amplifier at mm-wave frequencies.

- An offset-line-based-transformer Doherty combiner is proposed to enhance PA efficiency and bandwidth. A power-dependent uneven-feeding scheme is used to further improve back-off efficiency. The 37GHz Doherty PA achieves a maximum 1.92× PA efficiency improvement at 6dB power back-off over a Class-B PA.

The first WLAN SoC with fully integrated envelope tracking.

- A current-mode hysteresis comparator and a combination of core devices cascoded with high-voltage LDMOS transistors enables a wide-bandwidth supply modulator. Efficiency improvements for a 20MHz signal at 2GHz and a 40MHz signal at 5GHz are 28% and 34%.

A Class-G Doherty power amplifier with efficiency improvement at deep back-off.

- Voltage-mode Doherty and Class-G switched-capacitor techniques are combined to improve the efficiency of a PA at both 6dB and 12dB back-off. The CMOS PA achieves 25dBm P_{sat} with 30%/24%/17% PAE at peak/6dB/12dB back-off at 3.6GHz.

APPLICATIONS AND ECONOMIC IMPACT

- With the imminent deployment of 5G systems, improving the efficiency of the transmitter will be a critical enabler to achieve simultaneous high data-rates and long battery life. The techniques presented in this session are steps towards improving transmitter efficiencies.

Session 3 Overview: Digital Processors

Digital Architectures and Systems Subcommittee

Session Chair: *Thomas Burd, AMD, Sunnyvale, CA*

Session Co-Chair: *James Myers, ARM, Cambridge, UK*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Korea, DAS*

Digital processors continue to diversify in scope, utilizing a variety of process technologies, application-specific architectures, power management techniques, and heterogeneous processors integrated on a single die. The first two papers cover next-generation high-performance POWER and x86 CPUs, followed by ISSCC's first high-density FPGA. Next come two highly integrated power-optimized mobile SoCs including the first at 10nm, an automotive microcontroller and a MIMO baseband chip. The final paper is a vision processor for autonomous drones.

- In Paper 3.1, IBM describes the 8 billion transistor 24 core POWER9™ processor implemented in a 14nm SOI FinFET technology, featuring 48 lanes of PCIe Gen4, and 48 lanes of 25Gb/s links.
- In Paper 3.2, AMD presents the next-generation high-performance x86 core, implemented in a 14nm FinFET technology achieving 40% higher instructions-per-clock-cycle than the previous-generation processor.
- In Paper 3.3, Intel presents a 17 billion transistor 1GHz FPGA in a 14nm technology, with up to six 20nm transceiver chips integrated within a 2.5D embedded bridge packaging.
- In Paper 3.4, Mediatek describes a 10nm SoC featuring three different ARMv8A microarchitectures in a tri-cluster, decacore configuration.
- In Paper 3.5 Renesas describes a 40nm microcontroller with intelligent motor timer hardware control that realizes 0.8μs field-oriented control execution and functional safety mechanism for EV/HEV motor control.
- In Paper 3.6, Lund University presents a 128×8 massive MIMO baseband implementation achieving 60pJ/b at 300Mb/s detection rate, implemented in 28nm FDSOI.
- In Paper 3.7, University of Michigan presents a 30fps HD stereovision processor with 512 levels of depth perception, featuring a deep pipeline and high bandwidth custom SRAMs to achieve a 5.8× energy-efficiency improvement.

Session 3 Highlights: Digital Processors

[3.4] A 10nm FinFET 2.8GHz, Tri-Gear Deca-core CPU Complex with Optimized Power-Delivery Network for Mobile SoC Performance

[3.1] POWER9™: A Processor Family Optimized for Cognitive Computing with 25Gb/s Accelerator Links and 16Gb/s PCIe Gen4

[3.2] Zen: A Next-Generation High-Performance x86 Core

Paper 3.4 Authors: Hugh Mair[1], Ericbill Wang[2], Alice Wang[2], Ping Kao[2], Yuwen Tsai[2], Sumanth Gururajarao[1], Rolf Lagerquist[1], Jin Son[1], Gordon Gammie[1], Gordon Lin[2], Achuta Thippana[1], Kent Li[1], Manzur Rahman[1], Wuan Kuo[2], David Yen[2], Yi-Chang Zhuang[2], Ue Fu[2], Hung-Wei Wang[2], Mark Peng[3], Cheng-Yuh Wu[2], Taner Dosluoglu[4], Anatoly Gelman[4], Daniel Dia[2], Girishankar Gurumurthy[2], Tony Hsieh[2], WX Lin[2], Ray Tzeng[2], Jengding Wu[2], CH Wang[2], Uming Ko[2]

Paper 3.4 Affiliation: [1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan; [3]MediaTek, San Jose, CA; [4]Endura Technologies, San Diego, CA

Paper 3.1 Authors: Christopher Gonzalez[1], Eric Fluhr[2], Daniel Dreps[2], David Hogenmiller[2], Rahul Rao[3], Jose Paredes[2], Michael Floyd[2], Michael Sperling[4], Ryan Kruse[2], Vinod Ramadurai[2], Ryan Nett[2], Saiful Islam[2], Juergen Pille[5], Donald Plass[4]

Paper 3.1 Affiliation: [1]IBM, Yorktown Heights, NY; [2]IBM, Austin, TX; [3]IBM, Bangalore, India; [4]IBM, Poughkeepsie, NY; [5]IBM, Boblingen, Germany

Paper 3.2 Authors: Teja Singh[1], Sundarajan Rangarajan[2], Deepesh John[2], Carson Henrion[3], Shane Southard[2], Hugh McIntyre[4], Amy Novak[2], Stephen Kosonocky[3], Ravi Jotwani[2], Alex Schaefer[2], Edward Chang[3], Joshua Bell[2], Michael Co[2]
Paper 3.2 Affiliation: [1]AMD, Austin, TX; [2]AMD, Austin, TXI [3]AMD, Fort Collins, CO; [4]AMD, Sunnyvale, CA

Subcommittee Chair: Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, DAS

CONTEXT AND STATE OF THE ART

- The tri-gear deca-core CPU from Mediatek represents the industry's first 10nm microprocessor.
- IBM's POWER9™ chip addresses the ever growing need for more bandwidth and compute power to solve the world's most complicated computing problems
- AMD's new Zen core demonstrates significant performance and power efficiency gains in the x86 processor landscape

TECHNICAL HIGHLIGHTS

- MediaTek introduces the industry's first 10nm deca-core SoC featuring three distinct power-optimized implementations of the ARMv8a architecture
- IBM POWER9™ features 24 4-threaded cores with 120MB L3, 48 lanes of PCIe Gen4, and 48 lanes of 25 Gb/s next generation NVLink™
- AMD presents its next generation "Zen" CPU core: A quad-core complex with 8MB L3 providing 40% more IPC performance targeted for server, desktop, and mobile PC applications

APPLICATIONS AND ECONOMIC IMPACT

- The industry's first-ever 10nm microprocessor demonstrates continued technology density improvement in the everlasting pursuit of Moore's law. The density improvements arising from 10nm will help drive lower power devices with higher levels of integration across the industry.
- The three highlighted microprocessors span the spectrum of computing applications from server class microprocessors to cutting edge mobile devices, each highlighting a specific need in the marketplace. IBM's POWER9™ chip will expand data-center compute performance and will enable new classes of cognitive workloads with industry-leading accelerator interfaces. AMD's next Zen core is designed to scale between server, desktop, and mobile chips. Finally, Mediatek's deca-core mobile SoC enables increased energy efficiency and features a Cortex-A73 CPU complex.

Session 4 Overview: Imagers

IMMD Subcommittee

Session Chair: *Hayato Wakabayashi, Sony Electronics, San Jose, CA*

Session Co-Chair: *Jun Deguchi, Toshiba Corporation, Kawasaki, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

The session presents advances in image sensors covering the emerging topics of 3D stacking, organic photoconductive film, fluorescent imaging, global shutters and dynamic vision sensors. The first paper, by Samsung, presents a vision sensor that processes events group by group using a fully synthesized word-serial group address-event representation. Then, InSilixa presents an integrated biochip with a 32×32 fluorescence-based pixel array with integrated excitation filter and on-chip heater for real-time amplicon-probe hybridization detection. The next paper facilitates fluorescent lifetime imaging with multiple exponential decays using a 4-tap lock-in pixel and shared pulse generator. The University of Michigan presents a low-power single cell light-to-digital converter for monitoring accumulated light exposure for wearable applications. Canon presents a low-noise, wide-dynamic range, small-pixel-pitch global-shutter imager with dual-gain amplifiers. Sony presents a 3-layer stacked CMOS image sensor with a 1Gb DRAM used as a frame buffer for accumulating multiple frames to improve image quality, while reducing output data rate. Panasonic demonstrates high conversion gain in large pixels by replacing the traditional reset gate with a bootstrapping reset technique. Finally, a high-speed 3D stacked vision chip is presented, which includes line buffers and frame buffers for spatio-temporal image processing.

- In Paper 4.1, Samsung presents a BSI Dynamic Vision Sensor with 9μm pixel pitch supporting a data rate of 300Meps. The sensor employs a gain-boosted log amplifier and processes events group by group using a fully synthesized word serial group address event representation.
- In Paper 4.2, InSilixa presents a fully integrated biochip system having 32×32 fluorescence–based biosensor pixel array with on-chip thermal cycling capability and 116dB detection dynamic range.
- In Paper 4.3, Shizuoka University presents a programmable sub-nanosecond time-gated 4-tap lock-in pixel fluorescence lifetime imager using an in-pixel pulse-generator. This sensor achieves an intrinsic response of 170ps at 172nm and 0.85e^-_{rms} with true correlated double sampling (CDS) operation.
- In Paper 4.4, University of Michigan presents a light-to-digital converter, which measures light intensity over the range from 80mlx to 1.26Mlx, using two dynamic leakage suppression inverter-based ring oscillators.
- In Paper 4.5, Canon describes a low-noise and high dynamic range (HDR) 3.4μm pixel pitch global shutter CMOS image sensor with dual-gain amplifiers SS-ADC. This sensor employs a multiple accumulation shutter technique to increase the signal saturation level.
- In Paper 4.6, Sony Semiconductor Solutions presents a 3-layer stacked CMOS image sensor with DRAM as a frame buffer. The sensor reads out 19Mpixels to DRAM at a speed of 120fps and outputs at 30fps from the sensor.
- In Paper 4.7, Panasonic presents a 2.1Mpixel RGB-IR image sensor. The sensor realizes electrically controllable IR sensitivity with stacked organic photoconductive films.
- In Paper 4.8, Shizuoka University describes a 0.5Mpixel CMOS image sensor with a high conversion gain pixel using a bootstrapping reset technique to achieve 0.44e^-_{rms} read-noise at 32fps.
- In Paper 4.9, Sony Semiconductor Solutions presents a high-speed vision chip with 3D-stacked column-parallel ADCs and 140GOPS programmable SIMD column-parallel processing elements for spatio-temporal image processing.

Session 4 Highlights: Imagers

[4.6] A 1/2.3in 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM

Paper Authors: *Tsutomu Haruta[1], Tsutomu Nakajima[1], Jun Hashizume[1], Taku Umebayashi[1], Hiroshi Takahashi[1], Kazuo Taniguchi[1], Masami Kuroda[1], Hiroshi Sumihiro[1], Koji Enoki[1], Takatsugu Yamasaki[2], Katsuya Ikezawa[1], Atsushi Kitahara[1], Masao Zen[1], Masafumi Oyama[1], Hiroki Koga[1], Hidenobu Tsugawa[1], Tomoharu Ogita[1], Takashi Nagano[1], Satoshi Takano[3], Tetsuo Nomoto[1]*

Paper Affiliation: *[1]Sony Semiconductor Solutions, Atsugi, Japan, [2]Sony Semiconductor Manufacturing, Atsugi, Japan, [3]Sony LSI Design, Atsugi, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD subcommittee*

[4.7] A 2.1Mpixel Organic-Film Stacked RGB-IR Image Sensor with Electrically Controllable IR Sensitivity

Paper Authors: *Shin'ichi Machida, Sanshiro Shishido, Takeyoshi Tokuhara, Masaaki Yanagida, Takayoshi Yamada, Masumi Izuchi, Yoshiaki Sato, Yasuo Miyake, Manabu Nakata, Masashi Murakami, Mitsuru Harada, Yasunori Inoue*

Paper Affiliation: *Panasonic, Moriguchi City, Osaka, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- The trend towards 3D wafer-level stacking for integration of the sensor substrate with deep-submicron CMOS technology nodes is reaching new frontiers by adding more stacked layers to enable image sensors featuring high pixel count, combined with high frame rate and embedded processing capabilities.
- The stacking of organic film on CMOS permits extension of the imager spectral response to near-infrared with very high quantum efficiency performance, high pixel count, and no aliasing due to pixel segmentation.

TECHNICAL HIGHLIGHTS

Sony reports a three-layer stacked CMOS image sensor with DRAM for frame buffering, enabling high-frame-rate operation for slow-motion movie recording and minimization of rolling shutter distortion.

- In Paper 4.6, Sony presents 1/2.3-inch 20Mpixel three-layer stacked CMOS image sensor embedding a 1Gb DRAM capable of reading 19Mpixels at 120 frames per second.

Panasonic introduces an organic photoconductive film image sensor with electrically controllable infrared sensitivity.

- In Paper 4.7, Panasonic presents a 1920x1080-pixel RGB-IR CMOS image sensor based on directly stacked organic photoconductive films featuring 3-micron pixel pitch and electrically controlled IR sensitivity with less than -15dB extinction ratio.

APPLICATIONS AND ECONOMIC IMPACT

- High-resolution, high-speed, compact image sensors for cameras will enable slow-motion movie recording on portable devices and pave the way to on-chip processing-intensive features.
- Organic photoconductive film CMOS image sensors advance the state of the art by improving the NIR sensitivity and reducing the pixel size for applications in automotive, machine vision and security and surveillance.

Session 5 Overview: Analog Techniques

Analog Subcommittee

Session Chair: *Tim Piessens, ICsense, Belgium*

Session Co-Chair: *Vadim Ivanov, Texas Instruments, Tucson, AZ*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX, Analog*

Analog techniques continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. Entries span the range of linear regulators, Class-D audio, references and oscillators. New frontiers of precision, power, and performance are established.

- In Paper 5.1, NXP Semiconductors describes a 5x80W 0.004% THD+N multiphase Class-D audio amplifier aimed at automotive applications. Integrated low-latency ADCs with 116dB dynamic range enable digital loop-filters to compensate the output filter and enable high loop-gain and low-cost filter components in 0.14µm BCD SOI.
- In Paper 5.2, the KAIST School of Electrical Engineering presents a 0.18µm BCD 7-level Class-D Audio amplifier with a 91% power efficiency in an 80hm load. By employing a folded-PWM scheme, high linearity of 0.02% THD+N is preserved at multilevel boundaries. It transmits 10W output power at THD+N=1%.
- In Paper 5.3, Holst Centre / imec introduces a 90nm LP CMOS 95µW 24MHz crystal oscillator for IoT. By dynamically adjusting the load, the negative resistance is boosted, achieving a > 13x start-up time reduction. The presented technique imposes a negligible energy overhead of 3.3nJ and 0.0073 mm^2 area for achieving 6.9x start-up energy reduction.
- In Paper 5.4, Texas Instruments describes a 0.13um CMOS ring oscillator with less than 3ns peak-to-peak accumulated jitter over a 1ms time window. By locking the ring oscillator to an RC time constant, a high time resolution of 770ps is obtained.
- In Paper 5.5, a 0.18um CMOS quadrature relaxation oscillator with a frequency-error compensation loop is presented by Pohang University of Science and Technology. The oscillator achieves a FOM of 155dBc/Hz at 444.9kHz. Using a switching scheme to compensate process variation and 1/f noise, it alleviates speed requirements and reduces power consumption.
- In Paper 5.6, the University of Southampton presents a 0.68nW/kHz relaxation oscillator in 65nm CMOS. It is demonstrated to have a +/-0.49%/V and 96ppm/ºC stability in a 0.005mm^2 area.
- In Paper 5.7, a 0.18µm CMOS capacitive-gain amplifier with common-mode sampling is presented by Analog Devices. The amplifier achieves 19nV/Hz noise with 75uA supply current. It defines the common-mode voltage in a single autozero phase. A precharge technique and dynamic filtering are used to drive a switched-capacitor ADC directly. It achieves 5ppm/FS INL, 2µV offset and 0.8ppm/ºC max gain error drift.
- In Paper 5.8, a 9.3nW bandgap and current reference is presented by the Pohang University of Science and Technology. The bandgap reference is implemented in a 0.18µm CMOS process and achieves a standard deviation of 0.43% with a temperature coefficient of 26ppm/ºC.
- In Paper 5.9, TSMC is describing a 18.75µW temperature sensor. By using dynamic distributing bias, an untrimmed 0.87ºC, 3-sigma accuracy is achieved, occupying 0.00946mm^2 area in a 28nm CMOS process.
- In Paper 5.10, Marvell is presenting a 1A LDO regulator. By using a Class-D control scheme to drive the pass transistor, the quiescent current could be as low as 152µA. The controller occupies 0.0013mm^2 in a 28nm CMOS process.
- In Paper 5.11, an inverter-based LDO in 65nm LP CMOS is presented by the Hong Kong University of Science and Technology. The LDO is capable of regulating while running on a supply down to 0.2V. The proposed regulator achieves a higher than 20dB PSR from 1MHz to over 10MHz while consuming 410nA when running from a 0.2V supply voltage, and 32uA when running from a 0.6V supply

Session 5 Highlights: Analog Techniques

[5.3] A 95µW 24MHz Digitally Controlled Crystal Oscillator for IoT Applications with 36nJ Start-Up Energy and >13x Start-Up Time Reduction Using A Fully-Autonomous Dynamically Adjusted Load

Paper 5.3 Authors: *M. Ding, Y. Liu, Y. Zhang, C. Lu, P. Zhang, B. Busze, C. Bachmann, K. Philips*

Paper 5.3 Affiliation: *IMEC Hoist Centre, Eindhoven, Netherlands*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Crystal oscillators provide the highest frequency accuracy, required by radios, but need lengthy startup. Large current consumption during this startup is heavily taxing the IoT power budget.

TECHNICAL HIGHLIGHTS

13x reduction in start-up time of a crystal oscillator achieved by gradually increasing the load capacitance

- In Paper 5.3, crystal oscillator load is adjusted and negative resistance of the driver is boosted, achieving 13x startup time improvement

APPLICATIONS AND ECONOMIC IMPACT

- Faster power-cycling in IoT radios will greatly improve their energy efficiency, decrease required battery volume or energy harvesting needs.

Session 5 Highlights: Analog Techniques

[5.7] A 19nV/√Hz noise 2μV offset 75μA Low-Drift Capacitive-Gain Amplifier with Switched-Capacitor ADC Driving Capability

Paper 5.7 Authors: *H. Wang, G. Mora-Puchalt, C. Lyden, R. Maurino, C. Birk*

Paper 5.7 Affiliation: *Analog Devices, Inc.*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Accuracy of systems powered by low supply voltage is impaired when processing input signals outside of the supply range.

TECHNICAL HIGHLIGHTS

Low noise, low offset and fast common-mode settling achieved for a capacitive gain amplifier

- An accurate amplifier is designed for conditioning sensor signals with common mode outside the supply rail for ADCs.
- In Paper 5.7,the capacitive-gain amplifier combines chopping, dynamic filtering and capacitor precharging to accurately process signals outside of the supply range

APPLICATIONS AND ECONOMIC IMPACT

- Use of low-voltage signal processing of wide-range input signals will decrease consumed power and system size.

Session 6 Overview: Ultra High Speed Wireline

Wireline Subcommittee

Session Chair: *Simone Erba, STMicroelectronics, Pavia, Italy*

Session Co-Chair: *Takayuki Shibasaki, Fujitsu Laboratories, Kawasaki, Japan*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro OR, Wireline*

The continuous growth of the internet and of big data infrastructure drives the ever-increasing demand for data communication bandwidth between chips. In this context, wireline transceiver data rate, energy efficiency, and area are extremely critical. This session introduces two transceivers operating at 56Gb/s PAM-4 and 60Gb/s NRZ. It continues with a presentation of a 40-56Gb/s PAM-4 receiver with 10-tap direct decision feedback equalization in 16nm FinFET. Two papers presenting high-data-rate, low-power PAM-4 transmitter designs are presented next, including a 64Gb/s design with a 4-tap FFE in 28nm FDSOI CMOS, and a 56Gb/s design with fractionally spaced FFE in 14nm CMOS. Finally, the session concludes with two papers describing receivers at or beyond 28Gb/s, including a reference-less baud-rate CDR with DFE and CTLE in 28nm CMOS and a digital CDR with adaptive loop gain for optimum jitter tolerance.

- In Paper 6.1, National Taiwan University presents a TRX chipset at 56Gb/s with integrated serializer/deserializer, FFE/CTLE/DFE, CDR, and eye-monitoring circuits. It demonstrates BER<10^{-12} over 24dB loss at 14GHz and dissipates 602mW of power.
- In Paper 6.2, The University of California Berkeley presents a 60Gb/s NRZ. A new baud-rate CDR is proposed to enable energy efficient CDR operation. Implemented in a 65nm CMOS technology, the design achieves a 60Gb/s data-rate with 30% eye opening at BER < 10^{-12} while consuming only 288mW.
- In Paper 6.3, Xilinx presents a 40-56Gb/s PAM-4 receiver with a 10-tap DFE targeting chip-to-module interconnects designed in 16nm FinFET. The design implements direct feedback of the first post-cursor DFE tap to reduce the number of slicers. The receiver achieves PRBS31 BER < 10^{-12} over a channel with 10dB loss at 14GHz while dissipating 230mW.
- In Paper 6.4, STMicroelectronics presents a PAM-4 transmitter with 4-tap FFE in 28nm FDSOI CMOS. The proposed TX leverages a new serializer architecture and output stage to demonstrate 1.2Vppd output swing and the highest reported speed of 64Gb/s. Further, it shows state-of-the-art 2.26pJ/bit energy efficiency while meeting CEI-56G-PAM-4 requirements.
- In Paper 6.5, IBM T. J. Watson Research Center presents a 56Gb/s PAM-4 transmitter for VSR applications. Fabricated in 14nm FinFET technology, the design includes a data-rate-agile half-baud-spaced 3-tap FFE implemented using static CMOS logic with quadrature half-rate clocks. The TX achieves a power efficiency of 1.8pJ/bit from 0.8/0.95V supplies while equalizing a channel with 6dB of loss at 14GHz.
- In Paper 6.6, The University of Toronto presents a reference-less baud-rate CDR. Combined with a CTLE and 1-tap DFE, the design operates from 22.5Gb/s to 32Gb/s over up to 14.8dB channel loss at Nyquist. A proposed frequency detection scheme automatically controls an adjustable baud-rate PD to correct frequency error and improves CDR capture range by >200x. The entire receiver is fabricated in 28nm CMOS and achieves 3.2pJ/bit at 32Gb/s PRBS31.
- In Paper 6.7, The University of Toronto presents a loop gain adaptation strategy, which optimizes the jitter tolerance of a 28Gbps PI-based CDR implemented in 28nm CMOS. The technique increases the CDR's loop gain to suppress jitter while monitoring the autocorrelation function of the bang-bang PD output to avoid underdamped behavior. The proposed technique requires no knowledge of the CDR's latency or the input jitter characteristics and can also be extended to operate in the presence of periodic jitter.

Session 6 Highlights: Ultra High Speed Wireline

[6.2] A 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology

[6.3] A 40-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision Feedback Equalization in 16nm FinFET

Paper 6.2 Authors: *Jaeduk Han[1], Yue Lu[2], Nicholas Sutarddja[1], Elad Alon[1]*
Paper 6.2 Affiliation: *[1]University of California at Berkeley, Berkeley, CA, [2]Qualcomm Atheros, San Jose, CA*

Paper 6.3 Authors: *Jay Im[1], Dave Freitas[1], Arianne Roldan[2], Stanley Chen[1], Scott McLeod[1], Adam Chou[1], Lei Zhou[1], Ian Zhuang[1], Tim Cronin[1], Jaeduk Han[3], Sen Lin[3], Parag Upadhyaya[1], Ronan Casey[4], Kevin Geary[4], Geoff Zhang[1], Yohan Frans[1], Ken Chang[1]*
Paper 6.3 Affiliation: *[1]Xilinx, San Jose, CA, [2]Xilinx, Singapore, [3]University of California at Berkeley, CA, [4]Xilinx, Cork, Ireland*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline*

CONTEXT AND STATE OF THE ART

- The data-rate of electrical interfaces over chip-to-module interconnect is projected to reach 56Gb/s and beyond in order to meet increasing bandwidth demand in data-centers and telecommunication infrastructures. For cost considerations, it is desirable to keep the existing PCB materials and connectors. Such interconnect may exhibit up to 10dB channel insertion loss at 14GHz with a potential insertion loss cliff beyond 14GHz, motivating the use of PAM-4 signaling to keep signal frequency content below 14GHz.
- When better interconnect, like twinax cable, is considered and the insertion loss profile is more linear, NRZ signaling still provides the proper equalization capability to deal with >20dB channel insertion loss at the Nyquist frequency with state-of-the-art energy efficiency.

TECHNICAL HIGHLIGHTS

Highest data-rate and lowest power consumption 65nm electrical transceiver.

- In Paper 6.2, University of California Berkeley presents a 60Gb/s NRZ transceiver for high-speed wireline communications. A new baud-rate CDR is proposed to enable an energy efficient 60Gb/s CDR operation. The design is implemented in a 65nm CMOS technology and achieves a 60Gb/s data-rate with 30% eye-opening at BER < 10^{-12} BER, consuming 288mW.

First 10-tap analog direct DFE 56Gb/s PAM-4 for a low-power-consumption receiver.

- In Paper 6.3, Xilinx presents a 40-56Gb/s PAM-4 receiver with 10-tap DFE targeting chip-to-module interconnects designed in 16nm FinFET. The design implements direct feedback of the first post-cursor DFE tap to reduce the number of slicers. The receiver achieves PRBS31 BER < 10^{-12} over a channel with 10dB loss at 14GHz and consuming 230mW.

APPLICATIONS AND ECONOMIC IMPACT

- Continued performance gains for datacenter and supercomputers requires power- and cost-efficient bandwidth density scaling between components. These papers are early demonstrations of bandwidth density scaling reaching 56Gb/s and beyond.
- High-data rate NRZ transceivers are the best choice for energy efficient links over twinax cables where more complex modulation techniques are not required.
- Effective DFE analog implementation is enabling the next generation PAM-4 standard in modules and port ASICs applications, requiring low power per link consumption.

Session 7 Overview: Wireless Transceivers

Wireless Subcommittee

Session Chair: *Yuu Watanabe, Waseda University, Kitakyushu, Japan*

Session Co-Chair: *Danielle Griffith, Texas Instruments, Dallas, TX*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Espoo, Finland, Wireless*

Higher-performance and lower-power wireless systems are required for next generation transceivers. This session includes advanced wireless technology showing an 802.11ac Stage2 dual-band reconfigurable transceiver supporting up to four 80 MHz spatial streams, a 28GHz phased-array IC including 32 TRX elements, a transceiver for LTE-A carrier aggregation, a 915MHz asymmetric radio using a Q-enhanced amplifier, A TCXO-less 100Hz minimum bandwidth transceiver, A +8dBm BLE/BT transceiver with automatically calibrated integrated RF bandpass filter and dual-band 7.3GHz and 8.7GHz impulse-based direct RF sampling radar SoC.

- In Paper 7.1, MediaTek describes a four 80MHz channel spatial stream WiFi 40nm CMOS SoC chip with integrated dual-band PAs, LNAs, and T/R switches. With the proposed RF architecture, a high output power of 22dBm for each spatial stream for 802.11ac Stage 2 VHT160 256QAM is achieved.
- In Paper 7.2, IBM describes a 28GHz phased-array IC in 0.13µm SiGe BiCMOS including 32 TRX elements and features concurrent independent beams in 2 polarizations in either TX or RX operation. A new TX/RX switch minimizes TX path loss resulting in 13.5dBm/16dBm OP_{1dB}/P_{sat} per FE with >20% PA+switch PAE while maintaining 6dB LNA+switch NF.
- In Paper 7.3, MediaTek describes a low-power transceiver architecture with an adaptive receiver for LTE-A Carrier Aggregation (CA). RX slicing of LNA/Mixer/TIA, and TX loadline adjustment allow the transceiver to achieve low power. This work achieves RX 2.5dB NF, TX 50dBc ACLR1, and 69mA battery current @ 4G Cat-7 with one TX and four RXs paths. It is realized in a 40nm CMOS process with area of 13.9 mm^2.
- In Paper 7.4, the University of Michigan and CubeWorks describe a 915MHz asymmetric radio, including a 0.18µm CMOS transceiver IC and a 3D magnetic antenna. For TX, the cross-coupled pair resonates the antenna with 32.4% efficiency consuming 2mW. For RX, the cross-coupled pair is reused at a non-oscillating region, enhancing resonant tank Q from 110 to 300 and resulting in -93dBm sensitivity while consuming 1.85mW.
- In Paper 7.5, CEA-LETI-MINATEC and Sigfox describes the first 65nm CMOS RF transceiver dedicated to sub-GHz ultra-narrow-band communication systems employing the DBPSK/GFSK modulations with data-rates as low as 100b/s. In DBPSK 100b/s transmission mode, an error vector magnitude (EVM) better than 5% is measured for output powers up to 10dB.
- In Paper 7.6, MediaTek describes A BLE/BDR transceiver fabricated in 55nm CMOS process. In BDR mode, the RF RX consumes 12mW to achieve -93.4dBm sensitivity with high ACI_3MHz <-46.5dBc. The TX consumes 79.6mW to deliver 8dBm output (BDR/BLE) with <-58dBc TX HD2, and < 64dBc HD3. In BLE mode, high sensitivity (-96.8dBm) and high TX output extend IoT coverage range.
- In Paper 7.7, Novelda and the University of Oslo describe a 1-bit direct RF sampling impulse-based radar with applications in non-contact vital sign monitoring, presence detection and ranging, realized in 55nm CMOS. The transmitter complies with ETSI, KCC, and FCC regulatory masks with -10dB bandwidths of 1.4GHz and 1.5GHz centered at 7.29GHz and 8.748GHz. The receiver front-end has 6.3dB NF and 14.7dB gain at 7.29GHz.

Session 7 Highlights: Wireless Transceivers

[7.2] A 28GHz 32-Element Phased-Array Transceiver IC with Concurrent Dual Polarized Beams and 1.4 Degree Beam-Steering Resolution for 5G Communication

[7.7] A 118mW 23.3GS/s Dual-Band 7.3GHz and 8.7GHz Impulse-Based Direct RF Sampling Radar SoC in 55nm CMOS

Paper 7.2 Authors: *B. Sadhu[1], Y. Tousi[1], J. Hallin[2], S. Sahl[3], S. Reynolds[1], O. Renstrom[3], K. Sjorgren[2], O. Haapalahti[3], N. Mazor[4], B. Bokinge[3], G. Weibull[2], J.-E. Thillberg[3], L. Rexberg[3], X. Gu[1], D. Friedman[1], A. Valdes-Garcia[1]*

Paper 7.2 Affiliation: *[1]IBM T. J. Watson Research Center, Yorktown Heights, NY, [2]Ericsson, Lindholmen, Sweden, [3]Ericsson, Kista, Sweden, [4]IBM Research, Haifa, Israel*

Paper 7.7 Authors: *N. Andersen[1], K. Granhaug[1], J. A. Michaelsen[1], S. Bagga[1], H. A. Hjortland[1], M. Risopatron Knutsen[1], T. S. Lande[2], D. T. Wisland[1,2]*

Paper 7.7 Affiliation: *[1]Novelda AS, Oslo, Norway, [2]University of Oslo, Oslo, Norway*

Subcommittee Chair: *Aarno Pärssinen, Wireless*

CONTEXT AND STATE OF THE ART

- Gb/s data rates required for 5G are pushing wireless communication at mm-wave frequencies where large bandwidth is available, but phased-array architectures are required to overcome path loss. Integration of phased-array transceivers in a single RFIC together with antennas in a single package is required to enable low-cost commercial solutions.
- Radar sensors operating below 10GHz enable a wide range of applications like non-contact vital-signs monitoring, such as breathing and heart rate, presence detection and ranging. Several ad-hoc solutions exist, but an SoC integrating all radar functions in a single piece of silicon while meeting unlicensed band regulations and showing robust interference rejection is required.

TECHNICAL HIGHLIGHTS

Monolithic 28GHz 32-element phased-array transceiver IC for 5G with dual-polarized antenna-in-package [7.2]

- In Paper 7.2, IBM describes a 28GHz phased array IC in 0.13µm SiGe BiCMOS including 32 TRX elements and features concurrent independent beams in 2 polarizations in either TX or RX operation. A new TX/RX switch minimizes TX path loss resulting in 13.5dBm/16dBm OP_{1dB}/P_{sat} per FE with >20% PA+switch PAE while maintaining 6dB LNA+switch NF.

Impulse radar SoC for non-contact vital signs monitoring demonstrating heartbeat detection at 5m [7.7]

- In Paper 7.7, Novelda and the University of Oslo describe a 1-bit direct RF sampling impulse-based radar with applications in non-contact vital sign monitoring, presence detection and ranging, realized in 55nm CMOS. The transmitter complies with ETSI, KCC, and FCC regulatory masks with -10dB bandwidths of 1.4GHz and 1.5GHz centered at 7.29GHz and 8.748GHz. The receiver front-end has 6.3dB NF and 14.7dB gain at 7.29GHz.

APPLICATIONS AND ECONOMIC IMPACT

- 5G is promising to deliver a 1000x increase in mobile data traffic. Wireless transceivers with bandwidth in excess of GHz operating at mm-wave are required to meet this challenge. Highly integrated phased-array systems will enable low-cost, commercial 5G solutions for both infrastructures and mobile terminals.
- Wireless sensors play a big role in the rapid growth of IoT. Compact, short/mid-range radar systems based on impulse radio below 10GHz will enable a variety of applications that will further enrich human life and promote healthier living.

Session 8 Overview: Digital PLLs and Security Circuits

Digital Circuits Subcommittee

Session Chair: *Yasuhisa Shimazaki, Renesas Electronics Corp., Tokyo, Japan*

Session Co-Chair: *John Maneatis, True Circuits, Los Altos, CA*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits*

The seven papers in this session highlight developments in security building blocks and clock generation. Improvements to random number generators and physically unclonable functions provide lower error rates and lower susceptibility to side-channel attacks. The digital PLLs presented are designed with synthesized logic, and incorporate a variety of features, including dynamic self adjustment to optimize noise and power, a noise-isolation LDO, and seamless lock ranges.

- In Paper 8.1, Georgia Institute of Technology obfuscates the current signature of an 128b AES core using a integrated voltage regulator (IVR) with a digital randomizer. Correlation power analysis attacks on the IVR-AES system were unsuccessful even with 100,000 trace measurements, while the standalone AES was attacked within 5000 traces. The area overhead for the enhanced security is 2135μm^2 in 130nm CMOS.
- In Paper 8.2, Pohang University of Science and Technology presents a true-random-number generator based on a differential ring oscillator with feedback resistors that eliminate the need for pre-tuning. The differential cell structure is tolerant to power noise attacks and process variations. The average bitrate is 8.2Mb/s and the energy efficiency is 28.2Mb/mJ at 1.08V with area of 920μm^2 in 65nm CMOS.
- In Paper 8.3, University of Michigan presents a physically unclonable function (PUF) based on a subthreshold 2-transistor amplifier in 180nm CMOS. The PUF cell has a 17.9μm^2 footprint and achieves 0.05% instability after 11b majority voting. A throughput of 4.8Gb/s is achieved and the PUF consumes 11.3/1.5fJ/b at 1.2/0.8V.
- In Paper 8.4, the University of Michigan describes a bang-bang phase-frequency-detector-based all-digital PLL. It uses an autonomous noise-locking scheme that provides dynamic self-adjustment of noise and power. The PLL achieves 2.5ps integrated jitter with 5mW power dissipation at 2.4GHz and area of 0.049mm^2 in 28nm SOI CMOS.
- In Paper 8.5, Tokyo Institute of Technology presents a supply-regulated synthesizable injection-locked PLL. It uses a noise-isolation LDO and is implemented entirely using a foundry-provided standard-cell library. The PLL achieves 0.42ps_{rms} integrated jitter with 3.8mW power dissipation and area of 0.028mm^2 in 65nm CMOS.
- In Paper 8.6, the University of Illinois at Urbana-Champaign describes a ring-based injection-locked clock multiplier using a frequency doubler and injection locking. It achieves 0.335ps_{rms} integrated jitter with 5.3mW power dissipation and area of 0.09mm^2 in 65nm CMOS.
- In Paper 8.7, Pohang University of Science and Technology presents a synthesizable fractional-N PLL. It is implemented without a TDC or DCO, and achieves a seamless lock range of reference frequency to 1GHz and area of 0.0047mm^2 in 28nm CMOS.

Session 8 Highlights: Digital PLLs and Security Circuits

[8.1] Improved Power-Side-Channel-Attack Resistance of an AES-128 Core via a Security-Aware Integrated Buck Voltage Regulator

[8.4] A 2.5ps 0.8-to-3.2GHz Bang-Bang Phase- and Frequency-Detector-Based All-Digital PLL with Noise Self-Adjustment

Paper 8.1 Authors: *M. Kar[1], A. Singh[1], S. Mathew[2], A. Rajan[2], V. De[2], S. Mukhopadhyay[1],*
Paper 8.1 Affiliation: *[1]Georgia Institute of Technology, Atlanta, GA ; [2]Intel, Hillsboro, OR*

Paper 8.4 Authors: *T. Jang[1], S. Jeong[1], D. Jeon[2], K. D. Choo[1], D. Sylvester[1], D. Blaauw[1]*
Paper 8.4 Affiliation: *[1]University of Michigan, Ann Arbor, MI ; [2]Seoul National University, Seoul, Korea*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits*

CONTEXT AND STATE OF THE ART

- Data security is of increasing importance. Providing important security functions, such as encryption/decryption, random-number generation, and others using hardware-based solutions offers excellent energy efficiency.
- Cryptography is one common security application performed on-chip – these building blocks are well known to be susceptible to side-channel attacks, particularly the monitoring of current/power profiles to disclose secret keys.
- Standard approaches to combat power-side channel attacks involve high-overhead techniques such as differential circuit design or other non-conventional design styles. Seamless low-overhead strategies to obscure power profiles are therefore desirable.
- Synthesized digital PLLs (DPLLs) can be synthesized from HDL using standard design tools, which reduces design times and improves technology portability.
- Autonomous noise locking PLLs allow dynamic power to be automatically optimized for a noise budget. This enables the PLL to operate at minimum power, while meeting the jitter targets for an application.
- A digital PLL using a free-running oscillator driving a digital accumulator and phase interpolator is locked to the reference clock and achieves fractional-N multiplication. This architecture enables a seamless lock range from the reference frequency to one quarter of the free running oscillator frequency.

TECHNICAL HIGHLIGHTS

Georgia Institute of Technology and Intel presents a security-enhanced 128b AES core, where the integrated voltage regulator is employed to obfuscate the current signature.

- In Paper 8.1, Georgia Institute of Technology obfuscates the current signature of an 128b AES core using a integrated voltage regulator (IVR) with a digital randomizer. Correlation power analysis attacks on the IVR-AES system were unsuccessful even with 100,000 trace measurements, while the standalone AES was attacked within 5000 traces. The area overhead for the enhanced security is 2135μm^2 in 130nm CMOS.

University of Michigan and Seoul National University presents an autonomous noise locking all-digital PLL.

- In Paper 8.4, the University of Michigan describes a bang-bang phase-frequency-detector-based all-digital PLL. It uses an autonomous noise-locking scheme that provides dynamic-self-adjustment of noise and power. The PLL achieves 2.5ps integrated jitter with 5mW power dissipation at 2.4GHz and area of 0.049mm^2 in 28nm SOI CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- With the increasing pervasiveness of IoT devices, data security has become an important issue. Hardware encryption for secure data transfer is essential to prevent economic loss from identity theft.
- Inexpensive secure data transfers reduce the cost of consumer transactions.
- Synthesizable digital PLLs can use standard digital design tools to dramatically reduce design costs and improve technology portability.

Session 9 Overview: *Sensors*

IMMD Subcommittee

Session Chair: *Pedram Lajevardi, Bosch Research and Technology Center, Palo Alto, CA, USA*

Session Co-Chair: *Masayuki Miyamoto, Sharp, Nara, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

This session exhibits recent advances in the state of the art of temperature, touch, and MEMs sensors. A highly energy-efficient temperature sensor implemented in CMOS, and a temperature sensor calibrated in two packages (plastic and ceramic) are reported. Two touch sensors are presented, the first being an energy-efficient sensor with passive stylus, and the second a capacitive sensor with active stylus, which can express pressure and tilt angle with 6b resolution at 3.9kHz. Also featured are a low-power MEMs gyroscope readout, and a low-noise MEMs microphone. An energy-efficient CMOS IC readout with low noise performance (<10nV/√Hz) is reported. An eddy current sensor interface achieves 60Å resolution, which is 100× better than the present state of the art.

- In Paper 9.1, Delft University of Technology, Ulm University, and Broadcom present an energy-efficient CMOS temperature sensor. It uses silicided resistors as an alternative to BJTs, and achieves 410μK_{rms} resolution in a 5ms conversion time, while consuming only 160μW. This corresponds to a resolution FoM of 0.13pJ·K^2, a 5× improvement over previous CMOS sensors.
- In Paper 9.2, University of Michigan presents a temperature sensor based on a self-regulated sub-threshold oscillator, demonstrating -0.22/+0.19°C inaccuracy with 73mK_{rms} resolution when referenced by a crystal oscillator and ±0.76 inaccuracy with 90mK resolution when referenced by a fully integrated RC oscillator.
- In Paper 9.3, Delft University of Technology presents a BJT-based temperature sensor, which can be accurately calibrated in both ceramic and plastic packages. This was achieved by combining the voltage calibration technique with an on-chip heater. Measurements show that the sensor can then be trimmed to an inaccuracy of ±0.3ºC (3σ) over the military range (–55 to +125ºC).
- In Paper 9.4, University of Freiburg – IMTEK and Hahn-Schickard present a signal-independent integrated BPF tuning circuit solely based on noise observation for a CT-M gyroscope readout system. A precision of 0.25% over a temperature range of 115°C is achieved. The readout system achieves a noise floor of 0.002°/s/√Hz and a bias instability of 0.9°/hour while consuming 1.71mW.
- In Paper 9.5, Infineon Technology presents a CMOS MEMS digital microphone. The IC features a full-scale of 140dB sound pressure level (SPL) and is capable of delivering an SNR of 67dB at the reference level of 94dB SPL based on a 3rd-order hybrid ΔΣ modulator.
- In Paper 9.6, Hanyang University, Leading UI, and Miraetns present a capacitive touch system using a multiple-frequency driving method to provide a high frame rate and gauge the pressure and tilt angle of the active stylus. The readout IC achieves a frame rate of 3.9kHz. The measured SNRs of finger and active stylus are 61.0 and 50.1dB, respectively, with a 65-inch 104×64 touch screen panel.
- In Paper 9.7, Yonsei University and Trais present a 120fps touch controller using current-driven delta-sigma ADCs, which achieves 41.7dB SNR for 1mm-diameter stylus. The readout IC supporting 28 TX and 50 RX channels consumes only 6.9mW.
- In Paper 9.8, Delft University of Technology presents an energy-efficient readout IC for low-noise Wheatstone bridge sensors. Powered from a 1.8V supply, the IC can handle ±10mV bridge signals accompanied by ±118mV bridge offset and up to 3.3V common-mode voltages. With a PEF of 44.1 and a 3.7nV/√Hz input-referred noise PSD, it is about 5× more efficient than the state of the art.
- In Paper 9.9, Delft University of Technology and Catena Microelectonics present a 0.6nm resolution 19.8mW eddy-current displacement sensor interface with 126MHz excitation. The interface is fabricated in 0.18μm CMOS and consumes 19.8mW.

Session 9 Highlights: Sensors

[9.4] A 27μW 0.06mm² Background Resonant Frequency Tuning Circuit Based on Noise Observation for a 1.71mW CT-$\Delta\Sigma$ MEMS Gyroscope Readout System with 0.9°/h Bias Instability

Paper 9.4 Authors: *Maximilian Marx, Daniel De Dorigo, Sebastian Nessler, Stefan Rombach, Michael Maurer, Yiannos Manoli*

Paper 9.4 Affiliation: *University of Freiburg – IMTEK, Freiburg, Germany ; Hahn-Schickard, Villigen-Schwenningen, Germany*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Today's gyroscopes are built based on either open-loop or closed-loop, mostly discrete-time delta-sigma converters. The regulation needed to achieve a high sensitivity and stability of the angular rate detection (precision by °/s/√Hz and long-term error is given in °/hour) is both power-hungry and often a reason for reduced long-term stability. The lowest-power solutions are open-loop, but rather imprecise. Continuous-time delta-sigma offers lower power than discrete-time-based regulation, however it is challenging to achieve drive frequency matching of the loop filter background tuning sub-circuit of the gyro readout.

TECHNICAL HIGHLIGHTS

Paper 9.4 presents a MEMS gyroscope employing a continuous-time delta-sigma loop for regulation. Background noise is measured and employed for tuning the frequency of the loop filter and for accurate tracking of the drive frequency over the operating temperature range up to 115°C.

- In Paper 9.4, University of Freiburg – IMTEK presents a signal-independent integrated BPF tuning circuit solely based on noise observation for a CT-M gyroscope readout system. A precision of 0.25% over a temperature range of 115°C is achieved. The readout system achieves a noise floor of 0.002°/s/Hz and a bias instability of 0.9°/hour while consuming 1.71mW.

APPLICATIONS AND ECONOMIC IMPACT

- Gyroscopes are heavily used today in many automotive applications (electronic stability control, but also autonomous driving) and consumer applications (like motion tracking in smart phones and gaming). Their main purpose is to detect and track motion and recognize gestures, or even help in location and positioning in indoor environments, where both low power and high angular stability are critical.

Session 9 Highlights: Sensors

[9.6] A 3.9kHz-Frame-Rate Capacitive Touch System with Pressure/Tilt Angle Expressions of Active Stylus Using Multiple-Frequency Driving Method for 65in 104×64 Touch Screen Panel

Paper 9.6 Authors: *J.-S. An1, S.-H. Han2, Y.-H. Kim2, H.-H. Hong2, S.-J. Jung1, S.-H. Lee1, J.-Y. Jung1, J.-H. Ye3, S.-K. Hong1, O.-K. Kwon1*

Paper 9.6 Affiliation: *[1]Hanyang University, Seoul, South Korea, [2]Leading UI, Anyang, South Korea, [3]MIRAETNS, Cheongju, South Korea*

Subcommittee Chair: *Makoto Ikeda, The University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- As the demand for interactive displays increases in the capacitive touch systems, the stylus drawing has become indispensable to represent various expressions. Although some active stylus solutions have been introduced, most of them have provided position and pressure information only, and their speed was limited by time division multiplexing with touch sensing. Faster touch-stylus solution providing more versatile functions has been demanded.

TECHNICAL HIGHLIGHTS

A 3.9 KHz frame rate capacitive touch system with active stylus has been proposed. The proposed IC employs a multiple frequency driving method to achieve the high frame rate, and the active stylus can express pressure and tilt angle with 6-bit resolution.

- In Paper 9.6, the measured SNRs of finger and active stylus are 61.0 and 50.1 dB, respectively with a 65-inch 104 x 64 touch screen panel.

APPLICATIONS AND ECONOMIC IMPACT

- Smartphones, tablets, and note PCs

Session 10 Overview: *DC-DC Converters*

Analog Subcommittee

Session Chair: Hoi Lee, *University of Texas at Dallas, Richardson, TX*

Session Co-Chair: Gerard Villar Pique, *NXP Semiconductors, Eindhoven, The Netherlands*

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, TX, Analog*

The session on DC-DC converters is about improvements of power density, power efficiency and power dissipation in switched-capacitor, hybrid, and inductor-based DC-DC converters. The first paper addresses the power efficiency and power-density tradeoff of switched-capacitor power conversion. The next four papers present innovative ideas in inductor- and capacitor-assisted hybrid DC-DC converters. This is followed by two high-frequency inductor-based DC-DC converters. Finally, the last paper focuses on sub-nW DC-DC converter design.

- In Paper 10.1, KU Leuven describes a soft charging technique and a MOS capacitor implementation to address the power efficiency and power-density tradeoff in switched-capacitor DC-DC converters. It simultaneously achieves high power efficiency of 82% and power density of 1.1W/mm^2 in a baseline 28nm CMOS process.
- In Paper 10.2, Dartmouth College presents a hybrid/resonant switched-capacitor converter. Fabricated in 0.18µm CMOS with a 5V power-device option, it achieves a record high power efficiency of 94.8% and cuts passive component size up to 5 times while handling 3.7W power.
- In Paper 10.3, UIUC demonstrates a 65nm CMOS hybrid Dickson switched-capacitor DC-DC converter. It provides power efficiency of 94.2% and peak power density of 0.24W/mm^2 to support a peak current of 1.53A.
- In Paper 10.4, KAIST describes a 0.18µm BCD hybrid inductor-based flying capacitor-assisted step-up/down converter. It offers peak power efficiency of 95.6% and maintains efficiency over 86% over the whole battery voltage range.
- In Paper 10.5, National Chiao Tung University demonstrates a 28nm CMOS three-level single-inductor triple-output DC-DC converter. Novel design techniques enable a transient response improvement by 12 times with small output ripple of 3mV and cross regulation within 8mV.
- In Paper 10.6, the Hong Kong University of Science and Technology shows a 30MHz 0.13µm CMOS DC-DC converter with a compensator for near-optimal transient response. Load transients are further assisted by the addition of a digital regulator to the output. This combination results in a 36mV output voltage drop and 125ns 1% settling time for a 1.25A load transient in 2ns.
- In Paper 10.7, the University of Texas at Dallas presents a 0.35µm CMOS 25MHz 4-phase hysteretic DC-DC converter for application processors. It achieves 190ns settling time for 4A load transient and peak power efficiency of 88%.
- In Paper 10.8, MIT describes a 65nm CMOS buck converter with power consumption optimization of the control loop for minimum quiescent current and a wide range of operating frequency (Hz to MHz). It only dissipates 240pW quiescent power.

Session 10 Highlights: DC-DC Converters

[10.8] A Buck Converter with 240pW Quiescent Power, 92% Peak Efficiency and a 2x10^6 Dynamic Range

Paper Authors: A. Paidimarri, A. Chandrakasan

Paper Affiliation: *Massachusetts Institute of Technology, Cambridge*

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin (USA), Analog*

CONTEXT AND STATE OF THE ART

- Switched-mode power supplies are crucial to bridge the voltage gap between energy sources and low-power systems in the most advanced CMOS technologies.
- However, due to the increasing trend of deeper duty-cycling of activity of systems, low quiescent power becomes as important as power efficiency in active mode.

TECHNICAL HIGHLIGHTS

Ultra-low quiescent power (240pW) achieved by the application of ultra-low power techniques at all design levels.

- In paper 10.8, the authors optimize power consumption of the control loop and the output stage for minimum quiescent current and for a wide range of operating frequency (Hz to MHz), which allows to efficiently supply a wide range of output current.

APPLICATIONS AND ECONOMIC IMPACT

- The relevance of the work becomes especially important in applications that are strongly energy constrained like wireless-sensor nodes with energy harvesting or battery-operated portable devices. The reported quiescent power becomes an enabler for such applications, whose market is expected to rapidly grow in the coming years.

Session 11 Overview: Nonvolatile Memory Solutions

Memory Subcommittee

Session Chair: *Takashi Kono, Renesas Electctonics, Tokyo, Japan*

Session Co-Chair: *Ki-Tae Park, Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Continued proliferation of semiconductors drives the evolution of nonvolatile memory technologies towards higher density, lower power consumption, and lower cost. This year, NAND Flash memories are demonstrated in 3D technologies with up to 64 stacked word-line layers. An embedded split-gate NOR Flash is also shown to dramatically reduce power consumption and meet the requirements of high-temperature sensing applications. Finally, logic antifuse one-time-programmable (OTP) memory is scaled down to the 10nm technology node.

- In Paper 11.1, Western Digital and Toshiba present a 512Gb 3b/Cell 3D NAND Flash with 64 stacked WL layers to achieve 3.88Gb/mm^2 areal density. A new precharge technique for unselected strings is proposed to obtain a larger V_T window. A 20% faster read-sensing scheme is introduced to improve read throughput.
- In Paper 11.2, The University of Michigan and TSMC present a 1Mb 90nm embedded split-gate NOR Flash macro suitable for mm-scale high-temperature sensing applications. A combined Dickson and Cockcroft-Walton charge pump scheme with a self-adjusted regulation loop enables the reduction of programming power to 39µW and 82µA at 25°C and 125°C, respectively.
- In Paper 11.3, TSMC introduces an antifuse one-time-programmable memory with the smallest cell to date using 10nm technology. The proposed read schemes reduce V_{min} and achieve immunity to data tampering, which makes the technology suitable for security-related applications.
- In Paper 11.4, Samsung presents a 512Gb 3b/Cell NAND Flash, which is the fourth generation of 3D NAND flash with 64 stacked WL layers. 1.2V I/O voltage supply contributes to increasing read bandwidth with low power. In order to overcome challenges due to vertical scaling, an on-chip processing algorithm for error correction is adopted.

Session 11 Highlights: Nonvolatile Memory Solutions

[11.1] A 512Gb 3b/Cell 3D NAND Flash Memory on 64-Word-Line-Layer Technology

[11.4] A 512Gb 3b/Cell 64 Stacked WL 3D V-NAND Flash Memory

Paper 11.1 Authors: *Ryuji RY Yamashita[1], Sagar Magia[2], Tsutomu Higuchi[3], Kazuhide Yoneya[3], Toshio Yamamura[3], Hiroyuki Mizukoshi[1], Shingo Zaitsu[1], Minoru Yamashita[1], Shunichi Toyama[1], Norihiro Kamae[1], Juan Lee[2], Shuo Chen[2], Jiawei Tao[2], William Mak[2], Xiaohua Zhang[2], Ying Yu[2], Yuko Utsunomiya[3], Yosuke Kato[1], Manabu Sakai[1], Masahide Matsumoto[1], Hardwell Chibvongodze[1], Naoki Ookuma[1], Hiroki Yabe[1], Subodh Taigor[2], Rangarao Samineni[2], Takuyo Kodama[3], Yoshihiko Kamata[3], Yuzuru Namai[3], Jonathan Huynh[2], Sung-En Wang[2], Yankang He[2], Trung Pham[2], Vivek Saraf[2], Akshay Petkar[2], Mitsuyuki Watanabe[1], Koichiro Hayashi[1], Prashant Swarnkar[2], Hitoshi Miwa[1], Aditya Pradhan[2], Sulagna Dey[2], Debasish Dwibedy[2], Thushara Xavier[2], Muralikrishna Balaga[2], Samiksha Agarwal[2], Swaroop Kulkarni[2], Zameer Papasaheb[2], Sahil Deora[2], Patrick Hong[2], Meiling Wei[2], Gopinath Balakrishnan[2], Takuya Ariki[1], Kapil Verma[2], Chang Siau[2], Yingda Dong[2], Ching-Huang Lu[2], Farookh Moogat[2]*

Paper 11.1 Affiliation: *[1]Western Digital, Yokohama, Japan, [2]Western Digital, Milpitas, CA, [3]Toshiba Semiconductor and Storage Products, Yokohama, Japan*

Paper 11.4 Authors: *Chulbum Kim, Ji-Ho Cho, Woopyo Jeong, Il-han Park, Hyun-Wook Park, Doo-Hyun Kim, Daewoon Kang, Sunghoon Lee, Ji-Sang Lee, Wontae Kim, Jiyoon Park, Yang-lo Ahn, Jiyoung Lee, Jong-hoon Lee, Seungbum Kim, Hyun-Jun Yoon, Jaedoeg Yu, Nayoung Choi, Yelim Kwon, Nahyun Kim, Hwajun Jang, Jonghoon Park, Seunghwan Song, Yongha Park, Jinbae Bang, Sangki Hong, Byunghoon Jeong, Hyun-Jin Kim, Chunan Lee, Young-Sun Min, Inryul Lee, In-Mo Kim, Sung-Hoon Kim, Dongkyu Yoon, Ki-Sung Kim, Youngdon Choi, Moosung Kim, Hyunggon Kim, Pansuk Kwak, Jeong-Don Ihm, Dae-Seok Byeon, Jin-yub Lee, Ki-Tae Park, Kye-hyun Kyung*

Paper 11.4 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- Current mainstream NAND Flash memory technology leverages 3b/cell and up to 48 stacked layers to achieve high density and low cost.
- Continued NAND Flash scaling will depend on the ability to further increase the number of stacked layers.

TECHNICAL HIGHLIGHTS

- **3b/cell 512Gb 3D NAND Flash with 64 stacked WL layers.**
- In Paper 11.1, Western Digital and Toshiba achieve area density of 3.88Gb/mm^2.
- A new precharge technique for unselected strings is demonstrated to obtain a wider V_T window for 3D structures. In addition, a 20% faster read sensing scheme is introduced for improving read throughput.
- In Paper 11.4, Samsung presents its 4th generation 3D NAND Flash.
- 1.2V I/O voltage supply contributes to increasing read bandwidth with low power. In order to overcome challenges due to vertical scaling, an on-chip processing algorithm for error correction is adopted.

APPLICATIONS AND ECONOMIC IMPACT

- Next-generation NAND Flash memories achieve 512Gb densities with high performance by leveraging 3D stacking technology and will be the major solid-state device for storage media.
- High-density and highly reliable 3D NAND combined with 3b/cell Flash memory will contribute to the growth of the SSD market, which is expected to be well over $25 billion USD in 2017.

Session 12 Overview: SRAM

Memory Subcommittee

Session Chair: *Fatih Hamzaoglu, Intel, OR*

Session Co-Chair: *Chun Shiah, Etron, Hsinchu, Taiwan*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

The growing demand for battery-powered mobile devices is the major driver to keep pushing power and area scaling for SoCs. This year, the SRAM session is headlined by the most advanced 7nm SRAM designs from both TSMC and Samsung. A novel dual-rail low-power SRAM design in 10nm from TSMC, and a two-phase-precharge ML sensing TCAM design from Globalfoundries in 14nm, are demonstrated.

- In Paper 12.1, TSMC presents a 7nm 256Mb SRAM in high-K metal gate FinFET technology with write-assist circuitry for low V_{min} Applications. It reports the smallest SRAM bit cell published to date at $0.027\mu m^2$.
- In Paper 12.2, Samsung presents a 7nm FinFET SRAM macro using EUV lithography for peripheral repair analysis. A 512Kb SRAM macro is implemented with detour logic to analyze the failure phenomena of bit cell array and peripheral. The proposed peripheral repair expects to improve V_{min} by 39.9 mV based on the failure analysis.
- In Paper 12.3, TSMC presents a low-power and high-performance 10nm SRAM architecture for mobile applications, with innovative dual-rail SRAM architecture. It achieves superior power savings and performance scaling when compared to the previous 16nm technology node.
- In Paper 12.4, Globalfoundries presents 1.4Gsearch/sec $2Mb/mm^2$ TCAM using a two-phase-precharge ML sensing and power-grid pre-conditioning to reduce Ldi/dt power-supply noise by 50%. To reduce within-cycle noise, a two-phase match-line pre-charge cuts the current on easy-to-detect multibit mismatched MLs early to save 60% ML power and 52% power supply noise.

Session 12 Highlights: SRAM

[12.1] A 7nm 256Mb SRAM in High-K Metal Gate FinFET Technology with Write-Assist Circuitry for Low V_{min} Applications

[12.2] A 7nm FinFET SRAM Macro using EUV Lithography for Peripheral Repair Analysis

Paper 12.1 Authors: *J. Chang, Y.H. Chen, G. Chan, S. P. Singh, H. Cheng, H. Fujiwara, J.Y. Lin, K. C. Lin, R. Lee, J. J. Liaw, Q. Li, C.Y. Lin, M.C. Chiang, S.Y. Wu*

Paper 12.1 Affiliation: *TSMC, Hsinchu, Taiwan*

Paper 12.2 Authors: *T. Song, H. Kim, D. Ha*

Paper 12.2 Affiliation: *Samsung Electronics, Gyeonggi-do, Korea, Republic of*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- SRAM continues to scale over process technologies since first implemented in 22nm node.
- Both TSMC and Samsung demonstrated a functional MByte-level SRAM array in a 7nm process node.
- Both companies have scaled SRAM below 0.030μm^2 area, where TSMC reports record 0.027μm^2 bitcell area.

TECHNICAL HIGHLIGHTS

256Mb SRAM in 7nm technology functional at a core supply voltage of 0.75V

- In Paper 12.1, TSMC presents a 7nm 256Mb SRAM in a high-K metal gate FinFET technology with write-assist circuitry for low V_{min} applications. It reports the smallest SRAM bit cell published to date at 0.027μm^2.

8Mb SRAM in 7nm using EUV Lithography functional with optimized bitcell and periphery repair schemes

- In Paper 12.2, Samsung presents a 7nm FinFET SRAM macro using EUV lithography for peripheral repair analysis. A 512kb SRAM macro is implemented with detour logic to analyze the failure phenomena of bit cell array and peripheral. The proposed peripheral repair expects to improve V_{min} by 39.9mV based on the failure analysis.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrate that SRAM and logic can scale to 7nm technology with 0.027μm^2 SRAM bitcell area, the smallest ever reported.
- Optimal repair schemes, read/write assist techniques and strapped wordline and segmented bitline metals continue to enable high-speed and low-voltage MByte level array functionality, which is crucial for cost-effective and low-power chips.

Session 13 Overview: High Performance Transmitters

Wireless Subcommittee

Session Chair: *Guang-Kaai Dehng, MediaTek, Hsinchu, Taiwan*

Session Co-Chair: *Kyoohyun Lim, FCI, Gyeonggi, Korea*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Espoo, Finland, Wireless*

This session describes state-of-the-art transmitter and PA designs implemented in deep-submicron CMOS processes featuring low noise, wide bandwidth, and high efficiency. It includes a multi-mode front-end Module with CMOS PA for GSM/EDGE/TD-SCDMA/TD-LTE application, a 14nm SAW-less transmitter with a voltage-mode harmonic-reject mixer, a 28nm multilevel outphasing transmitter enabling 400MHz instantaneous bandwidth, a 28nm digital polar transmitter supporting 40MHz LTE Carrier Aggregation (CA), a 28.6dBm CMOS digital PA with 35% PAE, a 24dBm digital PA with built-in AM-PM distortion self-compensation and several digital PA/transmitter designs for cellular, 802.11, IoT, and wearable applications.

- In Paper 13.1, Mediatek presents the first and most compact fully integrated multimode TDD front-end module supporting multiband GSM/EDGE/TD-SCDMA/TD-LTE using a 0.153µm CMOS PA. The module achieves +34dBm P_{sat} at the antenna port, 36.8% PAE in LB GSM mode and < -33dBm spurious harmonic emissions in all modes.
- In Paper 13.2, Intel, DPMA, and DMCE introduce a 28nm CMOS digital polar transmitter based on signed amplitude path and switched-capacitor RFDAC limits large phase jumps in the DPLL with a high-resolution RFDAC, achieving 3.6% EVM in 40MHz LTE CA (2xLTE20) while fulfilling 3G TX noise of -159dBc/Hz at 6dBm output power.
- In Paper 13.3, Samsung describe a three-phase passive harmonic-reject mixer (HRM) used in 14nm CMOS LTE transmitter for SAW-less operation. The broadband $3F_{LO}$ suppression technique achieves a CIM3 of -68dBc and noise of -155dBc in LTE-B13 single-RB mode with 50% DC power consumption compared to prior art.
- In Paper 13.4, Aalto University and Huawei demonstrate a 28nm CMOS all-digital RF transmitter using programmable digital noise shaping of RX-band noise, achieving -155 to -163dBc/Hz noise at a programmable duplex distance, achieves CIM3/CIM5 < -67dBc, and ACLR < -60dBc with LTE20 carrier, with active area of 0.82mm^2.
- In Paper 13.5, Aalto University, Tampere University of Technology and Nokia present a multilevel outphasing transmitter in 28nm FDSOI CMOS. The transmitter achieves the widest reported instantaneous bandwidth of 400MHz at 2GHz carrier frequency.
- In Paper 13.6, Intel, Fudan University, Movellus Circuits, and Radiawave Technologies present a WLAN 2.4GHz digital polar transmitter in 14nm trigate/finfet technology. The PA achieves peak PA PAE of 32% for 19dBm P_{out} and 25% PAE for 14dBm P_{out} for -25dB EVM with 54Mb/s 64QAM. The TX core area is 0.27mm^2.
- In Paper 13.7, Marvell presents an inverse Class-D digital power amplifier (DPA). This 0.23mm^2 DPA in 28nm CMOS achieves 28.2dBm peak output power and 39% peak drain efficiency at 2.45GHz. For 20MHz 64-QAM OFDM signals, average output power is 22.5dBm and power-added efficiency is 28% with -25dB EVM.
- In Paper 13.8, Georgia Institute of Technology and Intel present a 24dBm 2-to-4.3GHz 28nm CMOS wideband digital polar power amplifier with built-in AM-PM distortion compensation techniques. The measured rms EVM with 20MSym/s 64-QAM and 256-QAM signals are 2.55% and 2.39% without any phase pre-distortion.
- In Paper 13.9, Intel and Padova University present a switched-capacitor 28nm CMOS digital PA featuring 28.6dBm P_{sat} at 35% PAE while operating directly from 1.1V digital-core supply voltage without the need for any DPD.
- In Paper 13.10, Columbia University describes a 65nm CMOS digital transmitter that achieves -149dBc/Hz RX-band noise level with 30.3dBm P_{sat} by embedding mixed-domain multi-tap FIR filtering with programmable analog sub-sample delays within a highly linear and mismatch-resilient switched-capacitor digital transmitter architecture.

Session 13 Highlights: High Performance Transmitters

[13.4] All-Digital RF Transmitter in 28nm CMOS with Programmable RX-Band Noise Shaping

[13.9] A 1.1V, 28.6dBm Fully Integrated Digital Power Amplifier for Mobile and Wireless Applications in 28nm CMOS Technology with 35% PAE

[13.10] A >1W 2.2GHz Switched-Capacitor Digital Power Amplifier with Wideband Mixed-Domain Multi-Tap FIR Filtering of OOB Noise Floor

Paper 13.4 Authors: *Enrico Roverato[1], Marko Kosunen[1], Koen Cornelissens[2], Sofia Vatti[2], Paul Stynen[2], Kaoutar Bertrand[2], Teuvo Korhonen[2], Hans Samsom[2],* Patrick Vandenameele[2], Jussi Ryynänen[1]
Paper 13.4 Affiliation: *[1]Aalto University, Espoo, Finland, [2]Huawei Technologies, Leuven, Belgium*

Paper 13.9 Authors: *Antonio Passamani[1], Davide Ponton[1], Edwin Thaller[1], Gerhard Knoblinger[1], Andrea Neviani[2], Andrea Bevilacqua[2]*
Paper 13.9 Affiliation: *[1]Intel Austria GmbH, Villach, Austria, [2]University of Padova, Padova, Italy*

Paper 13.10 Authors: *Ritesh Bhat, Jin Zhou, Harish Krishnaswamy*
Paper 13.10 Affiliation: *Columbia University, New York, NY*

Subcommittee Chair: *Aarno Parssinen, University of Oulu, Finland, Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- High output power and highly efficient PAs in deep sub-micron CMOS processes have been difficult to implement using low supply voltages compatible with state-of-the-art CMOS technologies
- Programmable FIR filtering techniques are needed to reduce or expand noise at RX band for multimode/multiband CMOS PAs and transmitters for FDD applications.

TECHNICAL HIGHLIGHTS

A low-voltage fully-integrated digital PA in 28nm CMOS for smart phones

- In paper [13.9], Intel presents a switched-capacitor digital PA featuring 28.6dBm P_{sat} at 35% PAE while operating directly from 1.1V digital core supply voltage. For the LTE5 10, WIFI20/WIFI40 test cases, the measured EVM is 3.2/3.8%, and 4.3/5.4% at an average output power of 20.7dBm and 17.3dBm, respectively, without the need for any DPD.

Programmable wideband FIR filtering technique for power amplifiers and transmitters [13.10] [13.4]

- In paper [13.10], Columbia University describes a digital transmitter that achieves -149dBc/Hz RX-band noise level with 30.3dBm P_{sat} by embedding mixed-domain multi-tap FIR filtering with programmable analog sub-sample delays within a highly linear and mismatch-resilient switched-capacitor digital transmitter architecture.
- In paper [13.4], Aalto University demonstrates an all-digital RF transmitter using programmable digital noise shaping of RX-band noise achieving -155 to -163dBc/Hz noise at a programmable duplex distance, with only 10-bit DAC and no DPD, calibration or analog filtering. The transmitter achieves CIM3/CIM5 < -67dBc, and ACLR < -60dBc with LTE20 carrier. Implemented in 28nm CMOS, the circuit consumes 150mW from 0.9/1.5V supplies at +3dBm output power with active area of 0.82mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- Modern battery-operated cell phones and IoT devices call for both very low supply voltages and excellent PA efficiency to achieve long operation times without recharging. Paper 13.9 shows excellent efficiency using only 1.1V supply compatible with high-reliability requirements for cellular operation.

Session 14 Overview: Deep Learning Processors

Digital Architecture and Systems Subcommittee

Session Chair: *Takashi Hashimoto, Panasonic, Osaka, Japan*

Session Co-Chair: *Mahesh Mehendale, Texas Instruments, Bangalore, India*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, DAS*

Processors targeting embedded perception and cognition have evolved tremendously in the past decade. Thanks to CMOS process scaling, the cost in terms of area and energy per operation have decreased drastically. This makes it feasible to equip next-generation processing with human-like intelligence for emerging applications, such as detection, recognition, and classification.

This session covers highly integrated embedded next-generation processing systems for improved accuracy of speech recognition, face recognition for next-generation UI/UX of wearable devices. In addition, programmable or scalable deep-learning accelerators for Convolutional Neural Networks (CNNs) and Recurrent Neural Networks (RNNs), and fully programmable deep learning SoCs are presented. The session concludes with a data processor for Next-Generation Sequencing (NGS).

- In Paper 14.1, STMicroelectronics presents a deep convolutional neural network SoC in 28nm FDSOI with energy efficiency of 2.9TOPS/W and peak performance of more than 676GOPS, operating at 200MHz with supply voltage of 0.575V.
- In Paper 14.2, KAIST presents a reconfigurable CNN-RNN processor SoC in 65nm CMOS with energy efficiency of 8.1TOPS/W, operating at 50MHz with supply voltage of 0.77V.
- In Paper 14.3, Harvard University presents a fully connected (FC)-DNN accelerator SoC in 28nm CMOS, which achieves 98.5% accuracy for MNIST inference with 0.36μJ/prediction at 667MHz and 0.57μJ/pred at 1.2GHz.
- In Paper 14.4, MIT presents an IC designed in a 65nm LP process for DNN-based automatic speech recognition (ASR) and voice-activity detection (VAD). Real-time ASR capability scales from 11 words (17μW) to 145k words (7.78mW) and the noise-robust VAD has power consumption of 22.3μW.
- In Paper 14.5, KU Leuven presents an energy-scalable CNN processor in 28nm FDSOI achieving efficiencies up to 10TOPS/W by modulating computational accuracy, voltage and frequency, while maintaining recognition rate and throughput.
- In Paper 14.6, KAIST presents an ultra-low-power CNN-based face recognition (FR) processor and a CMOS image sensor integrated with always-on Haar-like face detector in 65nm CMOS. The analog-digital hybrid Haar-like face detector improves the energy efficiency of face detection by 39% and the FR system dissipates 0.62mW at 1fps.
- In Paper 14.7, University of Michigan presents a programmable fully connected (FC)-DNN accelerator in 40nm CMOS. It achieves 374GOPS/W at 0.65V (288μW) and 3.9MHz, with configurable data precision, strategic data assignment in NUMA memory (270KB) and dynamic drowsy memory operation,
- In Paper 14.8, National Taiwan University presents a data processor for Next-Generation Sequencing (NGS) in 40nm CMOS, which realizes DNA mapping, including suffix-array (SA) sorting and backward searching. With 135mW at 200MHz, it achieves significantly higher energy efficiency over CPU/GPU-based implementations.

Session 14 Highlights: Deep Learning Processors

[14.1] A 2.9TOPS/W Deep Convolutional Neural Network SoC in FDSOI 28nm for Intelligent Embedded Systems

[14.4] A Scalable Speech Recognizer with Deep-Neural-Network Acoustic Models and Voice-Activated Power Gating

Paper 14.1 Authors: *G. Desoli[1], N. Chawla[2], T. Boesch[3], S. Singh[2], E. Guidetti[1], F. Ambroggi[4], T. Majo[1], P. Zambotti[4], M. Ayodhyawasi[2], H. Signh[2] and N. Aggarwal[2]*

Paper 14.1 Affiliation: *[1]STMicroelectronics, Cornaredo, Italy; [2]STMicroelectronics, Greater Noida, India; [3]STMicroelectronics, Geneva, Switzerland; [4]STMicroelectronics, Agrate Brianza, Italy*

Paper 14.4 Authors: *M. Price, J. Glass and A. Chandrakasan*

Paper 14.4 Affiliation: *Massachusetts Institute of Technology, Cambridge, MA*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, DAS*

CONTEXT AND STATE OF THE ART

- Deep learning has recently demonstrated state-of-the-art accuracy on many computer vision tasks, such as object detection, recognition, and segmentation. Embedded implementations of state-of-the-art deep-learning networks require the efficient execution of millions of convolution operations and memory accesses per second, and fully programmable solutions.
- Accuracy and programmability of current state-of-the-art speech recognition approaches are inefficient. The power and system complexity pose significant challenges for applications such as next-generation wearables and robots.

TECHNICAL HIGHLIGHTS

Paper 14.1: First reported efficient deep-learning SoC is presented by STMicroelectronics capable of flexibly mapping state-of-the-art deep neural networks.

- An energy-efficient deep convolutional neural network (CNN) SoC is presented by STMicroelectornics and implemented in a 28nm FDSOI process. The SoC integrates a host CPU, a 16 DSP array and a convolutional DNN accelerator fed by an on-chip reconfigurable network that reduces on-chip and off-chip memory traffic.

Paper 14.4: Standalone hardware recognizer achieved by MIT through well-tailored DNNs with limited network width and quantized, sparse weight matrices.

- A low-power standalone speech recognizer with a voice activity detection mechanism for wake-up, and a feed-forward DNN accelerator for speech recognition is implemented by MIT in 65nm CMOS. It achieves 4.1× fewer word errors, 3.3× lower core power consumption and 12.7× lower memory bandwidth over the latest speech recognizer.

APPLICATIONS AND ECONOMIC IMPACT

- Machine learning is a major trend today, due to the availability of powerful computing, growing data volumes, and the progress being made in the development of smart algorithms. The era of smart machines is forecast to become one of the most disruptive phases in the history of IT according to the Gartner market research company. The market for machine learning is growing in line with this technology's increasing importance. According to BCC Research, the global market for smart machines is forecast to grow to $15.3 billion by 2019, with an average annual growth rate of 19.7 percent.
- The ability to perform highly accurate speech detection and recognition is the key enabler towards different emerging application domains, such as wearable devices, autonomous vehicles and natural human-machine interaction.

Session 15 Overview: Innovations in Technologies and Circuits

Technology Directions Subcommittee

Session Chair: *Jan Genoe, imec, Belgium*

Session Co-Chair: *Hiroshi Fuketa, AIST, Japan*

Subcommittee Chair: *Eugenio Cantatore,* Eindhoven University of Technology*, The Netherlands, Technology Directions*

This session covers a diverse set of novel technologies and circuits. The first 3 papers of this session implement circuits in large area technologies. Subsequent papers describe optical beam steering, interfaces to scalable quantum computing, ultra-high-resolution gravimetric mass sensing using NEMS arrays, dopamine sensing using graphene electrodes, $4F^2$ X-point technologies for archive systems, and integrated photonic crystals for physically unclonable functions (PUFs).

- In Paper 15.1, Princeton University presents a system for acquisition from a large number of large-area sensors into a CMOS IC via minimal number of interfaces. A prototype with 18 pressure sensors and 8 frequency-hopping channels achieves an acquisition error <0.27% over the entire range for all sensors.
- In Paper 15.2, imec, AU Optronics, and KU Leuven present a flexible 128b IGZO RFID tag compliant with the ISO14443-A NFC barcode standard, enabling readout by standard NFC readers. The on-chip clock is generated by direct clock division from a 13.56MHz carrier wave by using a self-aligned IGZO technology with L< 2μm and 2.4ns gate delay.
- In Paper 15.3, Eindhoven University of Technology and Holst Centre present an asynchronous delta-sigma modulator (ADSM) realized in an a-IGZO technology that is able to transform analog inputs to a robust PWM representation. The ASDM achieves 55dB SNR, 50dB SNDR in 10Hz BW, and 43dB SNR, 40dB SNDR in 300Hz BW.
- In Paper 15.4, University of Southern California presents a 1024-element monolithic optical phased array prototype operating at the 1550nm wavelength, targeting autonomous navigation. The system achieves 0.03° beam-width and 45° steering angle.
- In Paper 15.5, Delft University of Technology, EPFL, and Intel present building blocks for a scalable CMOS interface to solid-state quantum processors with a projected efficiency of 200μW/qubit. The circuits include an analog noise-canceled 1.2GHz LNA with 28dB gain, a 6.2GHz class-F local oscillator with better than –145dBc/Hz phase noise at 10MHz offset, a 12μm SPAD with 0.1Hz dark count rate at 2V excess bias, and digital logic, all designed using ad hoc deep-cryogenic models.
- In Paper 15.6, CEA presents a NEMS array gravimetric sensing pixel-based circuit. The compact (26000μm^2) heterodyne 30-to-80MHz self-oscillator analog front-end IC performs fast (1ms) simultaneous dual-mode frequency tracking and achieves with the NEMS sensor 300 zeptogram mass resolution.
- In Paper 15.7, New York University presents a multi-electrode array of dopamine sensors built transferring epitaxial graphene on top of a CMOS chip. The measured sensitivity of the electrode is ~14nA/μM and the ADC resolution is 40pA.
- In Paper 15.8, Kobe University presents a $4F^2$ permanent digital archive system using a metal nano-dot at the X-point of interconnects. A 0.18μm CMOS prototype successfully operates after accelerated 1000-year aging.
- In Paper 15.9, Princeton University presents an optical PUF that exploits integrated copper interconnects to build process-sensitive photonic crystals whose band edge is subject to large changes with lithographic variations. The PUF achieves a uniqueness of 49.81% and native stability of 99.75% at nominal conditions, with a native Inter/Intra-Hamming Distance ratio of 198.

Session 15 Highlights: Innovations in Technologies and Circuits

[15.1] Large-Scale Acquisition of Large-Area Sensors using an Array of Frequency-Hopping ZnO Thin-film Transistor Oscillators

Paper Authors: *Y. Afsar, T. Moy, N. Brady, S. Wagner, J. Sturm, N. Verma*

Paper Affiliation: *Princeton University, Princeton, NJ*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Large-area electronics enables the creation of many distributed sensors on flexible and/or stretchable surfaces, but the transistors have low performance, limiting accurate analog and digital processing of the sensor information.
- Hybrid systems combine large-area electronics for sensing and silicon CMOS for computation, but are limited by the interfaces required between the two technologies. This necessitates highly scalable methods for interfacing a large number of sensors through a minimal number of physical interconnects.

TECHNICAL HIGHLIGHTS

- Extremely scalable acquisition over an array of distributed large-area sensors is made possible through frequency-hopping thin-film-transistor oscillators.
- Employing high-frequency high-spectral-purity LC oscillators in a distributed fashion together with frequency hopping leads to combinatorial scaling, enabling more sensors to be accessed through a small number of interfaces to a CMOS chip as compared to active matrices or binary addressing.

APPLICATIONS AND ECONOMIC IMPACT

- Frequency-hopping sensor-acquisition system enables an extremely large number of distributed sensors in large-area electronics to be processed efficiently via minimal interfaces to silicon-CMOS chips. This can enable entirely new sensing paradigms for IoE applications, such as flexible sensor surfaces and wearable sensors

Session 15 Highlights: Innovations in Technologies and Circuits

[15.5] Cryo-CMOS Circuits and Systems for Scalable Quantum Computing

Paper Authors: *E. Charbon[1,2,3], F. Sebastiano[1], M. Babaie[1], A. Vladimirescu[4,5], M. Shahmohammadi[1], R.B. Staszewski[1], H.A.R. Homulle[1], B. Patra[1], J.P.G. van Dijk[1], R.M. Incandela[1], L. Song[1,6], B. Valizadehpasha[1].*

Paper Affiliation: *1. Delft University of Technology, Delft, The Netherlands 2. EPFL, Lausanne, Switzerland, 3. Intel, Hillsboro, OR, 4. University of California, Berkeley, Berkeley, CA, 5. Institut Supérieur d'Electronique de Paris, Paris, France, 6 Tsinghua University, Beijing, China*

Subcommittee Chair: *E. Cantatore, Eindhoven University of Technology, Eindhoven, Technology Directions*

CONTEXT AND STATE OF THE ART

- Quantum processors require very sophisticated support from non-quantum electronics to maintain coherence and to correct for operating errors.
- It is believed that quantum computer scalability will only be achieved by means of highly miniaturized circuits and systems capable of interfacing with millions of quantum bits (qubits) at temperatures near absolute zero. Cryogenic CMOS (cryo-CMOS) technology is well positioned to achieve just that, provided that a very low power dissipation per qubit will be achievable at very high operating speed and low noise.

TECHNICAL HIGHLIGHTS

- Delft University of Technology, EPFL, and Intel present a scalable CMOS interface to solid-state quantum processors with a projected efficiency of 200μW/qubit. The interface includes an analog noise-canceled 1.2GHz LNA with 28dB gain, a 6.2GHz class-F local oscillator with better than –145dBc/Hz phase noise at 10MHz offset, a 12μm SPAD with 0.1Hz dark count rate at 2V excess bias, and digital logic, all designed using ad-hoc deep-cryogenic models.

APPLICATIONS AND ECONOMIC IMPACT

- In the near term, it is unlikely to find a quantum computer on ones laptop or mobile. However, this technology will have an impact in supercomputers and data centers in the future.
- Cryo-CMOS technology will create new opportunities that may have an immediate impact on today's technology, potentially improving speed and overall power.

Session 16 Overview: Gigahertz Data Converters

Data Converter Subcommittee

Session Chair: *Jan Mulder, Broadcom Ltd, Bunnik, The Netherlands*
Session Co-Chair: *Paul Ferguson, Analog Devices, Wilmington, MA*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

Circuit and architectural innovations have enabled medium and high-resolution data converters to push bandwidths beyond 1GHz. This entire session is devoted to gigahertz data converters covering resolutions up to 14b and sampling rates up to 10GS/s. The ADC papers in this session make extensive use of dynamic amplifiers and comparators, calibrations for offsets, timing, gain errors and transfer functions, and randomization techniques. An oversampled continuous-time pipeline ADC architecture combines the wide bandwidth of a pipeline ADC with the antialiasing properties of a continuous-time oversampling converter. The DAC papers employ mixing techniques in the analog or digital domains for direct up-conversion up to 21GHz.

- In Paper 16.1, Xilinx presents a 13b 4GS/s asynchronous pipelined SAR ADC in 16nm CMOS. The ADC features multiple on-chip calibration loops that enable the use of open-loop integrator-based amplifiers thus achieving 57.3dB SNDR for a 1.9GHz input signal.
- In Paper 16.2, Analog Devices introduces a 9GS/s 1GHz-BW oversampled continuous-time pipeline ADC in 28nm CMOS. This new ADC architecture simultaneously achieves the wide bandwidth of a pipeline ADC and the antialiasing properties of a continuous-time oversampled converter, reaching a -161dBFS/Hz NSD.
- In Paper 16.3, Xilinx describes a 14b 6.8GS/s RF-DAC in 16nm CMOS. By realizing a mixing function in the data path, the DAC attains a -70.8dBc ACPR in a 20MHz channel at 5.2GHz while consuming 330mW.
- In Paper 16.4, The University of Macau presents a 7b, 2.4GS/s SAR ADC in 28nm CMOS. The 1b-then-2b/cycle algorithm skips the DAC operation during the first cycle and enables background calibration of the comparator offsets, leading to a power consumption of 5mW.
- In Paper 16.5, Keysight Technologies introduces an 8GS/s SAR ADC with 4GHz bandwidth in 28nm CMOS achieving 60.3dB SFDR at 3.8GHz input. Detecting late comparator decisions lowers power consumption to 300mW while allowing for improved resolution and metastability error rate.
- In Paper 16.6, Ohio State University presents a 20GHz multiple-return-to-zero DAC in 0.13µm SiGe BiCMOS. The converter uses a vertically stacked output tree combined with timing and amplitude calibration to achieve >48dB SFDR from DC to 21GHz with 1.65GHz bandwidth.
- In Paper 16.7, Analog Devices describes a 12b pipeline ADC in 28nm CMOS sampling at 10GS/s. Using multiple calibration and randomization techniques, the ADC achieves 55dB SNDR for a 4GHz input signal while consuming 2.9W.

Session 16 Highlights: Gigahertz Data Converters

[16.3] A 330mW 14b 6.8GS/s Dual-Mode RF-DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz

[16.7] A 12b 10GS/s Interleaved Pipeline ADC in 28nm CMOS Technology

Paper 16.3 Authors: Christophe Erdmann, Edward Cullen, Damien Brouard, Roberto Pelliconi, Bob Verbruggen, John Mcgrath, Diarmuid Collins, Marites De La Torre, Pierrick Gay, Patrick Lynch, Peng Lim, Anthony Collins, Brendan Farley

Paper 16.3 Affiliation: Xilinx, Dublin, Ireland

Paper 16.7 Authors: Siddharth Devarajan[1], Larry Singer[1], Dan Kelly[1], Steve Kosic[2], Tao Pan[1], Jose Silva[1], Janet Brunsilius[2], Daniel Rey-Losada[2], Frank Murden[3], Carroll Speir[3], Jeff Bray[2], Eric Otte[1], Nevena Rakuljic[2], Phil Brown[3], Todd Weigandt[2], Qicheng Yu[1], Donald Paterson[1], Corey Petersen[2], Jeffrey Gealow[1]

Paper 16.7 Affiliation: [1]Analog Devices, Wilmington, MA, [2]Analog Devices, San Diego, CA, [3]Analog Devices, Greensboro, NC

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

CONTEXT AND STATE OF THE ART

- High-bandwidth data converters, with bandwidths above 1GHz, are required in future instrumentation and communication applications.
- Advanced IC technologies, like 28nm and 16nm FinFET CMOS, allow data converters to push the traditional bandwidth limits and shift traditionally analog functions into the digital domain.
- Extensive calibration, randomization and interleaving techniques break the traditional limitations between resolution, noise, area, and power consumption.

TECHNICAL HIGHLIGHTS

The DAC described by Xilinx achieves -70.8dBc ACPR in a 20MHz channel at 5.2GHz while consuming 330mW.

- Xilinx exploits the speed of 16nm FinFET CMOS to move a DAC mixing function from the analog to the digital domain. The DAC has a resolution of 14b and a 6.8GS/s sample rate.

Analog Devices demonstrates a highly time-interleaved 12b pipeline ADC in 28nm CMOS sampling at a record 10GS/s.

- Using multiple calibration and randomization techniques, the ADC achieves 55dB SNDR at 4GHz input signal while consuming 2.9W.

APPLICATIONS AND ECONOMIC IMPACT

- High-bandwidth data converters enable future instrumentation and communication applications.
- New techniques help to reduce power consumption and save system cost by reducing area and integrating functions in a single chip.

Session 17 Overview: TX and RX Building Blocks

RF Subcommittee

Session Chair: *Brian Ginsburg, Texas Instruments, Dallas, TX*

Session Co-Chair: *Payam Heydari, UC Irvine, Irvine, CA*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF*

RF transceivers enable everything from the plethora of connectivity on mobile devices to emerging applications in fixed point-to-point links, imaging, and sensing. Advances across all aspects of signal generation, modulation, power amplification, and radiation are required to reduce power dissipation while increasing performance. The papers in this session highlight several advances in the state of the art in RF, mm-wave, and THz domains. Antenna interface improvements include a circulator for TX/RX isolation, a digitally assisted CMOS front-end module, a polar PA with intrinsic nonlinearity compensation, electrical-balance-duplexer impedance detection, and radiator-embedded power combining. Wideband systems for spectroscopy achieve a wide bandwidth for integrated spectroscopy and parallel multi-tone generation. A 310-to-370GHz array embeds beam steering with independent frequency tuning. High data-rate communication is demonstrated with a 5m 130GHz 12.5Gb/s link and a 105Gb/s 300GHz transmitter.

- In Paper 17.1, MediaTek describes a digitally assisted CMOS WiFi 802.11ac/11ax front-end module. The TX path delivers 20dBm output power with -35dB EVM and 12%/10% PAE. The RX path achieves a 2.6dB NF and a 12.5dB gain while consuming 9mA from a 2.5V supply.
- In Paper 17.2, Columbia University describes a magnetic-free non-reciprocal passive CMOS circulator. Operating at 28GHz, the circulator achieves 3.2/3.3dB insertion losses, 1dB-insertion-loss bandwidth of 4.6GHz, >21dBm P_{1dB} and ~4dB NF using sub-harmonic spatial-temporal conductance modulation.
- In Paper 17.3, Georgia Institute of Technology presents a 60GHz on-chip linear radiator. Using a multifeed antenna with direct on-antenna power combining, the transmitter generates 27.9dBm P_{sat} and 33.1dBm peak EIRP with 23.4% PAE at 59GHz. Without pre-distortion, it achieves -21.9dB EVM with 20.2dBm P_{avg} for a 4Gb/s 16-QAM signal.
- In Paper 17.4, imec describes antenna impedance detection for single-step on-chip tunable matching. Consuming only 0.83mW, the Cartesian detection embedded within an electrical balance duplexer demonstrates an accuracy of 18 degrees of phase and 0.1 of magnitude of the antenna reflection coefficient.
- In Paper 17.5, Delft University of Technology and Ampleon show a wideband, intrinsically linear digital PA. Nonlinear sizing, overdrive-voltage control, and multiphase RF clocking correct AM-AM and AM-PM nonlinearities to achieve -40dBc ACPR and -31dB EVM for a 40MHz 64-QAM signal with a peak PAE of 28.8%.
- In Paper 17.6, the Massachusetts Institute of Technology describes a rapid and energy-efficient molecular sensing 220-to-320GHz spectrometer in 65nm CMOS. Dual THz combs produce 5.2mW radiated power and have a noise figure of 14.6 to 19.5dB.
- In Paper 17.7, Georgia Institute of Technology presents a transmitter and a coherent receiver for full-band mm-wave hyperspectral imaging, flip-chip integrated with wideband Vivaldi antennas. A distributed quadrupler has +/-2dB P_{out} variation over 90 to 300GHz. The sub-harmonic receiver reaches -115dBm sensitivity and operates over 115 to 325GHz.
- In Paper 17.8, Stanford University, University of Nice, STMicroelectronics, Instituto de Telecomunicações, ISCTE-IUL, and University of Lisbon demonstrate a 130GHz point-to-point wireless system. Fully packaged silicon ICs integrated with a 3D printed antenna, a 5m wireless link is established with 32dBm EIRP, 12.5Gb/s with BER $<10^{-6}$, and energy efficiency of <8pJ/b.
- In Paper 17.9, Hiroshima University, NICT, and Panasonic Corporation describe a transmitter in 40nm CMOS operating at 300GHz. Introducing an image/LO suppression technique, it demonstrates a 105Gb/s data-rate over a single 32-QAM channel.
- In Paper 17.10, University of California, Davis, presents a 318-to-370GHz 2D phased array in 0.13µm BiCMOS. Adding a travelling wave to a standing wave radiator allows beam steering over 128°/53° in the E/H planes, independent from the 15.1% frequency tuning.

Session 17 Highlights: TX and RX Building Blocks

[17.1] A Digitally Assisted CMOS WiFi 802.11ac/11ax Front-End Module Achieving 12% PA Efficiency at 20dBm Output Power with 160MHz 256-QAM OFDM Signal

[17.5] An Intrinsically Linear Wideband Digital Polar PA Featuring AM-AM and AM-PM Corrections Through Nonlinear Sizing, Overdrive-Voltage Control, and Multiphase RF Clocking

[17.8] A Compact 130GHz Fully Packaged Point-to-Point Wireless System with 3D-Printed 26dBi Lens Antenna Achieving 12.5Gb/s at 1.55pJ/b/m

Paper 17.1 Authors: *Y H Chee[1], F Goluk[1], T Matsuura[1], C Beale[2], J F Wang[1], O Shanaa[1]*

Paper 17.1 Affiliation: *MediaTek, [1]San Jose, CA USA, [2]MediaTek, Kent, United Kingdom*

Paper 17.5 Authors: *M Hashemi[1], Y Shen[1], M Mehrpoo[1], M Acar[2], R van Leuken[1], M S Alavi[1], L de Vreede[1]*

Paper 17.5 Affiliation: *[1]Delft University of Technology, Delft, The Netherlands ; [2]Ampleon, Nijmegen, The Netherlands*

Paper 17.8 Authors: *N Dolatsha[1], B Grave[1], M Sawabi[1], C Chen[1], A Babveyh[1], S Kananian[1], A Bisognin[2], C Luxey[2], F Gianesello[3], J Costa[4], C Fernandes[4], A Arbabian[1]*

Paper 17.8 Affiliation: *[1]Stanford University, Stanford, CA, [2]University of Nice, Sophia Antipolis, France, [3]STMicroelectronics, Crolles, France, [4]University of Lisbon, Lisbon, Portugal*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF*

CONTEXT AND STATE OF THE ART

- The trend towards more spectrally efficient communication for WiFi, LTE, and 5G is generally contradictory to stringent power requirements and high integration levels. Digital predistortion can be used with efficient nonlinear PAs but is typically not extended to front-end modules implemented in III-V technologies.
- In mm-wave frequencies, wide bandwidths are readily available but communication links are often over very short distances (<10cm), consuming high power (100s pJ/b), and/or requiring large reflectors.

TECHNICAL HIGHLIGHTS

First digitally assisted front-end module for WiFi with record 12% PAE at +20dBm output power for 160MHz 802.11ac

- In Paper 17.1, MediaTek describes a digitally assisted CMOS WiFi 802.11ac/11ax front-end module. The TX path delivers 20dBm of output power with -35dB EVM and 12%/10% PAE. The RX path achieves 2.6dB NF and 12.5dB gain with 9mA from a 2.5V supply.

Pre-distortion-less polar PA with internal nonlinearity compensation.

- In Paper 17.5, Delft University of Technology and Ampleon show a wideband, intrinsically linear digital PA. Nonlinear sizing, overdrive-voltage control, and multiphase RF clocking correct AM-AM and AM-PM nonlinearities to achieve -40dBc ACPR and -31dB EVM for a 40MHz 64-QAM signal with a peak PAE of 28.8%.

Energy-efficient 5m 12.5Gb/s link at 130GHz

- In Paper 17.8, Stanford University, University of Nice, STMicroelectronics, Instituto de Telecomunicações, ISCTE-IUL, and University of Lisbon demonstrate a 130GHz point-to-point wireless system. Fully packaged silicon ICs integrated with a 3D printed antenna, a 5m wireless link is established with 32dBm EIRP, 12.5Gb/s with BER $<10^{-6}$, and energy efficiency <8pJ/b.

APPLICATIONS AND ECONOMIC IMPACT

- As CMOS technology scales, digitally assisted techniques become increasingly valuable in improving performance and energy efficiency. By using a polar PA or extending predistortion to the front-end module, PA efficiency can be significantly improved, saving power and extending battery life in mobile applications.
- Due to the large available bandwidth at mm-wave frequencies, multi-Gb/s chip-to-chip links can break traditional backplane limitations in datacenters and allow unprecedented connection speeds for interactive kiosks. For these to be practical, extended range is critical while achieving energy efficiencies similar to wired connections.

Session 18 Overview: Full Duplex Wireless Front-Ends

Wireless Subcommittee

Session Chair: *Alyosha Molnar, Cornell University, Ithaca, NY*

Session Co-Chair: *Jan Craninckx, IMEC, Leuven, Belgium*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Espoo, Finland, Wireless*

Same-channel full-duplex wireless systems attempt to transmit and receive RF signals at the same frequency and at the same time. This requires specialized techniques in the radio front-end to suppress the transmit signal and associated artifacts so that it does not saturate the receiver. Here three distinct approaches are presented covering communication and radar signals.

- In Paper 18.1, the University of Washington describes a 40nm CMOS integrated transceiver front-end employing a pair of cancelation paths at RF and analog baseband to suppress TX leakage in the receiver. The duplexing transceiver achieves more than 50dB of cancellation across 42MHz of bandwidth while consuming only 3.5mW of additional power.
- In Paper 18.2, Columbia University demonstrates a 65nm CMOS integrated linear-time-varying circulator-receiver combination that employs an on-chip network to adjust for mismatched antenna port impedance. It achieves 40dB of TX suppression across 20MHz with a single antenna port, and +30dBm TX-to-RX IIP3.
- In Paper 18.3, National Tsinghua University presents a 65nm CMOS FMCW radar front-end where the transmit, receive and duplex functionality are combined thru a single antenna port with a switched PA/mixer. It achieves 10dBm output power and 18dB RX NF at 10GHz enabling 37.4cm resolution, and range up to 50 meters.

Session 18 Highlights: Full-Duplex Wireless Front-Ends

[18.1] A 1.7-to-2.2 GHz Full-Duplex Transceiver System with >50dB Self-Interference Cancellation over 42MHz Bandwidth

Paper Authors: *Tong Zhang, Ali Najafi, Chenxin Su, Jacques Christophe Rudell*

Paper Affiliation: *University of Washington, Seattle, WA*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Finland, Wireless*

CONTEXT AND STATE OF THE ART

- Full-duplex wireless communication is an important candidate for increasing RF spectrum capacity required in 5G. It poses many challenges on transceiver design, as the strong transmitted signal swamps the weak receiver signal.
- Existing solutions typically have low integration levels, or achieve insufficient isolation across a wide enough band to allow useful functionality.

TECHNICAL HIGHLIGHTS

Full Duplex Transceiver Achieves 50dB isolation across 40MHz bandwidth

- The techniques described in the paper provide high isolation with a very small impact on power consumption and basic performance, making it possible for this approach to replace existing radios.

APPLICATIONS AND ECONOMIC IMPACT

- Full-duplex wireless enables to re-use the very expensive licensed spectrum in two-way communications, effectively doubling the data rate and the cell capacity. It is a candidate for standardization in future 5G radio systems.
- Full-duplex also enables a number of protocol-level enhancements, avoiding many types of interference, and so enhancing network reliability.

Session 19 Overview: Frequency Generation

RF Subcommittee

Session Chair: *Andrea Mazzanti, University of Pavia, Italy*

Session Co-Chair: *Xiang Gao, Credo Semiconductor, CA*

Subcommittee Chair: *Piet Wambacq imec, Belgium, RF*

This session covers the latest advancements in frequency sources and synthesis, fundamental blocks for communication, sensing and imaging systems. The first presentation in the session demonstrates a high-efficiency, high-power multiport radiating element at 114GHz in a SiGe BiCMOS technology. The second paper proposes an efficient calibration technique applied to a 27-to-31GHz injection-locking frequency multiplier with quadrature outputs. The next three presentations discuss frequency synthesizers. The first is a digital 50-to-66GHz PLL featuring low noise and low spur levels by leveraging a high-speed TDC and intensive calibrations. The second and third PLLs are based on ring-oscillators and leverage subsampling phase detection and FIR filtering, respectively, to achieve simultaneously low noise and compact area. The session is concluded with an ultra-low-voltage DCO in a 16nm FinFET technology.

- In Paper 19.1, University of California, Irvine, introduces a high-efficiency high-power multiport radiating element at 114GHz, which can concurrently perform as a resonator, a power combiner, and a radiator. The SiGe BiCMOS design achieves 14dBm EIRP, -99.3dBc/Hz phase noise at 1MHz offset, and DC-to-EIRP and DC-to-RF efficiencies of 5% and 3.6%, respectively.
- In Paper 19.2, Ulsan National Institute of Science and Technology presents a low-phase-noise mm-wave injection-locked frequency multiplier (ILFM) using an ultra-low-power frequency-tracking loop. The ILFM generates a frequency between 27 and 30GHz and the calibration loop, which only requires 600μW, limits phase-noise variation to 2dB up to 100MHz offset over 0.5-to-1.35V supply and 20°C-to-100°C temperature variations.
- In Paper 19.3, Carnegie Mellon University shows a low-phase-noise mm-wave all-digital fractional PLL. The PLL is made of a 50-to-66GHz capacitively degenerated DCO and a f_{DCO}/4-input-frequency TDC with a 450fs resolution. Extensive digital calibration reduces spurs to -59dBc levels and jitter to 220fs.
- In Paper 19.4, Columbia University presents a sub-sampling PLL with a time-based loop filter. The 2.3GHz PLL achieves $0.72ps_{rms}$ integrated jitter with 4.5mW power consumption while occupying only 45μm×110μm.
- In Paper 19.5, University of California, Los Angeles, introduces a 34-tap FIR filter and XOR phase detectors to suppress $\Delta\Sigma$ noise and enable wide PLL bandwidth while achieving low jitter. The ring oscillator based on a 45nm CMOS synthesizer design achieves $1.5ps_{rms}$ jitter with 10mW power while using large bandwidth of $0.25f_{REF}$.
- In Paper 19.6, TSMC and University College Dublin propose an ultra-low voltage DCO in 16nm FinFET CMOS. Based on a trifilar-coil topology the oscillator supply can be reduced to 0.2V while operating over a 3.2-to-4.0GHz frequency range with a -188dBc/Hz phase-noise figure of merit.

Session 19 Highlights: Frequency Generation

[19.6] A 0.2V Trifilar-Coil DCO with an Energy-Harvesting DC-DC Converter in 16nm FinFET CMOS with 188dB FOM, 1.3kHz Resolution, and Frequency Pushing of 38MHz/V

Paper 19.6 Authors: *Chao-Chieh Li[1], Min-Shueh Yuan[1], Chih-Hsien Chang[1], Yu-Tso Lin[1], Kenny Hsieh[1], Mark Chen[1], Robert Bogdan Staszewski[2]*

Paper 19.6 Affiliation: *[1]TSMC, [2]University College Dublin*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF*

CONTEXT AND STATE OF THE ART

- Energy harvesting is a topic of intensive research promising battery-free operation of massive networks of wireless IoT devices. Ultra-low voltage and ultra-low power consumption are key design requirements, particularly challenging for oscillators and frequency sources.
- Previously reported silicon LC oscillators operate at voltages as low as 0.35V with a limited frequency-tuning range and being sensitive to supply variation.

TECHNICAL HIGHLIGHTS

First RF oscillator operating with voltage supply of 0.2V with a competitive tuning range and phase-noise figure of merit.

- In Paper 19.6, TSMC and University College Dublin propose an ultra-low voltage DCO in 16nm FinFET CMOS. Based on a trifilar-coil topology the oscillator supply can be reduced to 0.2V while the oscillator operates over a 3.2-to-4.0GHz frequency range with a -188dBc/Hz phase-noise figure of merit.

APPLICATIONS AND ECONOMIC IMPACT

- This low voltage VCO paves the way for energy harvesting and battery-less radios for IoT devices.

Session 20 Overview: Digital Voltage Regulators and Low Power Techniques

Digital Circuit Techniques Subcommittee

Session Chair: *Atsuki Inoue, Fujitsu Labs, Kawasaki, Japan*

Session Co-Chair: *Dennis Sylvester, University of Michigan, Ann Arbor*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits Subcommittee*

Integrated voltage regulation using digital-oriented design techniques is a growing area. Papers in this session focus on various approaches to digital voltage regulation and power management techniques, including one fully integrated buck converter with an on-die solenoid with a planar magnetic core, four digital low dropout (LDO) regulators, and one switched-capacitor DC-DC converter with dual outputs. The last paper in this session touches on a new ultra-low power adiabatic design style targeting signal processing for hearing aids. Taken together, these papers reflect today's major trends in digital power management for SoCs and microprocessors.

- In Paper 20.1, Intel describes a fully integrated digitally controlled 2-phase buck voltage regulator with on-die solenoid inductors with a planar magnetic core in 14nm tri-gate CMOS. The technology-circuit co-optimization enables ultra-thin packages, and the voltage regulator offers 1A/mm^2 power density with peak efficiency of 84% and utilizes a digital pulse width modulation scheme with 8ps resolution. Including inductor, the regulator occupies 0.4mm^2.
- In Paper 20.2, National Chiao Tung University presents a digital LDO that improves load regulation and output ripple voltage in the presence of PVT variations. The proposed DLDO occupies 0.193mm^2 in 40nm and achieves less than 3mV output ripple across 0°C to 80°C and output voltage from 0.6V to 1V, and the transient response time is 1.3μs for a load step from 1mA to 201mA.
- In Paper 20.3, University of California, San Diego describes a new recursive LDO that dramatically improves response time and load regulation range using a SAR-like binary search algorithm in its coarse loop. The 65nm design specifically achieves 15.1ns and 100ns response and settling times, respectively, while maintaining 5.6mV/mA load regulation and loop stability across a 20,000× dynamic load range.
- In Paper 20.4, University of Macau presents an analog-assisted digital LDO that focuses on achieving fast transient response, low power, and output capacitor size reduction. A high-pass filter is used in addition to conventional coarse and fine loops to improve output voltage regulation under fast load current steps. Undershoot of 105mV with a 10mA/1ns load step is achieved.
- In Paper 20.5, University of Macau describes a dual-output switched-capacitor DC-DC converter that is capable of dynamically reconfiguring the amount of flying capacitance to each output based on load demands in order to fully utilize the converter area. Cross regulation is maintained by ensuring each reconfigurable converter unit cell is fully allocated to only one output. This approach improves efficiency by 4.8%, and the converter achieves 83.3% peak efficiency at 100mA load.
- In Paper 20.6, Columbia University presents an event-driven LDO that significantly reduces the output capacitor size, while supporting higher load current compared to a recently presented event-driven LDO. The design reduces feedback latency using fine-grained parallelism in the PI controller, and achieves 99.2% peak current efficiency and <7.6% output voltage change for 1.44mA load change with 0.1nF output capacitance.
- In Paper 20.7, University of Michigan describes a 13.8μW filter bank targeting hearing aid applications and using adiabatic logic. The authors employ a new circuit technique to eliminate short-circuit current in 4-phase adiabatic logic. The 65nm test chip operates at 1.75MHz and offers 9.7× power reduction per input compared to prior work in the digital domain.

Session 20 Highlights: Digital Voltage Regulators and Low Power Techniques

[20.1] A Digitally Controlled Fully Integrated Voltage Regulator with On-Die Solenoid Inductor with Planar Magnetic Core in 14nm Tri-Gate CMOS

Paper Authors: H. K. Krishnamurty, V. Vaidya, S. Weng, K. Ravichandran, P. Kumar, S. Kim, R. Jain, G. Matthew, J. Tshanz, V. De

Paper Affiliation: *Intel, Hillsboro, OR*

Subcommittee Chair: *Edith Beigné, CEA-LETI, Grenoble, France, Digital Circuits*

CONTEXT AND STATE OF THE ART

- Intelligent power management is promising to reduce energy consumption and is realized by integrating the power management unit on the same die. Large power fluctuations require fast response time of on-die power delivery circuits, as well as high energy density and efficiency.

TECHNICAL HIGHLIGHTS

Intel demonstrates a fully integrated digitally controlled buck voltage regulator with on-die solenoid inductors with a planar magnetic core on 14nm tri-gate CMOS.

- The technology-circuit co-optimization enables ultra-thin packages, and the voltage regulator offers 1A/mm^2 power density with peak efficiency of 84% at 100MHz switching frequency and utilizes a digital pulse width modulation scheme with 8ps resolution. Including the inductor, the regulator occupies 0.42mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- For coming IoE era, intelligent sensors, smart cards and medical equipment will greatly impact our quality of life and the overall market for such devices is expected to grow. These devices require even lower power with smaller form factors, necessitating intelligent power management. Integrated power management for mobile processors will lower the cost of mobile phones.

Session 21 Overview: Smart SoCs for Innovative Applications

Technology Directions Subcommittee

Session Chair: *Antoine Dupret, CEA-Tech, France*

Session Co-Chair: *Pui-In Mak, University of Macau, China*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

While System on Chips (SoC) are common in the consumer electronics market, smart SoCs now emerge to enable more demanding applications, from biomedical sensors to security. In this Technology Directions session we showcase the high sensitivity, large dynamic range, energy efficiency and security issues that must be addressed to make possible the widespread uptake of these technologies. The session consists of 8 papers, including the demonstration of SoCs for bacterial sensing, 3D lung ventilation or intra-ocular pressure monitoring, piezoelectric drivers for diverse applications, mixed signal processing for acoustic sensing, and a secure actively detuned wireless power receiver.

- In Paper 21.1, MIT describes a nanowatt-level circuit interface for bioluminescence readout from bacterial sensors. The system achieves 600nJ/conversion from external NPN phototransistors with an effective photon noise flux of 5.3×10^5ph/mm^2. The system can successfully detect bacteria engineered for heavy-metal sensing using a 15µL sample.
- In Paper 21.2, KAIST describes a 3D electrical impedance tomography (EIT) System for lung ventilation monitoring. It features an active electrode system with dedicated calibration and communication, a 1.3MΩ output impedance current stimulator, and a 94dB DR impedance spectroscopy frontend that enables both time-difference EIT and frequency-difference EIT. The 3D EIT can detect a volume change with better than 90% accuracy.
- In Paper 21.3, Purdue University describes a sub-mm^3, wireless, implantable intraocular pressure monitor micro-system (IMM) that comprises a powering coil, an antenna, a piezoresistive MEMS pressure sensor and a pressure sensing IC. The IMM volume is limited to 0.38mm^3 for the studies on rodents. A cavity resonator magnetic coupling delivers wireless power with 4.89% efficiency. The IMM achieves 0.67mmHg pressure sensitivity with differential resistance sensing.
- In Paper 21.4, Texas A&M University presents a controller for an electric scalpel system with a reduced-order sliding mode control. To ensure that the transducer always operates around 55.5kHz even under heavy load conditions, the unwanted non-longitudinal resonant modes are prevented by a PLL-based frequency discriminator with intervention and release logic. The circuit achieves fast and reliable responses for large signal load variations and power mode charging with a buildup time of 9.2ms.
- In Paper 21.5, Harvard University describes a driver able to generate high-voltage (100Vpp) analog waveforms from a low voltage (3-to-5V) efficiently for piezoelectric actuators. The driver dissipates 32.47mW to drive a piezo haptic actuator at f = 150Hz, Vin = 3.6V, Vout = 100Vpp C_L = 94nF with 0.33% THD+N. This corresponds to a 10.82x reduction in power and a 3.4x reduction in THD+N compared to previous similar-size solutions.
- In Paper 21.6, University of Michigan, Ann Arbor presents an ultra-low power acoustic sensing and object recognition microsystems for IoT applications. An ultra-low power 8b SAR-ADC with 50fF input capacitance enables a frontend amplifier with nW-level power consumption. A serialized discrete Fourier transform feature extraction is performed in a digital back-end, replacing a high-power/area-consuming conventional FFT. The overall system consumes 12nW while successfully identifying the target objects with better than 95% accuracy.
- In Paper 21.7, University of California San Diego, describes a flexible mixed-signal 8x8 linear transform processor for spatial filtering operating over 2.4MHz using a new nested thermometer two-stage capacitive array multiplying DAC with 14b resolution. Measurements demonstrate 84dB spatial separation over a wide range of incident angles and incident interferer power. With an active area of 1.7mm^2 in 65nm CMOS, the processor consumes 2pJ per 14b mixed-signal multiply-accumulate operation.
- In Paper 21.8, MIT describes a 0.18µm CMOS wireless charging receiver, with an active detuning mechanism that does not use passive components being switched. Detuning is first combined with an on-chip 0.77J/ECSM Elliptic Curve accelerator and in-band telemetry to protect against counterfeit chargers, with up to 16× rejection of received power. Second, equitable power distribution between 2 receivers coupled to the same charger is demonstrated overcoming a 4:1 distance asymmetry.

Session 21 Highlights: Smart SoCs for Innovative Applications

[21.2] A 1.4mΩ Sensitivity 94dB Dynamic Range Electrical Impedance Tomography SoC and 48-Channel Hub SoC for 3D Lung Ventilation Monitoring System

Paper Authors: *M. Kim, H. Kim, J. Jang, J. Lee, J. Lee, J. Lee, K. Lee, K. Kim, Y. Lee, H.-J. Yoo*

Paper Affiliation: KAIST, Daejeon, Korea

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Real-time lung ventilation monitoring without large equipment and eventually migration of the point of care onto the body itself is important. Integrated electrical impedance tomography (EIT) solutions dedicated to monitor 2D cross-sectional lung image with limited spatial information have been demonstrated. This work, for the first time, demonstrates a robust implementation of an EIT system for 3D monitoring of lung ventilation with high spatial resolution in real-time.

TECHNICAL HIGHLIGHTS

- A compact wearable system that consists of 3 wearable belts integrated into a chest vest with a Hub-SoC supporting up to 48 active electrodes has been demonstrated.
- The system features 3D EIT with 94dB dynamic range and 1.4mΩ resolution. By including a COTS Bluetooth module into the system, it provides a seamless wireless connection to an external imaging system for 3D lung image reconstruction in real time.

APPLICATIONS AND ECONOMIC IMPACT

- Wearable and wireless physiological signals acquisition and monitoring systems capable of measuring multi-dimensional bioelectrical impedance have a large market opportunity.
- This system increases the patient's autonomy and reduces healthcare costs significantly by facilitating cloud-based remote patient monitoring.

Session 21 Highlights: Smart SoCs for Innovative Applications

[21.6] A 12nW Always-On Acoustic Sensing and Object Recognition Microsystem using Frequency-Domain Feature Extraction and SVM Classification

Paper Authors: S. Jeong, Y. Chen, T. Jang, J. Tsai, D. Blaauw, H-S. Kim, D. Sylvester

Paper Affiliation: University of Michigan, Ann Arbor, MI, United States

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Intelligence and context awareness is becoming increasingly important for IoT devices even as power consumption remains one of the biggest challenges for such devices. Extracting information from visual data is computationally intensive.
- In this paper, acoustic sensing is shown to be an alternate modality to extract real-time information while maintaining extremely low power operation.

TECHNICAL HIGHLIGHTS

- An acoustic sensing system that includes a MEMS-based microphone, SAR ADC, DFT-based feature extraction and a power-efficient classification system has been built. The 12nW a system-on-chip in 0.18μm CMOS achieves >95% successful identification of target objects in a real environment.

APPLICATIONS AND ECONOMIC IMPACT

- An always-on acoustic sensing system is demonstrated here that enables continuous and long-term monitoring e.g., in agriculture, to detect pests or precipitation, in infrastructure health tracking, or in security/safety monitoring. This system-in-package (SiP) solution can last more than 10 years on a button cell battery.

Session 22 Overview: Harvesting and Wireless Power

Analog Subcommittee

Session Chair: *Stefano Stanzione, Holst Center; The Netherlands*

Session Co-Chair: *Edgar Sanchez-Sinencio; Texas A&M University, College Station, TX*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX, Analog*

Innovation in energy harvesting continues to expand the capability to extract power from the environment through temperature differences, vibration, and solar radiation. New design methodologies for wireless power transfer and LED visible-light communication are moving the state of the art.

- In Paper 22.1, the University of Southampton describes a self-tuning large-signal antenna driver for inductively coupled systems. Resonance is achieved by using synchronous switching of a fractional capacitance employing quadrature symmetric timing. The driver is fabricated in 0.18µm HV 20v CMOS.
- In Paper 22.2, the University of Macau presents a fully integrated flipping capacitor rectifier for piezoelectric energy harvesting. The chip, fabricated in 0.18µm CMOS, extracts nearly 5x more power than an ideal full-bridge rectifier.
- In Paper 22.3, Pennsylvania State University introduces a power management IC capable of operating in either voltage or current mode, depending on the input voltage amplitude. The chip, fabricated in 0.35µm CMOS, allows to extend the inductive range and allowable receiver coil orientation by 125% and 150% respectively.
- In Paper 22.4, the University of Macau describes a 0.35µm CMOS reconfigurable bidirectional wireless power transceiver for allowing mobile phones to charge each other without additional hardware. A 58.6% battery-to-battery efficiency is measured with two identical coils and chips.
- In Paper 22.5, the University of Texas at Dallas introduces an irradiance-aware auto-reconfigurable MPPT-based photovoltaic energy harvesting IC in 0.35µm CMOS. The system reduces MPPT transient time by 86× with respect to previous works, while reaching peak power efficiency of 93%.
- In Paper 22.6, the University of Michigan presents a fully-integrated 0.18µm CMOS counter-flow energy reservoir that allows efficient energy extraction from the storage capacitors as a high intensity power supply. Integration with a radio demonstrates nearly 12× longer continuous RF transmission.
- In Paper 22.7, the University of California, Los Angeles describes an inductively-coupled wireless power transfer circuit that is immune to significant distance and load variations. The 0.18µm chip delivers power up to 4.2cm and handles 10× load change, with peak efficiency of 74% and 20mW max. power.
- In Paper 22.8, the Hong Kong University of Science and Technology introduces an AC-input inductorless LED driver for visible-light-communication applications. The 0.35µm 20V CMOS driver does not have passive component speed limitations and mitigates the harmful low-frequency-flicker to below 10%.

Session 22 Highlights: Harvesting and Wireless Power

[22.2] A 1.7mm² Inductorless Fully Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power Extraction Enhancement

Paper Authors: *Man-Kay Law, Pui-in Mak*

Paper Affiliation: *University of Macau, Macau, China*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX, Analog*

CONTEXT AND STATE OF THE ART

- Harvesting energy from the environment can allow reduced use of batteries or extend their lifetime.
- Especially in biomedical implantable applications, the energy harvesting system needs to be small form with an efficient power management unit.

TECHNICAL HIGHLIGHTS

A 1.7mm² Inductorless Fully Integrated Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting with 483% Power Extraction Enhancement

- First inductorless and fully integrated piezoelectric harvester interface
- It extracts up to 4.3x more power than an ideal full-bridge rectifier.

APPLICATIONS AND ECONOMIC IMPACT

- Minimizing form factor and increased integration are important for reduced impact for implanted biomedical sensors.
- Harvesting mechanical vibrations is a promising technique to extend their battery life.

Session 23 Overview: DRAM, MRAM, and DRAM Interfaces

Memory Subcommittee

Session Chair: *Takefumi Yoshikawa, National Institute of Technology, Nagano College, Nagano, Japan*

Session Co-Chair: *Seung-Jun Bae, Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Dynamic memories are at the heart of every computing system. Improvements in the memory sub-system are therefore directly impacting user experience – battery-powered systems operate longer, graphics are crisper and our phones will simply react more smoothly.
In this session, multiple new developments will be presented. The graphics interface GDDR5X enables a jump in performance for discrete-component graphics while the low-power interface LPDDR4X promises high bandwidth and low power – implemented both on the DRAM and on the controller side. MRAM is another viable low-power alternative since it does not require memory refreshes, which can only be minimized in LPDDR4 or LPDDR4X. The session will give a further outlook into alternate high-speed interfaces and the application of a low-latency specialty-DRAM as a CPU cache.

- In Paper 23.1, Micron presents a graphics-DRAM at a data-rate of 12Gb/s. Multiple high-speed circuit techniques for DRAM processes are discussed. The chip implements a CML-PLL-based clock generator, a two-stage RX with a gain-regulated amplifier and DFE, and an asymmetric de-emphasis transmitter to achieve the target data-rate.
- In Paper 23.2, Samsung presents an 8Gb 5Gb/s LPDDR4X with LVSTL of 0.6V V_{DDQ} at a swing of 0.3V. To compensate noise caused by the small swing, the timing margin is improved by de-skewing pseudo differential clocks and DQS equalizer. By adopting a split-die architecture, the die yield is improved.
- In Paper 23.3, SK Hynix presents a 2Gb 4.8Gb/s LPDDR4 with on-chip ECC. A sub-100μA self-refresh current is achieved by extending the refresh period and by turning off regulators and references periodically in standby mode. Cell screen and repair considering ECC are addressed.
- In Paper 23.4, Samsung presents a 2Gb 1V 3.733Gb/s LPDDR4 for wearable devices. The standby power of 0.15mW is 66% lower than conventional LPDDR4. It is achieved by ECC, aggressive power gating in deep-power-mode, temperature controlled regulators and increased gate length.
- In Paper 23.5, SK Hynix and Toshiba present a 4Gb STT-MRAM chip featuring the highest integration density of 0.0026mm^2 per Mb realized by a hierarchical bit line architecture. An LPDDR2-compatible interface achieving a 2.5ns clock cycle is implemented.
- In Paper 23.6, Samsung presents an LPDDR4X interface for a memory controller achieving 4.266Gb/s/pin on a 10nm logic process. Stability against tDQSCK variation is guaranteed by an automatic tracking of the memory-DQS without incurring any black-out penalty. Write-window is maximized by V_{REF} training.
- In Paper 23.7, Pohang University and Samsung Electronics present a power-efficient equalizing scheme for a single-ended DRAM interface by a voltage-to-time conversion technique. 0.46pJ/bit at 12Gb/s/pin with 13dB loss has been achieved in a 0.8V single power supply on a 65nm CMOS process.
- In Paper 23.8, Yonsei University and SK Hynix show a unique possibility to adopt an encoding scheme to boost data bandwidth. A 15.6Gb/s data rate with 7.8mW power consumption, which is a 2.9× improvement of the figure of merit over conventional LPDDR interfaces, has been achieved in a 65nm CMOS process.
- In Paper 23.9, Piecemakers Technologies, ITRI and Intel are presenting an 8-channel 4.5Gb 180GB/s low latency DRAM for cache applications. High performance while maintaining a reasonable die size is achieved by sharing address-decoding circuits as much as possible.

Session 23 Highlights: DRAM, MRAM, and DRAM Interfaces

[23.1] An 8Gb 12Gb/s/pin GDDR5X DRAM for Cost-Effective, High-Performance Applications

Paper 23.1 Authors: *Martin Brox[1], Mani Balakrishnan[1], Martin Broschwitz[1], Cristian Chetreanu[1], Stefan Dietrich[1], Fabien Funfrock[1], Marcos Alvarez Gonzalez[1], Thomas Hein[1], Eugen Huber[1], Daniel Lauber[1], Milena Ivanov[1], Maksim Kuzmenka[1], Chris Mohr[2], Francisco Emiliano Munoz[1], Juan Ocon Garrido[1], Swetha Padaraju[1], Sven Piatkowski[1], Jan Pottgiesser[1], Peter Pfefferl[1], Manfred Plan[1], Jens Polney[1], Stefan Rau[1], Michael Richter[1], Ronny Schneider[1], Ralf Oliver Seitter[1], Wolfgang Spirkl[1], Marc Walter[1], Jörg Weller[1], Filippo Vitale[1]*

Paper 23.1 Affiliation: *[1]Micron, Munich, Germany and [2]Micron, Allen, TX*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- DRAM bandwidth is critical for today's computer systems ranging from high-performance computing to mobile smartphones and graphics, particularly due to growth in emerging applications such as virtual reality and artificial intelligence.

TECHNICAL HIGHLIGHTS

Micron introduces the fastest graphics DRAM, GDDR5X for VR, AI, and future game console applications

- Paper 23.1 introduces a graphics DRAM operating at a data-rate of 12Gb/s/pin, which surpasses the fastest published GDDR5 (ISSCC 2016) by 33%. It adopts advanced interface techniques, including CML-PLL-controlled clock generation with on-die frequency doubling, one-tap gain and common-mode-regulated DFE RX, and an asymmetric de-emphasis TX.

APPLICATIONS AND ECONOMIC IMPACT

- Recently, high-performance applications such as next generation gaming, VR, and AI require over 1TB/s memory bandwidth. Currently, only high cost HBM (high bandwidth memory) can meet this requirement, but GDDR5X is a new low-cost option with standard packaging that reaches to over 10Gb/s data rates.

Session 23 Highlights: DRAM, MRAM, and DRAM Interfaces

[23.5] A 4Gb LPDDR2 STT-MRAM with Compact 9F2 1T1MTJ Cell and Hierarchical Bit Line Architecture

Paper 23.5 Authors: *Kwangmyoung Rho[1], Kenji Tsuchida[2], Dongkeun Kim[3], Yutaka Shirai[2], Jihyae Bae[1], Tsuneo Inaba[2], Hiromi Noro[2], Hyunin Moon[1], Sungwoong Chung[1], Kazumasa Sunouchi[2], Jinwon Park[1], Kiseon Park[1], Akihito Yamamoto[2], Seoungju Chung[1], Hyeongon Kim[1], Hisato Oyamatsu[2], Jonghoon Oh[1]*

Paper 23.5 Affiliation: *[1]SK Hynix Semiconductor, Incheon, Korea, [2]Toshiba Korea Corporation, Seoul, Korea, [3]SK hynix Semiconductor, Icheon, Korea,*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- STT-MRAM is one of the most promising emerging memory technologies.
- DRAM refresh current is a key barrier to ultra-low-standby-power devices.
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TECHNICAL HIGHLIGHTS

SK Hynix and Toshiba demonstrate a 4Gb STT-MRAM, the highest integration reported to date

- In Paper 23.5, SK Hynix and Toshiba present a 4Gb STT-MRAM chip featuring the highest integration density of 0.0026mm^2 per Mb realized by a hierarchical bit line architecture. An LPDDR2-compatible interface achieving a 2.5ns clock cycle is implemented.

APPLICATIONS AND ECONOMIC IMPACT

- The highest density STT-MRAM with an LPDDR2-compatible DRAM interface is demonstrated. This technology with innovative circuit techniques can enable ultra low standby power in IoT applications to serve as an ultimate non-volatile memory solution.

Session 24 Overview: Wireless Receivers and Synthesizers

Wireless Subcommittee

Session Chair: *Chun-Huat Heng, National University of Singapore, Singapore*
Session Co-Chair: *Ken Yamamoto, Sony Semiconductor Solutions, Kanagawa, Japan*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Espoo, Finland, Wireless*

This session describes state-of-the-art wireless receivers and synthesizers, supporting IoT and cellular applications. In this session, three low-power receivers including one 2.4GHz receiver with 3× area reduction, one BLE receiver with 2× power reduction, and one wake-up receiver with nano-Watt level power consumption have been included. There are also three advanced receiver techniques including a 4-element receiver array with analog/RF beamformer, a SAWless LTE radio, and a time-interleaved filter-by-aliasing receiver. The first 14nm synthesizer and a sub-mW dividerless synthesizer will also be reported. Finally, we have a highly-advanced 128-QAM 60GHz transceiver for 802.11ay.

- In Paper 24.1, imec, Delft University of Technology and University College Dublin describe an energy/area efficient 40nm CMOS phase-tracking receiver, achieving 3× smaller area while consuming only 1.55mW from a 0.85V supply.
- In Paper 24.2, Columbia University describes a 65nm CMOS 4-element receiver array that supports analog/RF beamforming. It provides >18dB rejection over >400MHz bandwidth, which leads to +34dBV OIP3.
- In Paper 24.3, the University of Twente and Mediatek report a high-linearity 28nm CMOS N-path-filter-based receiver architecture targeting SAW-Less LTE radio. It achieves +44dBm IIP3, +90dBm IIP2 and +13dBm B_{1dB}.
- In Paper 24.4, the University of Macau and Instituto Superior Tecnico present an ultra-low-voltage 28nm CMOS BLE for energy harvesting applications using micropower manager with ring-VCO-locked charge pumps. It can function at 0.18V while consuming only 382μW and 1.33nW sleep power.
- In Paper 24.5, the University of California, San Diego describes a 0.18μm CMOS OOK-modulated wake-up receiver using a transformer for 25dB passive gain. It achieves -69dBm sensitivity while consuming only 4.5nW.
- In Paper 24.6, the University of California, Los Angeles reported a 65nm CMOS time-interleaved filtering-by-aliasing receiver. It achieves +21dBm IIP3 for offset > 12MHz and >70dB stopband rejection at only 40MHz offset from the carrier frequency.
- In Paper 24.7, IMEC and Rohm Semiconductor present a 40nm CMOS dividerless fractional-N synthesizer using phase-dithering DTC and digital phase unwrap for IoT applications. It achieves 1.98ps rms jitter while consuming only 673μW.
- In Paper 24.8, Samsung Semiconductor and Samsung Electronics present a 14nm fractional-N digital PLL using a TDC chopping technique for cellular application. It attains 0.14ps_{rms} jitter and -78dBc fractional spur.
- In Paper 24.9, the Tokyo Institute of Technology reports an automatically calibrated 65nm CMOS 60GHz transceiver for IEEE802.11ay. The transceiver achieves -26dB EVM and a data-rate of 42.24Gb/s for the world-first 128QAM at 60GHz.

Session 24 Highlights: Wireless Receivers and Synthesizers

[24.8] A 14nm Fractional-N Digital PLL with 0.14 ps rms Jitter and -78dBc Fractional Spur for Cellular RFICs

[24.4] A 0.18V 382μW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS

Paper 24.8 Authors: *C. W. Yao[1], W. F. Loke[1], R. Ni[1], Y. Han[1], H. Li[1], K. Godbole[1], Y. Zuo[1], S. Ko[2], N. Kim[2], S. Han[2], I. Jo[2], J. Lee[2], J. Han[2], D. Kown[2], C. Kim[2], S. Kim[2], S. Son[1], T. Cho[2]*

Paper 24.8 Affiliation: *[1]Samsung Semiconductor, San Jose, CA, [2]Samsung Electronics, Hwaseong, Korea*

Paper 24.4 Authors: *W. H. Yu[1], H. Yi[1], P. I. Mak[1], J. Yin[1], R. P. Martins[1, 2]*

Paper 24.4 Affiliation: *[1]University of Macau, Macau, China, [2]Instituto Superior Tecnico, Lisbon, Portugal*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Finland, Wireless*

CONTEXT AND STATE OF THE ART

- Cellular ICs with carrier aggregation require synthesizers to meet stringent phase noise and spurious tones performance and most solutions in the cellular market have been fabricated in 28/40/65nm CMOS. 14nm CMOS technology now allows high performance fractional-N digital synthesizers to be implemented.
- IoT applications could benefit from self-powered wireless sensor nodes that require a wireless transceiver that can operate using harvested energy.

TECHNICAL HIGHLIGHTS

The first 14nm fractional-N digital synthesizer targeting cellular ICs with carrier aggregation

- The synthesizer in 24.8 meets very stringent performance requirements of cellular ICs with carrier aggregation and usees sophisticated circuit techniques to achieve very good spurious tone and phase noise performance.

A Sub-mW Bluetooth Low-Energy receiver that can be self-powered from the environment

- The BLE receiver in 24.4 includes a sophisticated micropower manager to allow ultra-low-voltage operation and can potentially be powered from the energy harvested from the environment.

APPLICATIONS AND ECONOMIC IMPACT

- A high-performance synthesizer complies with the LTE requirement to meet the ever-growing demands for higher data-rates.
- RF and analog circuits will benefit from the advanced 14nm CMOS technology node that was mainly developed for digital solutions.
- A self-powered wireless BLE receiver could lower the cost of IoT deployment.

Session 25 Overview: GaN Drivers and Galvanic Isolators

Technology Directions Subcommittee

Session Chair: *Shuichi Nagai, Panasonic, Osaka, Japan*

Session Co-Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

Gallium-Nitride (GaN) power devices have garnered a lot of attention for their reduced switching losses leading to small-form-factor high-frequency switching converters. However, issues related to reliable GaN gate driving, signal and power isolation with high common-mode immunity, and reduced electromagnetic interference (EMI) need special attention. This session presents recent advances in EMI-aware gate drivers for GaN devices and galvanic isolators for both signal and power transfer.

- In Paper 25.1, University of Texas at Dallas describes a subharmonic resonant isolated capacitive power transfer (ICPT) system that supplies power wirelessly to sensor interfaces across on-chip capacitive galvanic isolation barrier. The design achieves 4× higher efficiency and 3× higher power delivery compared to the prior art.
- In Paper 25.2, University of Texas at Dallas describes a GaN DC-DC converter for automotive applications that employs spurious noise compression and adaptive tri-slope gate driving schemes. Using these techniques the design is able to reduce the peak spurious noise from 84.73 to 44.23dBμV.
- In Paper 25.3, Reutlingen University presents a GaN gate driver with a fully integrated gate charge buffer capacitor. This gate driver supplies 11nC gate charge without any external buffer capacitor, which is more than 45× improvement as compared to previous designs.
- In Paper 25.4, Texas Instruments demonstrates a 500Mb/s bidirectional, isolated, inductively coupled die-to-die link at 200pJ/b in 0.18μm CMOS. This isolation technique achieves 24kV surge isolation and 50kV/μs common-mode transient noise rejection (CMR) that is 2× higher surge isolation and 2× higher data rate at 33% of the power level of previous designs.

Session 25 Highlights: GaN Drivers and Galvanic Isolators

[25.2] A 10MHz 3V-to-40V V_{IN} Tri-Slope Gate Driving GaN DC-DC Converter with 40.5dBμV Spurious Noise Compression and 79.3% Ringing Suppression for Automotive Applications

Paper Authors: *Xugang Ke[1], Joseph Sankman[2], Yingping Chen[1], Lenian He[3], D. Brian Ma[1]*

Paper Affiliation: *[1]University of Texas at Dallas, Richardson, TX, [2]Texas Instruments, Dallas, TX, [3]Zhejiang University, Hangzhou, China*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Increasing popularity of GaN power converters for high-frequency switching converters with high efficiency.
- Need for robust gate drivers that can switch very fast.
- Need for reduced electromagnetic interference (EMI) noise of the power stage due to high switching frequencies.

TECHNICAL HIGHLIGHTS

- A novel spurious noise compression (SNC) technique to generate randomly distributed frequencies is presented that suppresses EMI noise by 40dBμV and results in eliminating the bulky LC filter in a DC-DC converter.
- This adaptive tri-slope gate driver by detecting the Miller plateau region reduces current spikes and ringing.

APPLICATIONS AND ECONOMIC IMPACT

- Very high frequency switching converters using GaN power transistors.
- Compact power supplies with small form factor.
- Improved power transfer efficiency in automotive, industrial, and offline applications.

Session 26 Overview: Processor Power Management and Clocking

Digital Circuits Subcommittee

Session Chair: *Kathy Wilcox, AMD, Boxborough, MA*
Session Co-Chair: *Youngmin Shin, Samsung, Hwasung, Korea*

Subcommittee Chair: *Edith Beigné, CEA-LETI, Grenoble, France, Digital Circuits*

The first paper in this session considers optimization of computing systems at multiple levels from silicon to data center. A second paper pertains to power delivery network reliability and presents a software approach to mitigating worst-case droop. The remaining three papers deal improving the power of the clock network by making it reconfigurable, use of adiabatic techniques and through adaptive frequency throttling.

- In Paper 26.1, Intel presents an invited paper on highly agile system design to support both highest performance for peak demand and best-in-class performance/W to minimize datacenter operating costs. Silicon and system co-optimization, reliability, and configurability are required to increase performance to meet the computing demands of the modern computing era while driving the total cost of ownership lower.
- In Paper 26.2, IBM demonstrates an RLC network model for processor power delivery and measures the 22nm multicore z13™ processor to analyze worst-case droops called "perfect storms". Compared to the noise associated with synchronous activity on the cores, they create droops that are 1.2× deeper and 1.9× faster. A network of 32 critical-path monitors sense the local droops and initiate activity throttling, improving voltage noise margin to provide 2% increase in chip performance.
- In Paper 26.3, University of Singapore presents a reconfigurable clock network design for operation from sub-threshold to nominal voltage. Clock skew is reduced by up to 2.5 standard deviations and 100mV V_{min} reduction is achieved at 1.8% area penalty in a 40nm LP CMOS FFT testchip.
- In Paper 26.4, University of California, San Diego introduces a fully integrated adiabatic clocking scheme via a switched-capacitor DC-AC multi-level inverter topology. Designed in 45nm SOI, the adiabatic driver is 0.019mm^2 and enables up to 55.6% power savings and features a 200× dynamic frequency range.
- In Paper 26.5, IBM presents a novel adaptive clock strategy for the POWER9™ to reduce the timing margin needed during droop events by embedding analog Voltage Droop Monitors (VDMs) that direct a Digital Phase-Locked Loop (DPLL) to instantly reduce clock frequency in response to a droop. The 14nm implementation can respond in 6ns with 8mV precision with 0.12% area overhead. The quick response time results in 50% noise margin reduction, translating into 8% less power or 3.5% performance gain within the same power envelope.

Session 26 Highlights: Processor Power Management and Clocking

[26.2] Power Supply Noise in a 22nm z13™ Microprocessor

[26.5] Adaptive Clocking in the POWER9™ Processor for Voltage Droop Protection

Paper 26.2 Authors: *P. Chuang[1], C. Vezyrtzis[1], D. Pathak[2], R. Rizzolo[3], T. Webel[4], T. Strach[4], O.Torreiter[4], P. Lobo[5], A. Buyuktosunoglu[1], R. Bertran[1], M. Floyd[6], M. Ware[6], G. Salem[7], S. Carey[3], P. Restle[1]*

Paper 26.2 Affiliation: *[1]IBM Research, Yorktown Heights, NY ; [2]Drexel University, Philadelphia, PA ; [3]IBM Systems, Poughkeepsie, NY ; [4]IBM Systems, Booeblingen, Germany ; [5]IBM Systems, Bangalore, India ; [6]IBM Systems, Austin, TX ; [7]IBM Systems, Burlington, VT*

Paper 26.5 Authors: *M. Floyd[1], P. Restle[2], M. Sperling[3], P. Owczarczyk[3], E. Fluhr[1], J. Friedrich[1], P. Muench[3], P.Chuang[2], C. Vezyrtzis[2]*

Paper 26.5 Affiliation: *[1]IBM Systems, Austin, TX; [2]IBM Research, Yorktown Heights, NY; [3]IBM Systems, Poughkeepsie, NY*

Subcommittee Chair: *Edith Beigné, CEA-LETI, Grenoble, France, Digital Circuits*

CONTEXT AND STATE OF THE ART

- Intelligent power management is required to reduce energy consumption, and accurate power modeling and mitigation techniques enable improved power efficiency in high-performance systems.
- Innovations in adaptive clocking, such as fast response to droop events continue to show better performance gain in systems.

TECHNICAL HIGHLIGHTS

IBM demonstrates accurate power delivery network model confirmed to correlate well with silicon.

- IBM demonstrates an RLC network model for processor power delivery and measures the 22nm multicore z13™ processor to analyze worst-case droops called "perfect storms". Compared to the noise associated with synchronous activity on the cores, they create droops that are 1.2× deeper and 1.9× faster. A network of 32 critical-path monitors sense the local droops and initiate activity throttling, improving voltage noise margin to provide 2% increase in chip performance.

IBM presents a novel adaptive clock strategy with quick response for improved power efficiency and performance.

- A novel adaptive clock strategy is demonstrated by IBM for the POWER9™ to reduce the timing margin needed during droop events by embedding analog Voltage Droop Monitors (VDMs) that direct a Digital Phase-Locked Loop (DPLL) to instantly reduce clock frequency in response to a droop. The 14nm implementation can respond in 6ns with 8mV precision with 0.12% area overhead. The quick response time results in 50% noise margin reduction, which translates into 8% less power or 3.5% performance gain within the same power envelope.

APPLICATIONS AND ECONOMIC IMPACT

- Datacenter operating costs dominated by energy costs are driving the need to co-optimize design to improve performance and lower power in the nanoscale era.
- Robust operation and peak performance for ultra-high-reliable data compute centers is crucial for many business applications, including the health and financial industries.

Session 27 Overview: Biomedical Circuits

IMMD Subcommittee

Session Chair: *Gert Cauwenberghs, University of California, San Diego, CA*

Session Co-Chair: *Michiel Pertijs, Delft University of Technology, Delft, The Netherlands*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

Advances in biomedical circuits and systems are essential technology drivers in addressing critical societal needs to increase the effectiveness and reduce the cost of healthcare. This session highlights the latest circuit innovations that contribute to advances in medical devices, sensing and imaging. For implantable and unobtrusive devices, ultrasonic power delivery and telemetry, and improved neural sensing and stimulation are addressed. Advanced medical sensing increasingly combines multiple modalities in a single device, several examples of which are also featured in this session. Finally, circuit innovations enabling improved ultrasonic and magnetic resonance imaging and optical spectroscopy are presented.

- In Paper 27.1, University of California, Los Angeles, presents a 2.8μW chopper amplifier optimized for neural recording during stimulation in 40nm CMOS. It has an 80mV_{pp} linear-input-range, –76dB harmonic distortion, and 81dB dynamic range, while handling up to 650mV_{pp} common-mode interference.
- In Paper 27.2, KAIST, together with K-Healthwear and Korea University Guro Hospital, demonstrates a combined EEG and Near-Infrared Spectrometry (NIRS) readout, implemented in 65nm CMOS, for continuous quantitative anesthesia depth level monitoring during surgery. The EEG readout achieves an NEF of 3.59 and a LogTIA with a dynamic range up to 60dB is presented for the NIRS readout.
- In Paper 27.3, York University, together with the University of Toronto, GlaxoSmithKline, and Toronto Western Hospital, presents a 64-channel wireless closed-loop neurostimulator with a compact (0.013mm^2/ch) and energy-efficient (630nW/ch) channel architecture that merges both amplification and digitization in a single $\Delta^2\Sigma$-based neural ADC. The design, implemented in 0.13μm CMOS, yields 1.13μV_{rms} IR noise and an NEF of 2.86.
- In Paper 27.4, ETH Zurich presents a fully integrated CMOS receiver for medical MRI that can be placed directly on the coil eliminating any RF cabling. The RX features sub-1dB NF and 0dBm IIP3.
- In Paper 27.5, Stanford University and STMicroelectronics present a 28nm ultrasound receiver for 3D photoacoustic imaging with the front-end and the modulator integrated within a 250×250μm^2 pixel. It achieves 59.9dB SNR with a 7.4× area reduction over comparable prior-art solutions.
- In Paper 27.6, Hitachi presents a 2D array ASIC with 3072 channel analog RX/TX beamformers for volumetric ultrasound imaging. It features 138V_{pp} output capability on 0.09mm^2/ch. The IC is fabricated in 0.18μm HV-CMOS, and the echo imaging consumes 0.7mW/ch.
- In Paper 27.7, Stanford University demonstrates simultaneous ultrasonic wireless power and duplex data communication for implantable applications. It operates at a depth of 8.5cm tissue at a data rate of 95kb/s. The system consumes 405μW, while receiving power and delivering -9dBm to the transmitter.
- In Paper 27.8, Princeton University presents a fully integrated CMOS-based optical spectrometer in a 65nm bulk CMOS process that requires no external optical components. It achieves nearly 10nm resolution and 1.4nm accuracy in peak prediction of continuous-wave excitation in the visible and near-IR range between 500 and 830nm.

Session 27 Highlights: Biomedical Circuits

[27.2] A 25.2mW EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring

Paper Authors: *Unsoo Ha, Jaehyuk Lee, Kwantae Kim, Jihee Lee, Taehwan Roh, Sangsik Choi, and Hoi-Jun Yoo*

Paper Affiliation: *KAIST, Daejeon, Korea; K-Healthwear, Daejeon, Korea; Korea University Guro Hospital, Seoul, Korea*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Monitoring the depth of anesthesia during surgery is critical to safeguard against accidental lapse, which is a major cause of casualties in the operating room.
- Conventional BIS (bispectral) monitoring for depth of anesthesia uses bulky instrumentation that is obtrusive to the patient and the surgical staff, and poses risks in safety and accuracy due to electrical interference and limited sensitivity to certain anesthetic drugs.

TECHNICAL HIGHLIGHTS

- The presented wearable brain-computer interface accurately monitors the depth of anesthesia using non-invasive electroencephalography (EEG), electromyography (EMG), and near-infrared spectroscopy (NIRS) sensors integrated on a strip mounted on the skin.
- KAIST, together with K-Healthwear and Korea University Guro Hospital, demonstrates a combined EEG and Near-Infrared Spectrometry (NIRS) readout, implemented in 65nm CMOS, for continuous quantitative anesthesia depth level monitoring during surgery. The EEG readout achieves an NEF of 3.59 and a LogTIA with a dynamic range up to 60dB is presented for the NIRS readout.

APPLICATIONS AND ECONOMIC IMPACT

- Continuous brain state monitoring is desirable in various clinical settings, including neurological monitoring and cognitive assessment.
- Lowering the cost and increasing the quality of healthcare.

Session 28 Overview: Hybrid ADCs

Data Converter Subcommittee

Session Chair: *Tai-Cheng Lee, National Taiwan University, Taiwan*

Session Co-Chair: *Bob Verbruggen, Xilinx, Dublin*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

Analog-to-digital converters (ADCs) continue to evolve from classical architectures into hybrid converters that combine the strengths of various ADC types. This session demonstrates multiple hybrid ADCs ranging from MHz to GHz bandwidths, employing combinations of SAR, pipeline and oversampling architectures. Pipelined-SAR ADCs utilizing PVT-stabilized dynamic amplifiers, separate comparators per decision and digital amplifiers are disclosed. Noise-shaping phase-domain excess-loop-delay compensation as well as a double noise-shaping quantizer are employed in the ADCs to improve the conversion efficiency.

- In Paper 28.1, MediaTek describes a 5MHz BW noise-shaping SAR ADC with a highly efficient dynamic-amplifier-based FIR-IIR filter. Built in 28nm technology, the ADC consumes only 0.46mW and achieves a peak SNDR of 79.7dB with a Schreier FoM of 180.1dB.
- In Paper 28.2, The University of Florida presents a 4^{th}-order continuous-time delta-sigma modulator, employing a double noise-shaping quantizer, which incorporates both noise-shaped integrating and gated ring oscillator techniques. The prototype in 0.13µm CMOS consumes 11.4mW and exhibits 80.4dB peak SNDR over 15MHz BW.
- In Paper 28.3, MediaTek introduces a phase-domain excess-loop-delay compensation technique using a 128-state segmented rotator in a VCO-based continuous-time delta-sigma modulator to achieve 125MHz BW. Fabricated in 16nm CMOS, this ADC achieves 74.8dB/-80dBc DR/THD with a FOM_w of 67.2fJ/conv-step.
- In Paper 28.4, The University of Texas proposes a PVT-stabilized dynamic amplification technique for stable residue generation in a 12b 330MS/s pipelined SAR ADC. The measured SNDR variation is less than 1dB for supply voltages from 1.25V to 1.35V and temperatures from 5°C to 85°C.
- In Paper 28.5, IBM presents a pipelined-SAR ADC that employs separate comparators per decision with background offset compensation and common-mode regulation. This 1.5GS/s ADC consumes 6.92mW and achieves over 50dB SNDR at Nyquist with an area of $0.0016mm^2$ implemented in 14nm CMOS.
- In Paper 28.6, The University of Texas introduces a 75MS/s two-step split SAR ADC, incorporating single event effect error-detection techniques to achieve a 100% error-correction rate in an irradiation test with proton beams. The 65nm CMOS prototype demonstrates a 78.5dB peak SNDR and over 100dB peak SFDR at 35MS/s and consumes 24.9mW at 75MS/s.
- In Paper 28.7, Toshiba describes a digital amplifier technique to cancel out all the errors from the low-gain residue amplifier. The 28nm 12b 160MS/s pipelined-SAR ADC employing the proposed technique achieves a 61.1dB SNDR at Nyquist while dissipating 1.9mW from a 0.7V power supply.

Session 28 Highlights: Hybrid ADCs

[28.3] A 125MHz BW, 71.9dB SNDR VCO-Based CT ΔΣ ADC with Segmented Phase-Domain ELD Compensation in 16nm CMOS

[28.4] A 12b 330MS/s Pipelined SAR ADC with PVT-Stabilized Dynamic Amplifier Achieving <1dB SNDR Variation

Paper 28.3 Authors: Sheng-Jui Huang, Nathan Egan, Divya Kesharwani, Frank Opteynde, Michael Ashburn

Paper 28.3 Affiliation: *MediaTek, Woburn, MA*

Paper 28.4 Authors: Hai Huang[1], Sudipta Sarkar[1], Brian Elies[2], Yun Chiu[1]

Paper 28.4 Affiliation: [1]University of Texas, Dallas, TX, [2]Texas Instruments, Dallas, TX

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

CONTEXT AND STATE OF THE ART

- The boundaries between conventional ΔΣ, VCO-based, SAR and pipeline architectures continue to blur, driven by the unrelenting drive towards higher performance.
- ΔΣ converters with VCO-based quantizers are becoming competitive with ΔΣ converters based on conventional quantizers.
- Power-efficient amplification, for example using dynamic amplifiers, is critical to improve efficiency of pipelined SAR and noise-shaping SAR converters.

TECHNICAL HIGHLIGHTS

MediaTek shows a 125MHz bandwidth continuous-time ΔΣ achieving a Schreier FoM of 165dB.

- By unfolding the sampled VCO phases and using a segmented DAC, 7b quantization noise is achieved. Excess loop delay is compensated digitally using phase domain rotation. Using these two techniques, MediaTek demonstrates 71.9dB SNDR in a 125MHz bandwidth and 165dB Schreier FoM.

University of Texas, Dallas introduces a method to reduce the PVT variability of a dynamic amplifier.

- Dynamic amplification offers extremely efficient residue amplification but is sensitive to voltage and temperature variations. University of Texas, Dallas shows that by setting the integration time using a slewing replica amplifier, the SNDR degradation over changes in voltage and temperature is less than 1dB in a 63.5dB SNDR, 330MS/s converter.

APPLICATIONS AND ECONOMIC IMPACT

- The use of an efficient VCO-based quantizer in a continuous-time ΔΣ converter enables improved area and power consumption in various SoCs.
- A robust implementation of dynamic amplifiers extends their use to applications where background gain calibration is not practical. This will enable further reductions in power consumption.

Session 29 Overview: Optical and Electrical Link Innovations

Wireline Subcommittee

Session Chair: *Samuel Palermo, Texas A&M University, College Station, TX*

Session Co-Chair: *Hideyuki Nosaka, NTT, Atsugi-shi, Japan*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline Subcommittee*

Advances in high-performance optical and electrical links are essential for the continued improvements in performance, power, and area demanded by current and future wireline communication systems. The papers presented in this section highlight developments in high-speed optical and electrical transceivers and clocking circuitry. It starts with a 64Gb/s NRZ optical receiver that utilizes a self-referenced bandwidth-optimized TIA co-optimized with a speculative 1-tap DFE to achieve -5.5dBm OMA sensitivity. The next paper describes a transmitter and receiver for 100Gb/s coherent networks with integrated 4x64GS/s 8b ADCs and DACs. This is followed by a paper that demonstrates the first 40Gb/s optical PAM-4 transmitter in zero-change 45nm SOI CMOS. The fourth paper proposes a new phase-domain equalization scheme, which compensates for more than 19dB of channel loss at 16Gb/s. The next paper presents clock generation, recovery, and distribution techniques for flexible-rate transceivers that can be programmed to operate at any rate from 3 to 10Gb/s. The session concludes with a paper that utilizes a time-division dual calibration scheme to improve reference spur performance of injection-locked all-digital PLLs.

- In Paper 29.1, IBM Research describes a 64Gb/s NRZ optical receiver with 1.4pJ/b energy efficiency in a 14nm FinFET technology. It uses a self-referenced bandwidth-optimized TIA co-optimized with a speculative 1-tap DFE to achieve -5.5dBm OMA sensitivity and recovers error-free data (BER<10^{-12}) modulated by a VCSEL driver with 2-tap FFE (main+precusor).
- In Paper 29.2, Broadcom reports the first integrated receiver and transmitter in a 100G coherent DSP chip using 4x64GS/s ADCs and DACs in 20nm CMOS. By supporting 100Gb/s coherent transmission, the overall speed of the transceiver is the fastest among all reported data-converter-based transmitters or receivers.
- In Paper 29.3, The University of California, Berkeley, demonstrates the first 40Gb/s optical PAM-4 transmitter in zero-change 45nm SOI CMOS. The segmented "spoked" ring resonator structure, configured as an optical DAC and assisted by a thermal control loop, achieves modulator driver energy efficiency of 42fJ/b which is 2 orders of magnitude better than MZI-based transmitters.
- In Paper 29.4, in order to alleviate limitations associated with minimum pulse width in previously proposed pulse-width-modulation-based equalization, Oregon State University proposes a new equalization scheme based on accumulating and then applying the desired reduction in pulse width across multiple consecutive identical symbols. When operating at 16Gb/s, the 65nm CMOS transceiver compensates for more than 19dB of channel loss while consuming 57.3mW of power.
- In Paper 29.5, Korea University presents a new balanced-4-wire low-EMI signaling scheme for intra-panel interfaces that guarantees embedded symbol-spaced transitions for direct clock recovery by the receiver without any coding overhead. The 28nm CMOS interface achieves 12Gb/s over 4 wires consuming 3.1pJ/b and occupies 0.026mm^2, while emission spur levels are reduced by approximately 24dB.
- In Paper 29.6, The University of Illinois at Urbana-Champaign presents clock generation, recovery, and distribution techniques for flexible-rate transceivers. Using a fixed-frequency low-jitter clock provided by an integer-N PLL, fractional frequencies are generated/recovered locally using multi-phase fractional clock multipliers. Fabricated in 65nm CMOS, the prototype transceiver can be programmed to operate at any rate from 3 to 10Gb/s. At 10Gb/s, integrated jitter of the TX output and recovered clock is 360fs_{rms} and 758fs_{rms}.
- In Paper 29.7, Seoul National University presents time-division dual calibration to improve reference spur performance of injection-locked all-digital PLLs. The 65nm CMOS prototype chip achieves a spur level of -65dBc, which represents an improvement of 23dBc.

Session 29 Highlights: Optical and Electrical Link Innovations

[29.2] Transmitter and Receiver for 100Gbps Coherent Networks with Integrated 4x64GSps 8bit ADCs and DACs in 20nm CMOS

[29.3] A 40Gb/s PAM-4 Transmitter based on a Ring-Resonator Optical DAC in 45nm SOI CMOS

Paper 29.2 Authors: *Jun Cao, Delong Cui, Ali Nazemi, Tim He, Guansheng Li, Burak Catli, Mehdi Khanpour, Kamgmin Hu, Tamer Ali, Heng Zhang, Hairong Yu, Ben Rhew, Shiwei Sheng, Yonghyun Shim, Bo Zhang, Afshin Momtaz*

Paper 29.2 Affiliation: *Broadcom, Irvine, CA*

Paper 29.3 Authors: *Sajjad Moazeni[1], Sen Lin[1], Mark T Wada[2], Luca Alloatti[3], Rajeev J Ram[4], Milos A Popovic[5], Vladimir Stojanovic[1]*

Paper 29.3 Affiliation: *[1]University of California at Berkeley, Berkeley, CA, [2]Ayar Labs, San Franscisco, CA, [3]ETH Zurich, Zurich, Switzerland, [4]Massachusetts Institute of Technology, Cambridge, MA, [5]Boston University, Boston, MA*

Subcommittee Chair: *Frank O'Mahony, Intel, 2501 NW 229th Avenue Hillsboro, OR, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- At rates of 100Gb/s and above, CMOS DSP-based transceivers integrated with high-sampling-rate data converters are critical to realizing the phase-sensitive modulation schemes based on coherent detection utilized in metro and long-haul networks. To meet this demand, this year's conference reports the first integrated receiver and transmitter in a 100G coherent DSP chip using 4x64GS/s ADCs and DACs in 20nm CMOS.
- Silicon photonics is a rapidly maturing technology promising to realize low-cost and energy-efficient optical links for rack-to-rack, within-rack datacenter applications, and supercomputer interconnects. In ISSCC 2017, a monolithically integrated 40Gb/s PAM-4 transmitter in a zero-change commercial 45nm SOI CMOS process is demonstrated using an optical digital-to-analog converter based on a segmented active micro-ring resonator.

TECHNICAL HIGHLIGHTS

Transmitter and Receiver for 100Gb/s Coherent Networks with 64GS/s 8b ADCs and DACs in 20nm CMOS

- In Paper 29.2, Broadcom reports the first CMOS receiver and transmitter in a 100Gb/s coherent DSP chip, integrating 8b 4x64GS/s ADCs and DACs. It reaches the highest level of integration and is the fastest among all reported data-convertor-based transmitters or receivers. The individual ADC and DAC in the receiver and transmitter achieve state-of-art FOM relative to reported high-speed data converters.

40Gb/s PAM-4 Transmitter Based on a Ring-Resonator Optical DAC in 45nm SOI CMOS

- In Paper 29.3, UC Berkeley demonstrates the first 40Gb/s optical PAM-4 transmitter in zero-change 45nm SOI CMOS. A segmented "spoked" ring resonator structure is configured as an optical DAC and achieves modulator driver energy efficiency of 42fJ/b, which is 2 orders of magnitude better than MZI based transmitters.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of complete transceivers operating at data rates of 56Gb/s and beyond is critical to extending the high speed signaling roadmap that supports and enables Big Data infrastructure.
- Minimizing electro-optical transceiver power consumption is critical to enabling the use of small form factor silicon photonic optical modules.

ISSCC 2017

TRENDS

Conditions of Publication

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2017 in February in San Francisco

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 64th appearance of ISSCC, on February 5th to February the 9th, 2017, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2017, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 5 - February 9, 2017,

at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of October 9, 2016, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.

HISTORICAL TRENDS IN TECHNICAL THEMES

ANALOG SYSTEMS

ANALOG SUBCOMMITTEE

DATA CONVERTERS SUBCOMMITTEE

Analog – 2017 Trends

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for IoE devices, or to supplement conventional battery supplies in portable devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or super-capacitor. This trend is captured by movement towards the top-left in the plot shown in Fig. 1.

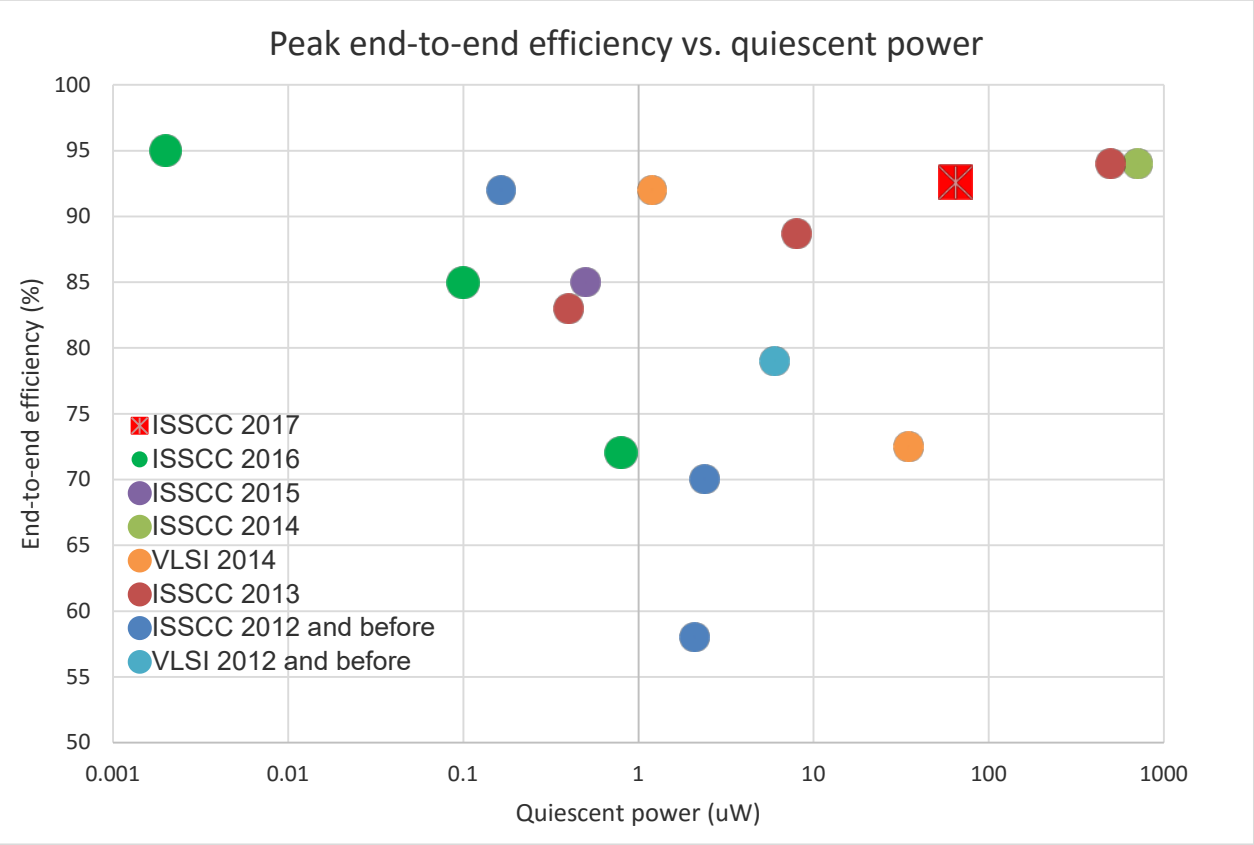

Fig. 1 – Comparison of Integrated Energy Harvesting Systems showing End-to-End Efficiency vs Quiescent Power

Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. This trend is captured by movement towards the bottom-right in the plot shown in Fig. 2. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will lead to devices powered indefinitely from sustainable sources, opening the door to internet of everything, ubiquitous sensing, environmental monitoring, and medical applications.

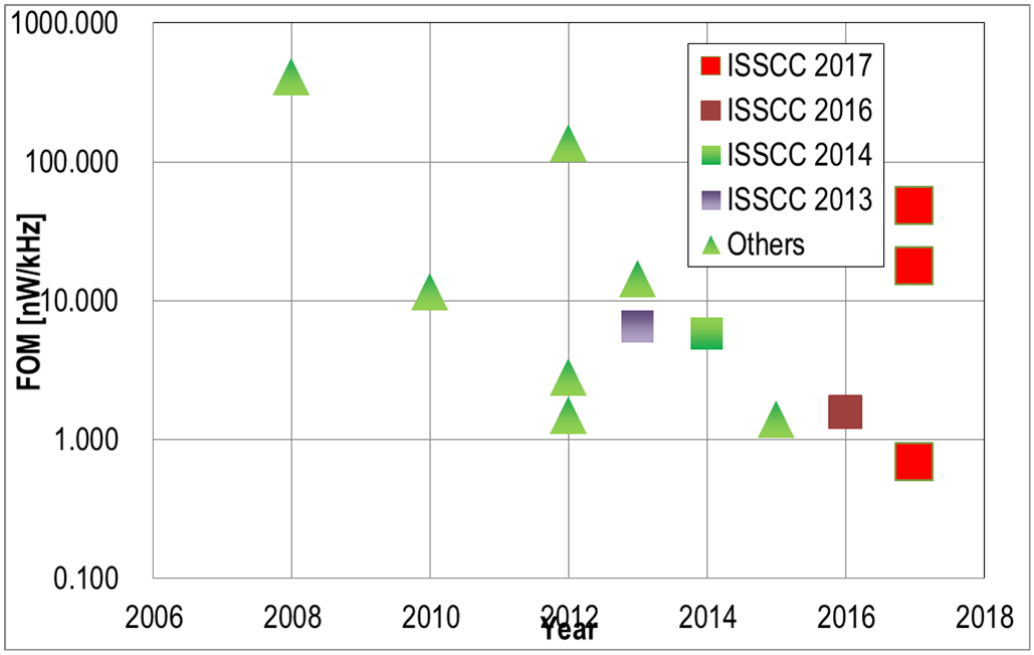

Fig. 2 – Comparison of Integrated 3-to-2000kHz Oscillators showing Power Normalized to Frequency vs Year

Analog circuits also serve as bridges between the digital world and the analog real world. Just like actual bridges, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, since digital circuits, such as microprocessors, drive the market, semiconductor technology has been optimized relentlessly over the past 40 years to reduce their size, cost, and power consumption. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in the analog parameters has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor processes. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area, and increasing power density. The latest advances are implemented in low cost standard CMOS technologies. These trends are captured by movement towards the top-right in the plot shown in Fig. 3.

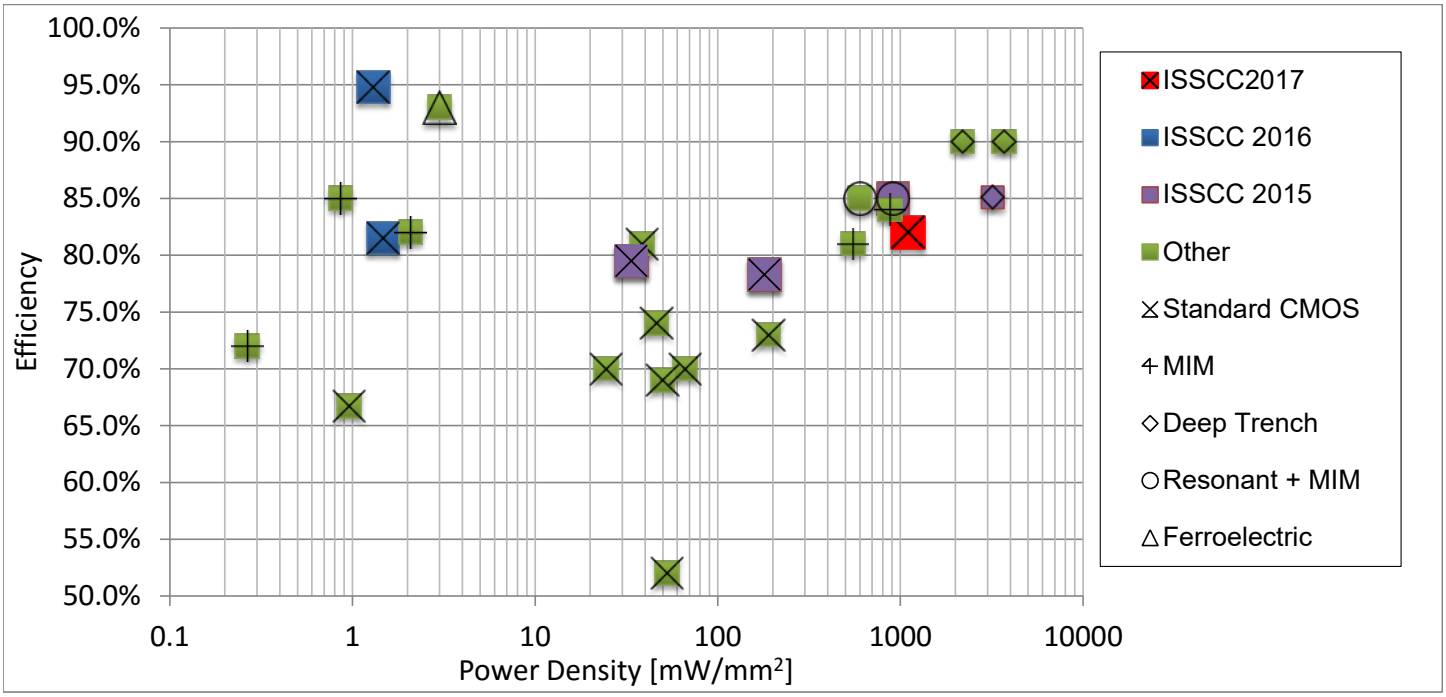

Fig. 3 – Comparison of Integrated Switched-Capacitor Power Converters showing Peak Efficiency vs Maximum Power Density

Data Converters – 2017 Trends

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

Data converters form the key link between the analog physical world and the world of digital computing and signal processing prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and greater linearity while continuing to increase power efficiency. The dominance of successive-approximation (SAR) techniques continues at ISSCC 2017 with their extension into pipelined architectures to set new metrics in resolution and conversion speed.

The three figures below represent traditional metrics to capture innovative progress in data converters. The first figure plots power dissipated relative to the effective Nyquist rate (P/f_{snyq}), as a function of signal-to-noise and distortion ratio (SNDR), to give a measure of ADC power efficiency. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 5fJ/conversion-step. ISSCC 2017 heralds the first converter achieving this benchmark while simultaneously demonstrating nearly 80dB SNDR through the use of noise shaping and dynamic amplification techniques. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Contributions at ISSCC 2017 are depicted by the colored legends representing various converter architectures; historical contributions are shown using smaller markers. (Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart.)

The second figure plots signal fidelity vs. the Nyquist sampling rate normalized to power consumption. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner. This year, pipelined SAR converters demonstrate gigahertz bandwidths while delivering the levels of accuracy and energy efficiency demanded by modern applications.

The final figure plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. Nonetheless, ISSCC 2017 presents multiple approaches demonstrating excellent results in this metric. A continuous-time noise-shaped pipeline joins interleaved converters based on SARs and pipelined SARs to advance the state-of-the-art across a wide range of SNDR and bandwidths.'

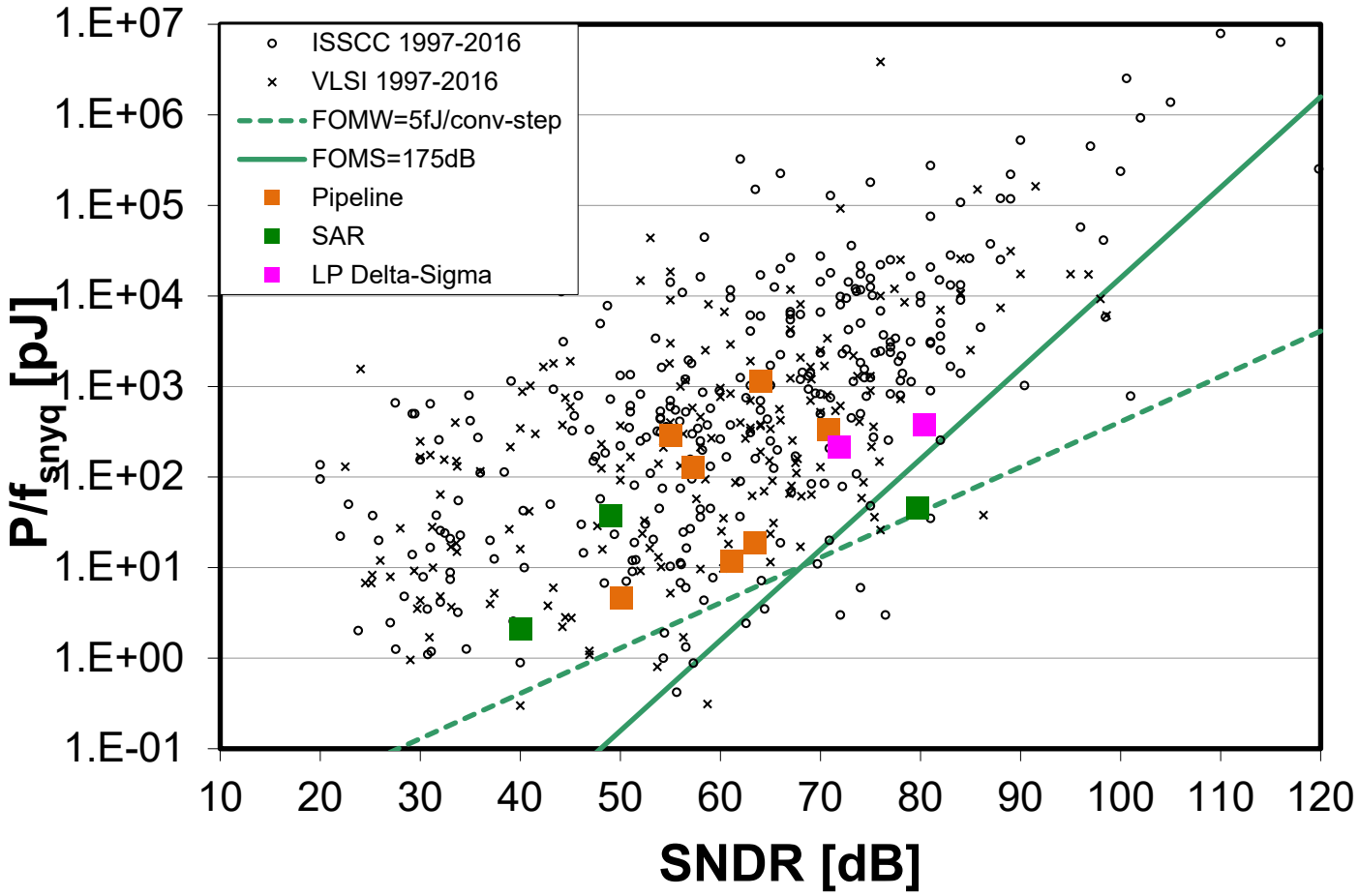

Figure 1: ADC power efficiency (P/f_{snyq}) as a function of SNDR

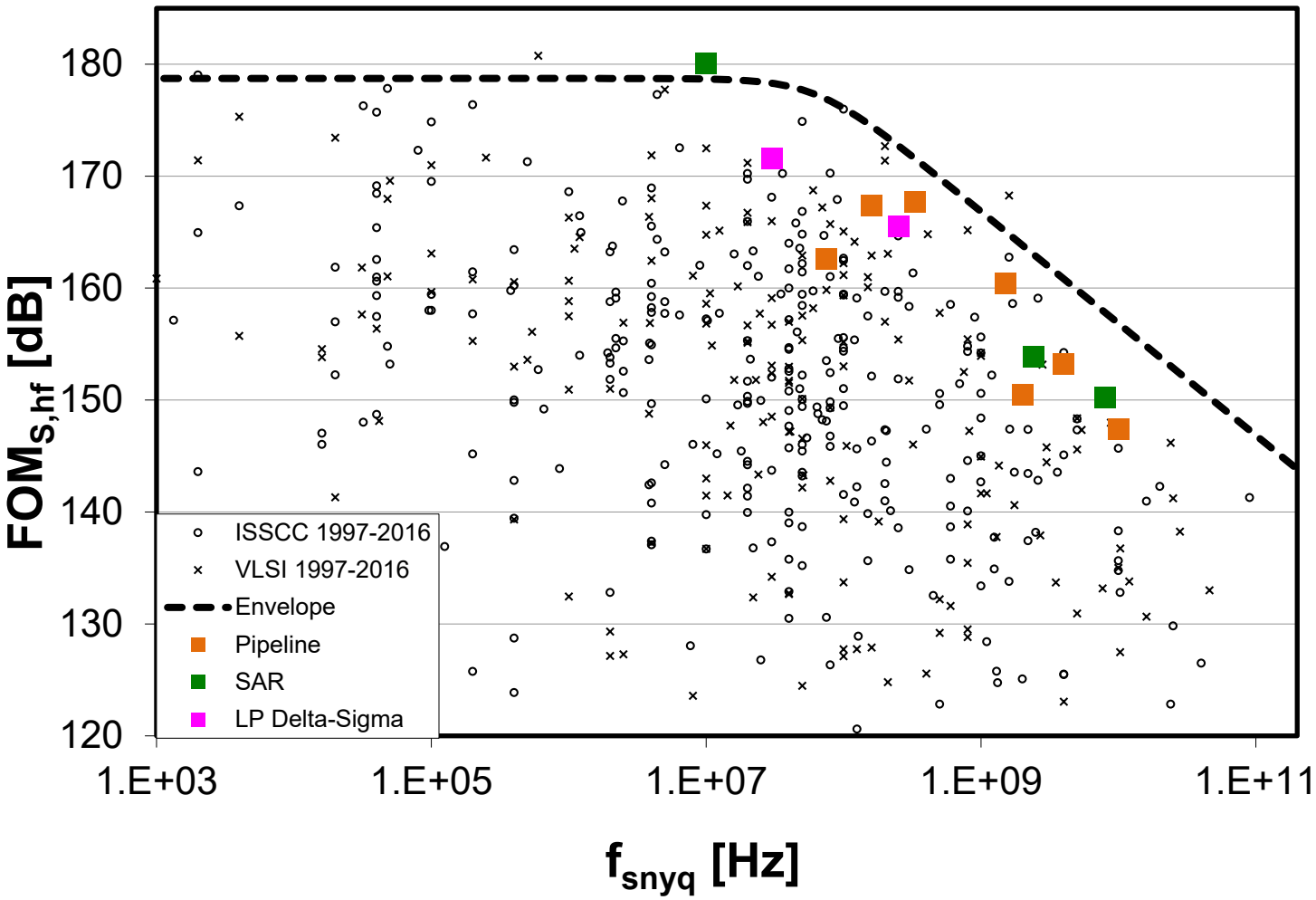

Figure 2: Power normalized noise and distortion vs. the effective Nyquist sampling rate

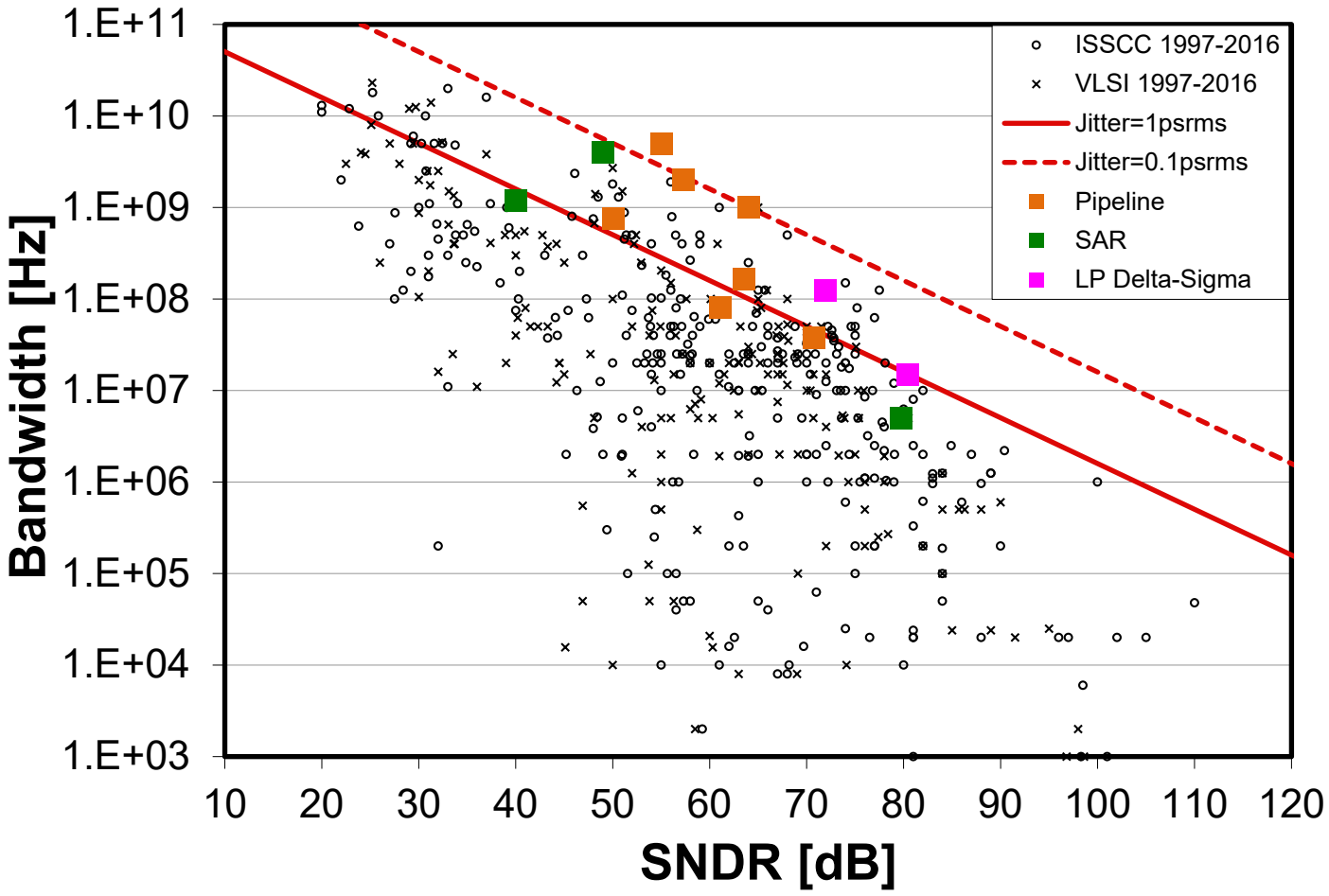

Figure 3: Bandwidth vs. SNDR

HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

RF SUBCOMMITTEE – WIRELESS SUBCOMMITTEE

WIRELINE SUBCOMMITTEE

RF Subcommittee – 2017 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

Introduction

This year, ISSCC 2017 shows ongoing advancements in circuits and subsystems for various applications spanning a broad frequency range from below 1GHz to beyond 1THz. Innovation topics include circuits for RF and mm-wave frequency generation, efficient power-amplification techniques as well as building blocks for mm-wave and THz spectroscopy, imaging applications and broadband communication systems. This document highlights such trends that will emerge at the 2017 ISSCC conference. Papers showcase advances in voltage controlled oscillators, digitally-intensive mm-wave frequency synthesizers, linearized power amplifiers, and efficiency-improving envelope-tracking transmitter front-ends. RF building blocks demonstrate support for complex modulation schemes to enable increased data-rates. Advanced circuit and system techniques as well as antenna interface improvements enable broadband imagers and spectrometers at mm-wave/THz frequencies.

RF and mm-wave frequency generation: The trend is toward high-efficiency frequency generation, ultra-low-voltage frequency generation without compromising figure-of-merit (FOM), and the use of calibration and digital architectures targeting applications such as 5G and wireless LAN. The 2017 ISSCC presents a high-efficiency, high-power multiport radiating element at 114GHz in SiGe BiCMOS technology is demonstrated. An efficient calibration technique, applied to a 27GHz-to-31GHz injection-locking frequency multiplier with quadrature outputs, is introduced. In the area of frequency synthesizers, three papers at ISSCC 2017 highlight advancements in digital architectures: a 50GHz-to-66GHz PLL featuring low-noise and low spur levels by leveraging a high-speed TDC and intensive calibrations; two PLLs based on ring-oscillators, leveraging subsampling phase detection and FIR filtering, respectively, to achieve simultaneously low noise and compact area. An ultra-low voltage DCO in a 16nm FinFET technology with a 188dBc/Hz FOM is shown. As illustrated with a 2017 ISSCC ultra-low-voltage VCO identified in Figure 1, frequency generation with low phase-noise at low power becomes challenging and even more so at higher frequencies.

Efficient power amplification for broadband communications systems: Improving efficiency at the back-off power levels has become an active area of research to support spectrally efficient modulation schemes with high peak-to-average power ratios. Doherty-like power-amplifier topologies and envelope-tracking supply modulation are key enablers to improve the back-off efficiency of transmitters. Increasing signal bandwidths for applications such as carrier-aggregation LTE and WiFi 802.11ac poses challenges for supply modulation. A triple-band mm-wave PA with an offset-line-based transformer is discussed and demonstrates the enhancement of efficiency and bandwidth. A WLAN SoC with a fully-integrated envelope tracker is demonstrated for wideband modulation. A Class-G voltage-mode Doherty power amplifier is presented, which achieves high efficiency at various power backoff levels. The trend to simultaneously optimize power and efficiency is indicated in Figure 2. This year, at ISSCC 2017, wideband PAs achieve high linearity in addition to adequate P_{sat} and PAE for both cellular applications with excellent EVM and mm-wave frequencies over multiple bandwidths.

RX and TX Building Blocks: The 2017 ISSCC will highlight several advances in the state of the art in the RF, mm-wave, and THz domains. Antenna interface improvements include a circulator for TX/RX isolation, a digitally assisted CMOS front-end module, a polar PA with intrinsic nonlinearity compensation, electrical-balance-duplexer impedance detection, and radiator-embedded power combining. Wideband systems for spectroscopy achieve record bandwidths and parallel multitone generation. A 310-to-370GHz array embeds beam steering with independent frequency tuning. High data-rate communication is demonstrated with a 5m 130GHz 12.5Gb/s link and a 105Gb/s 300GHz transmitter with 6 carrier-aggregated 128-QAM channels.

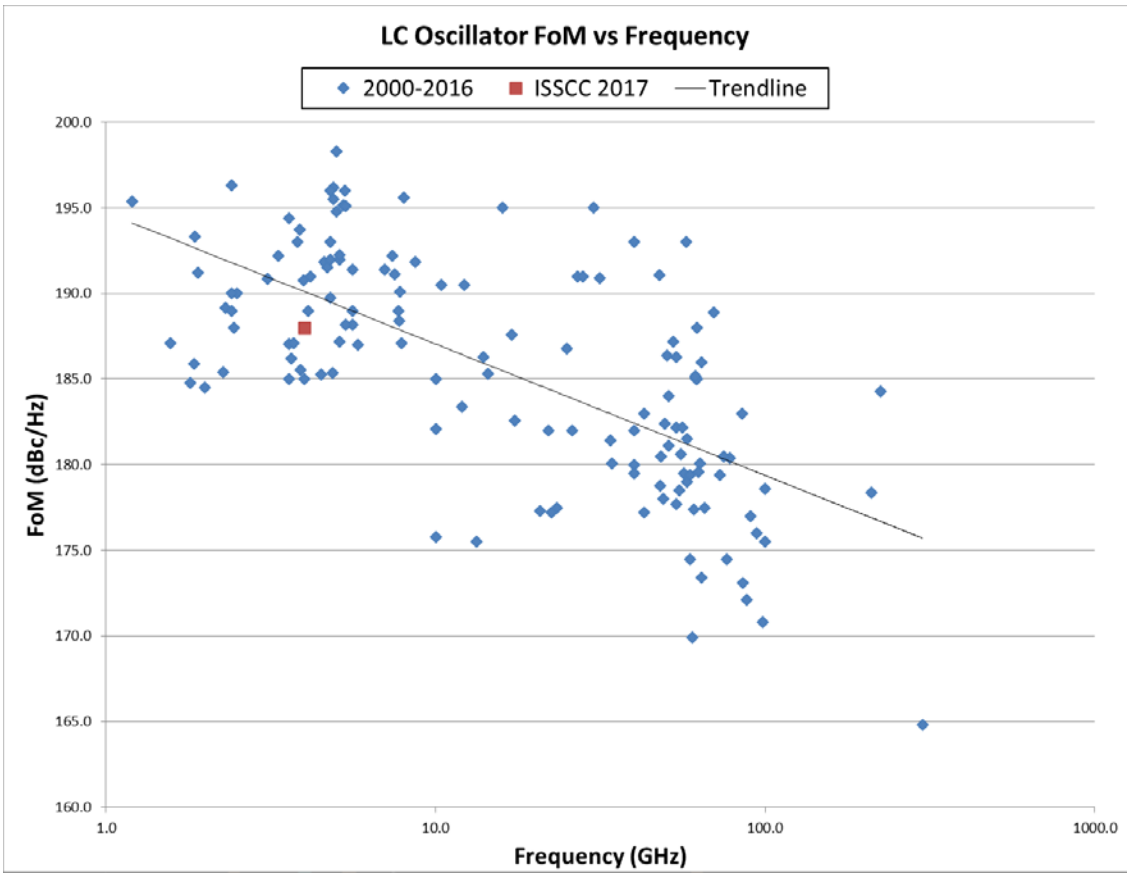

Figure 1: LC Oscillator FoM versus frequency.

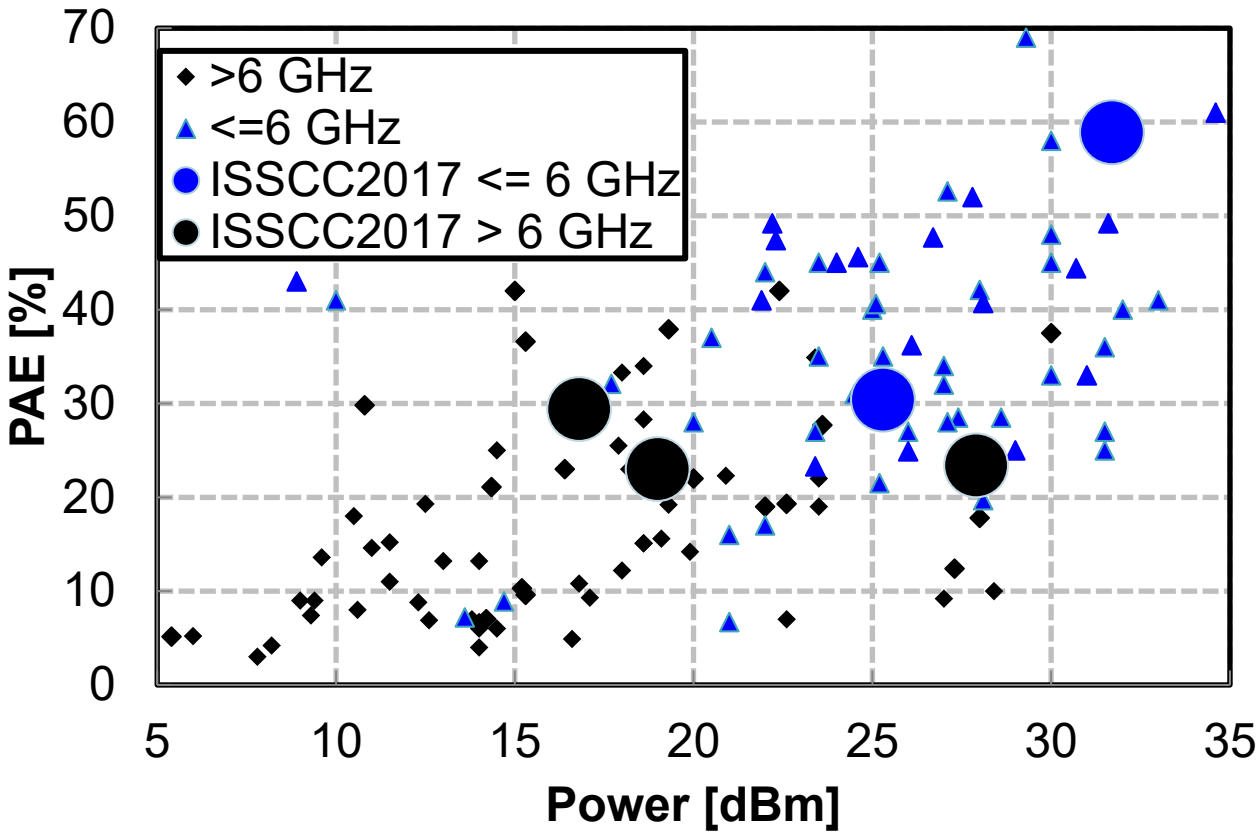

Figure 2: PAE (%) vs. output power for recent submicron CMOS PAs.

Wireless – 2017 Trends

Subcommittee Chair: Aarno Pärssinen, University of Oulu, Oulu, Finland

The insatiable need for big-data communication calls for transceivers with high throughput, achieved through higher digital modulation, carrier aggregation, MIMO with beam forming or beam steering, and interference detection and cancellation. As presented at ISSCC 2017, a variety of new techniques have been developed, such as a 5G transceiver employing dual polarized beam steering with a 32-phased array, a 128QAM 4-channel bonding transceiver, a MIMO receiver array with analog/RF spatial equalization and a wideband full-duplex cancellation transceiver**,** to help push to even higher data-rates.

As seen at ISSCC 2017, high-speed digital complex sampling schemes applied to transmitters, receivers, and fractional-N PLL's allow RF to scale with digital in more advanced process nodes. Digital PAs replace the area-hungry inductors/transformers with high-speed digital processing circuits running at lower supply voltage. Various kinds of digital PAs such as switched capacitor, inverse Class-D/E and Class-F digital PAs are reported paving the way for a lower cost, miniaturized module. The FOM of all digital fractional-N spurious reduction PLLs continues to improve to enable higher SNR, higher data-rate, and ultimately better spectral efficiency.

At ISSCC 2017, in IoE space, ultra low power and highly integrated system solutions have emerged in various fields. A first sub-GHz ultra-narrow-band DBPSK/GFSK modulation RF transceiver for low-power wide-area networks is reported. In designing IoT devices, there is a well-known trade-off in sensitivity, output power, and blocker tolerance for lower cost and low power. Instead, a higher output power and better sensitivity Bluetooth low-energy transceiver with integrated RF bandpass filter saving overall power consumption is reported.

Figure 1 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency trends, while Figure 2 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends. Because many different techniques are used to design the circuits, there is significant scatter in the graphs. However, in both cases, the arrows show the desired trend directions.

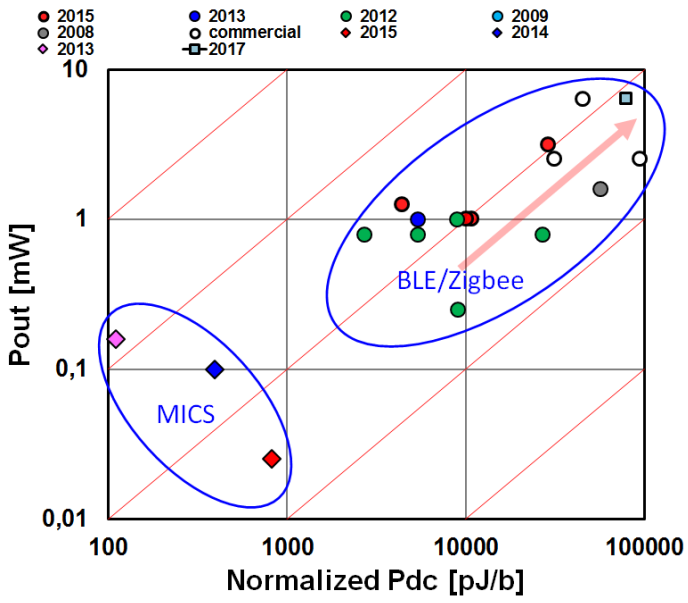

Figure 1: Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency Trends.

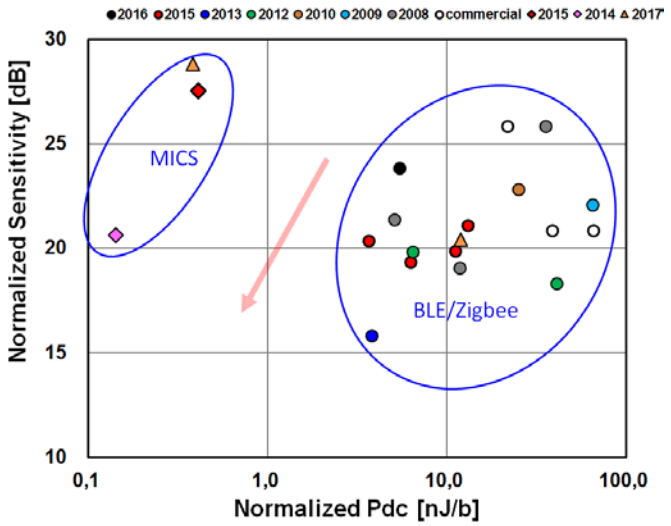

Figure 2: Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends.

Wireline – 2017 Trends

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR*

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2 to 3× every 2 years. Demand for bandwidth is driven by applications such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this demand has been met by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than simply transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems. Papers at ISSCC this year include a 64Gb/s NRZ optical receiver in 14nm CMOS, a 64Gb/s PAM-4 transmitter in 28nm CMOS, and a 100Gb/s coherent optical transceiver in 20nm CMOS featuring 4x64GS/s 8b ADCs and DACs.

Energy Efficiency and Interconnect Density:
Power consumption of I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os have increased, so has the percentage of total power consumed by I/Os. Technology scaling enables increased clock and data rates and offers improved energy, especially for digital components. However, simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss is slightly less than unity—in particular, that 30dB channel loss corresponds to a roughly 10× increase in pJ/b. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. At ISSCC this year, Paper 6.4 demonstrates a 64Gb/s 4-tap FFE PAM-4 TX with 1.2Vppd swing that consumes only 2.3pJ/b. Paper 29.5 combines high signaling density with low power, demonstrating a braid clock signaling scheme over four balanced NRZ lines for interpanel interfaces.

Electrical Interconnect:
There is ever-growing demand for very high data rate communication across a wide variety of channels. Some types of channels, especially those related to medium-distance electrical I/O, such as server backplanes, must support high data rates over high-loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent receivers achieve data rates above 28Gb/s across channels with up to 50dB of loss. This year at ISSCC, we see examples of transceivers that are starting to extend the equalization range of 56Gb/s wireline communication. This year at ISSCC, Paper 6.2 describes a 60Gb/s NRZ transceiver that compensates 21dB loss at an energy efficiency of 4.8pJ/b. Paper 6.3 presents a 40-56Gb/s PAM-4 receiver with 10-tap direct feedback equalization.

Optical Interconnect:
As the bandwidth demand has accelerated and as electrical channel impairments become increasingly severe with the rise of per-lane data rates, optical interconnects have become an increasingly attractive alternative to traditional electrical wireline interconnects. Optical communication has clear benefits for high-speed and long-distance interconnects because it offers lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. At ISSCC this year, a 64Gb/s 1.4pJ/b optical receiver [Paper 29.1], a 40Gb/s PAM-4 transmitter based on a ring resonator optical DAC [Paper 29.3], and an ADC-and-DAC-based analog front-end for coherent optical transceivers [Paper 29.2] are presented.

Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2017.

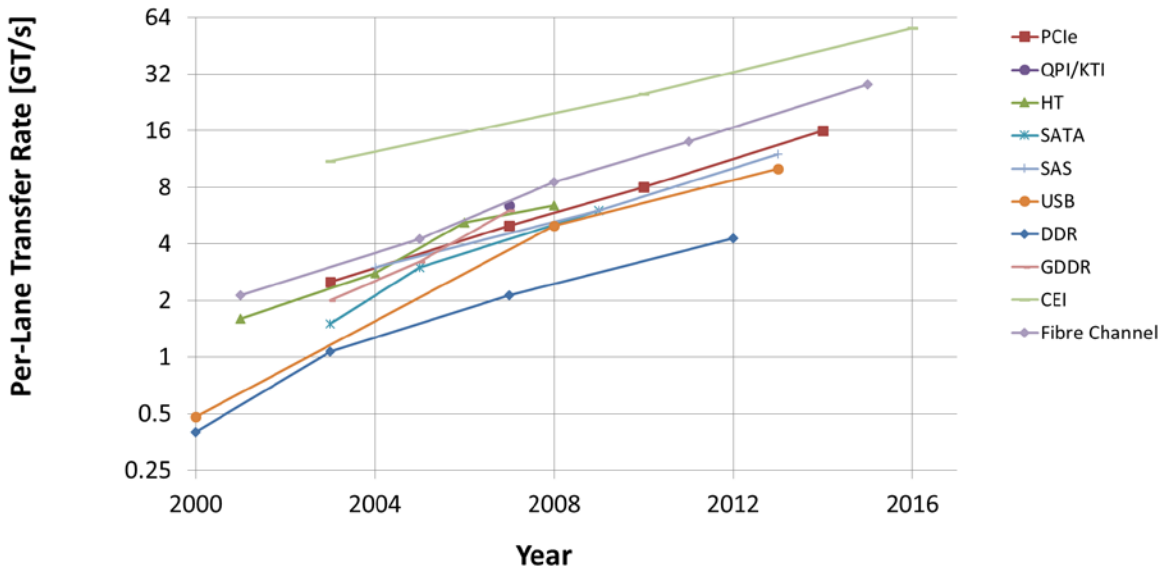

Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

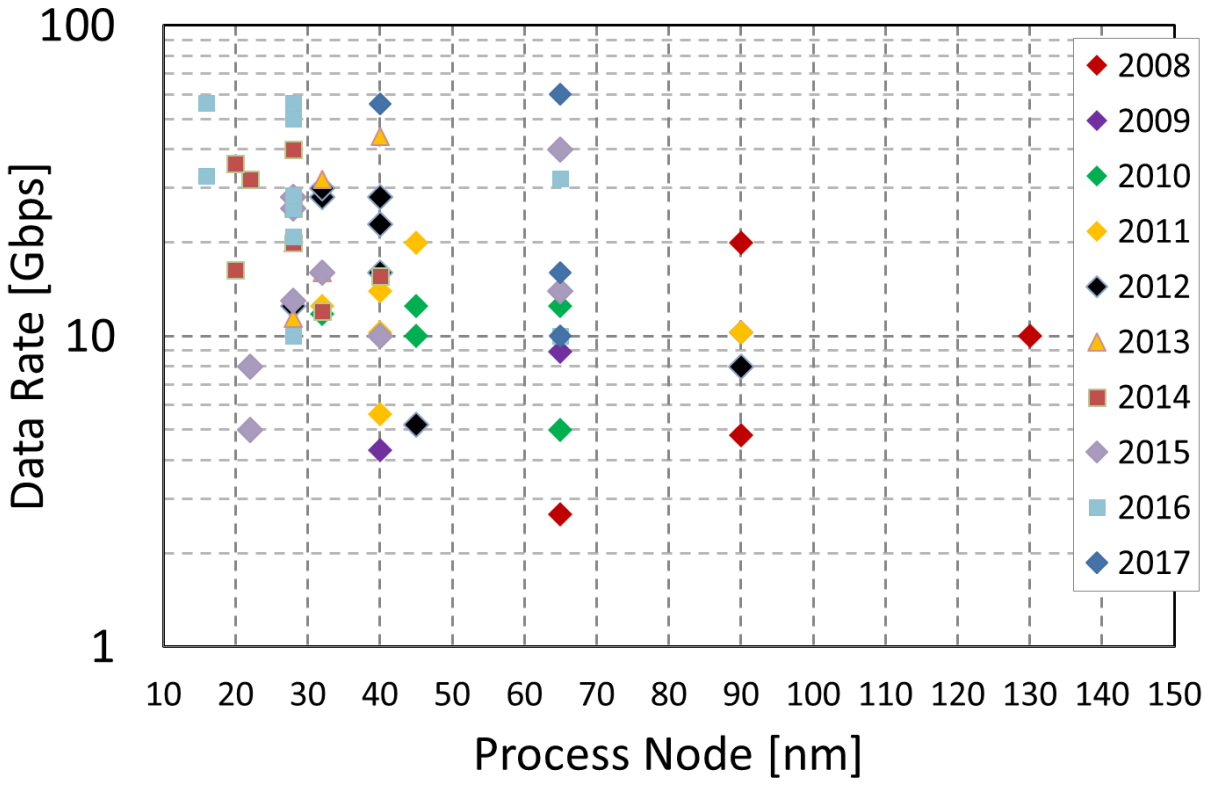

Figure 2: Data-rate vs. process node and year.

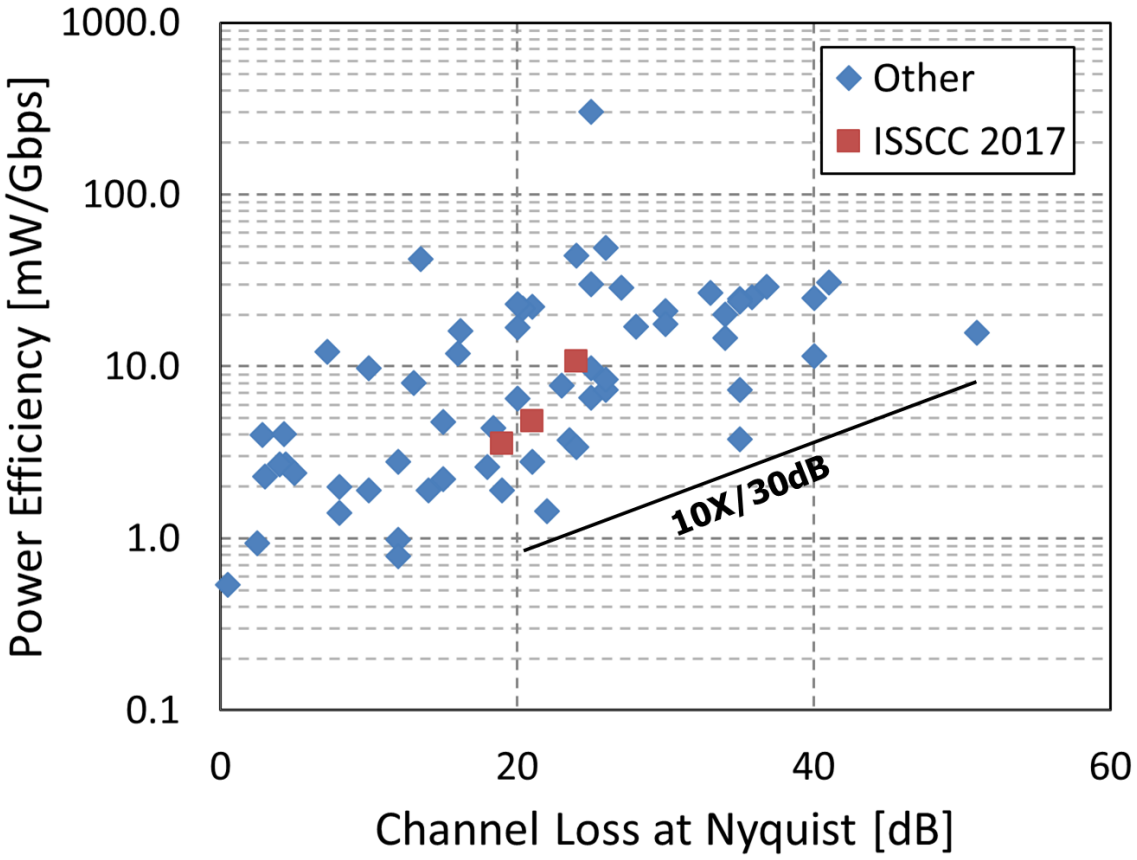

Figure 3: Transceiver power efficiency vs. channel loss.

HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE

DIGITAL CIRCUITS SUBCOMMITTEE

Digital Architectures & Systems (DAS) – 2017 Trends

Author: Byeong-Gyu Nam, *Chungnam National University, Daejeon, Korea, Digital Architectures and Systems Sub-Committee Chair*

This year at ISSCC 2017, process scaling continues with the application of the 10nm node. Process scaling continues to enable integration of more transistors and reduces power consumption, but frequency scaling is slowing down. Thus, performance improvements are now being achieved primarily through architectural innovations.

One continued trend is towards increasing heterogeneity with application-specific CPUs, GPGPUs, and custom accelerators. Thus, computation is moving from general-purpose CPUs to more power-efficient cores to meet performance demands within limited power budgets. From the following graphs, the core numbers (Figure 1) and frequencies (Figure 2) are not growing significantly, but application-specific cores and accelerators represent a growing portion of die area. Heterogeneous computing that enables efficient collaboration among various cores is gaining in importance.

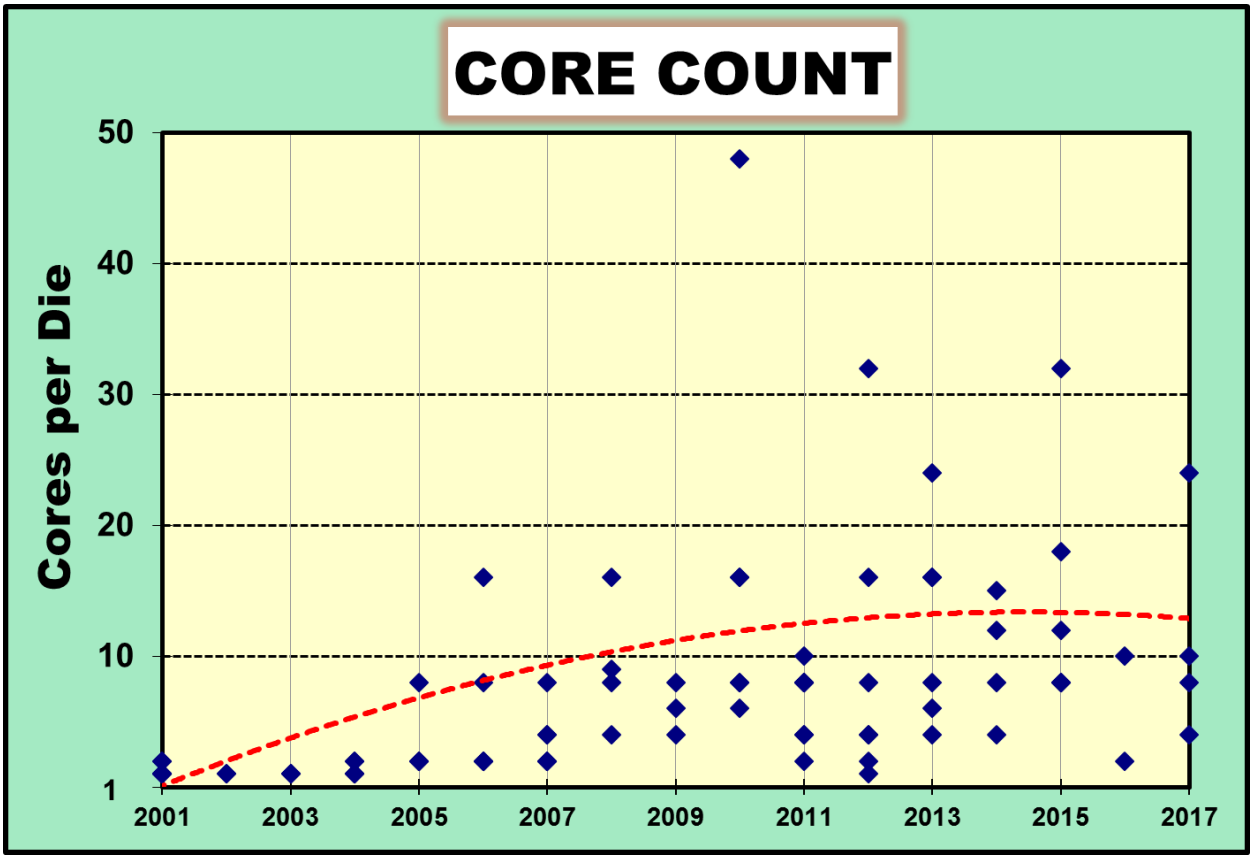

Figure 1. Core counts on processors published at ISSCC.

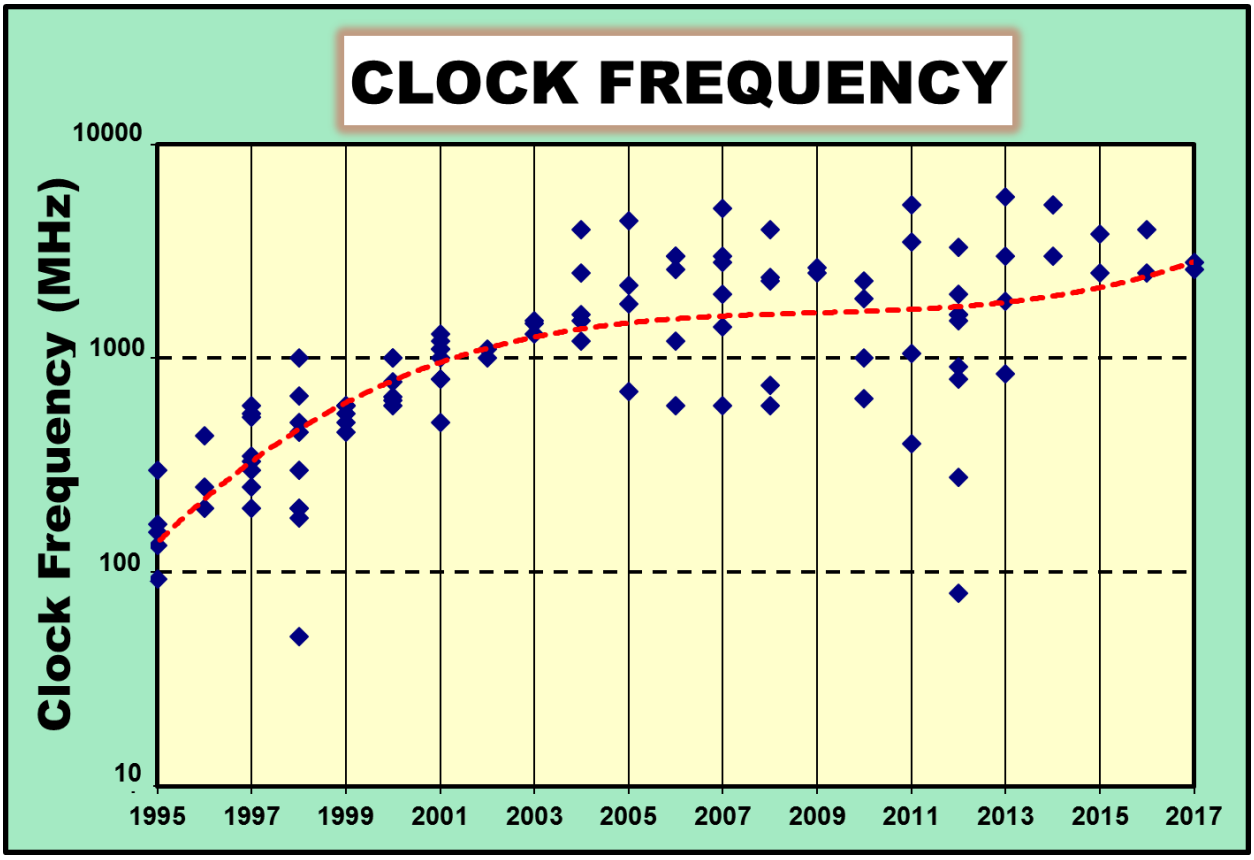

Figure 2. Clock frequency scaling trends.

Using Increased Integration Density to Improve Application Energy Efficiency

The first 10nm chip is a mobile applications processor SoC, as the development cycle is shorter than for high-performance general-purpose CPUs. The new process node provides lower power (Figure 3) and higher performance-per-Watt, even though transistor speed has saturated. Advanced power management techniques – such as integrated voltage regulators, fast voltage-droop detection and mitigation, and adaptive voltage guard bands – are now crucially important to maximize the power efficiency or performance within a power/thermal budget. Continued area scaling allows increased core numbers for CPUs and GPUs, and also additional multimedia features, such as dual cameras, larger screen size, and VR features.

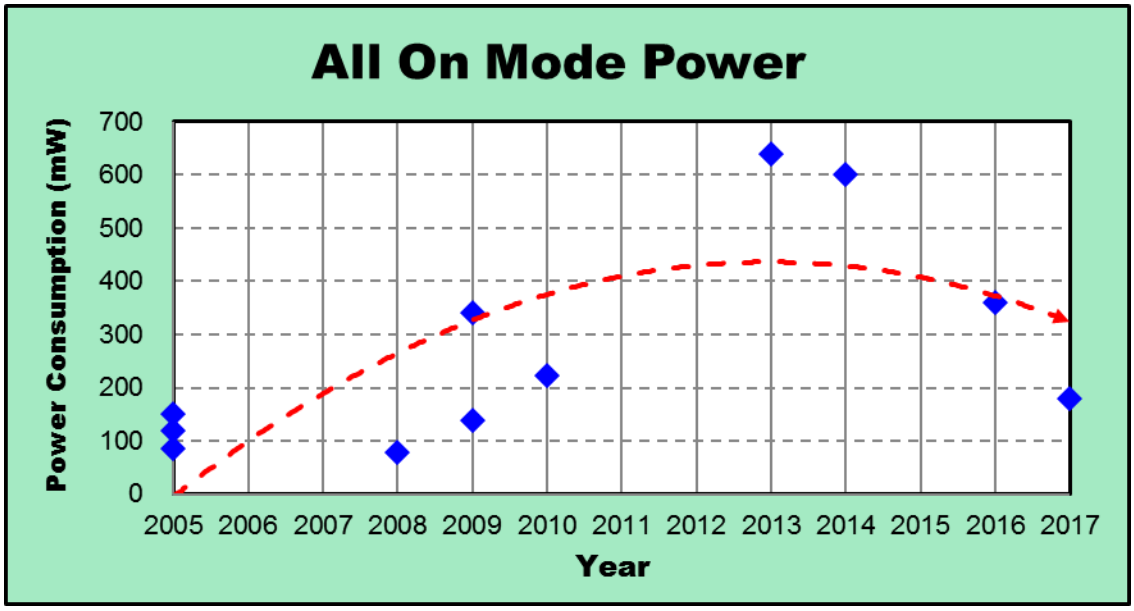

Figure 3. Application processor power trends.

Figure 4 shows application processor feature trends for smart phones. These CPUs are now running up to 2.8GHz, approaching laptop and desktop CPUs. Single-thread performance is improved by micro-architectural improvements and multi-thread performance by adding more cores and more efficient management of differently optimized cores. State-of-the-art incorporates up to ten cores with three distinct power/efficiency points. A new graphics API standard, Vulkan, will utilize multicores more efficiently. Virtual reality (VR) is one of the key drivers of the demand for the evolution of GPUs, displays and cameras. Small CPU sub-systems are being added for I/O and sensor-hub control to ensure low-power always-on functionality. Wireless bandwidth keeps evolving, reaching 1.6Gb/s bandwidth and heading toward 5G in the near future.

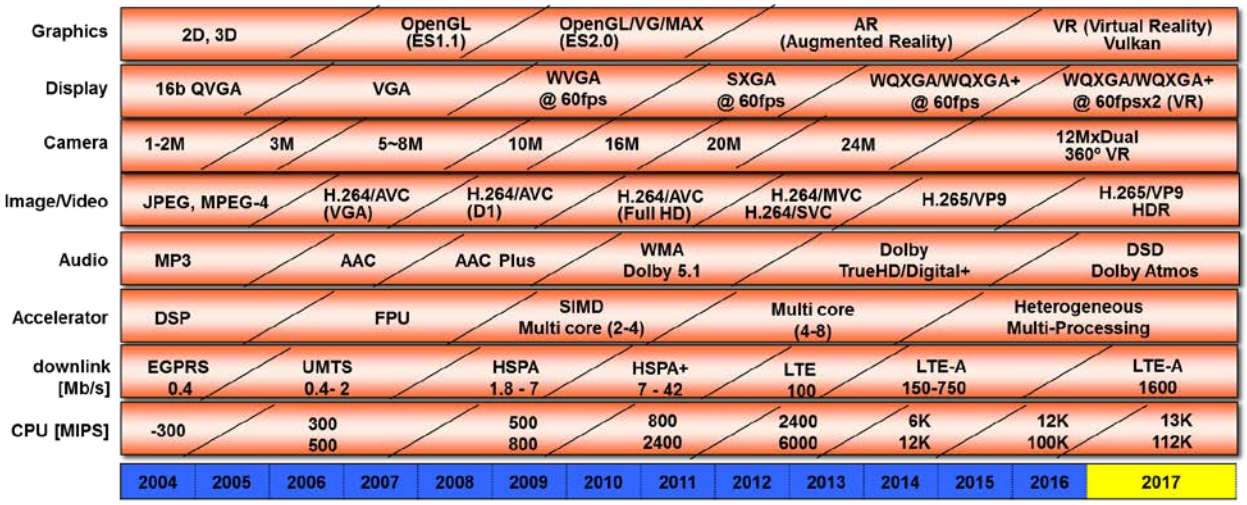

Figure 4. Application processor trends in smart phones.

Wired and wireless links continue to increase in bandwidth. As illustrated in Figure 5, a consistent 10× increase in datarate is seen every five years. The IoE revolution is bringing an explosion of demand for network bandwidth. Everything will be connected through wired and wireless networks, generating a tremendous amount of data to be processed/analyzed in the cloud. Correspondingly, IEEE 802.3 400Gb/s is being developed and LTE-A standard is extending to 1.6Gb/s bandwidth; 5G is targeting 10Gb/s-to-100Gb/s, comparable with current WiFi speeds which can enable real-time VR streaming.

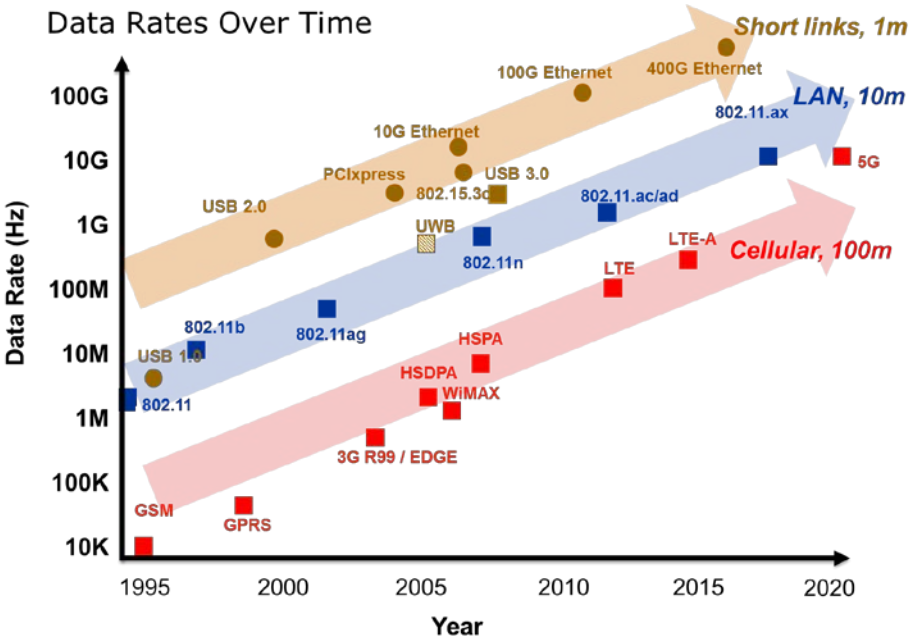

Figure 5. Datarate trends in wired, wireless and cellular.

Deep learning is on the rise, drastically shaking up the landscape of high-accuracy recognition applications, achieving near human performance in visual and acoustic recognition. Yet until now, the computational complexity of typical deep neural networks impedes their execution on resource-scarce mobile or wearable devices. This year, ISSCC 2017 shows strong growth in the area of deep learning processors, significantly improving computational energy efficiency up to multiple TOPS/W, bringing deep neural networks within reach of battery-operated devices. This development has been enabled through innovative memory organization, reduced bit-width computation, and approximate and error-tolerant datapath structures. Figure 6 illustrates the order of magnitude efficiency and throughput improvement to be presented at ISSCC 2017, compared to 2016's state-of-the-art in deep-learning processors. Benefiting from this efficiency leap, several always-on sensing applications will be showcased. Hierarchical wake-up schemes, which gradually activate more and more complex neural networks and recognition algorithms, are exploited to enable always-on recognition at low average power consumption.

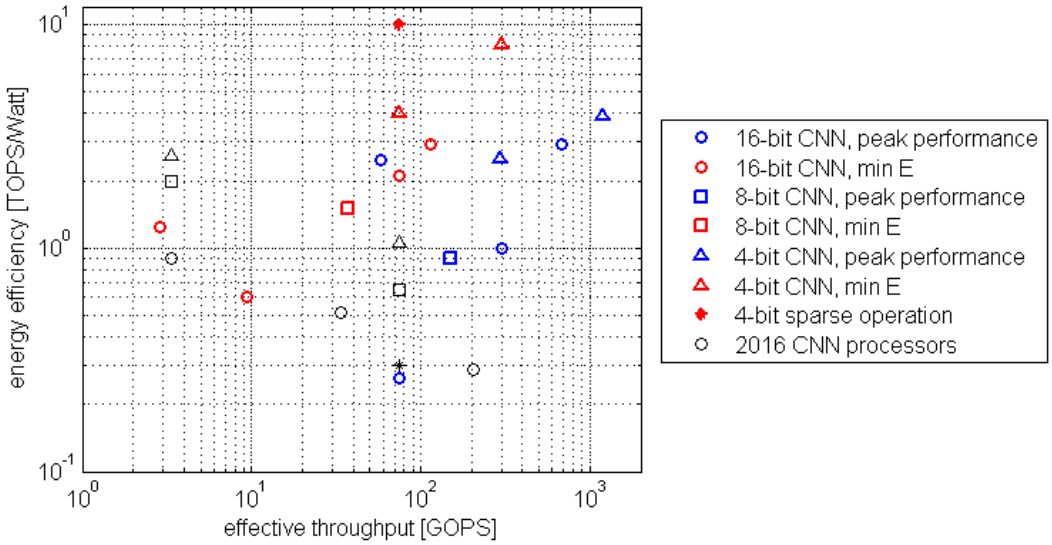

Figure 6. Deep learning processor throughput and efficiency

Highlights for ISSCC 2017

ISSCC 2017 features MediaTek's 10nm FinFET mobile SoC with a tri-gear deca-core CPU complex running up to 2.8GHz. Logic blocks are integrated to aid software and hardware debug, while new circuit blocks improve system power budget management and reduction in supply droop. A new standard-cell approach is used to mitigate the MEOL performance penalty in the 10nm. IBM describes a 24-core microprocessor implemented in 14nm SOI FinFET technology using 17 metal layers. It features a redesigned core based on an execution slice microarchitecture, contains 8B transistors, and has 120MB of eDRAM L3 cache. STMicro presents an energy-efficient deep convolutional neural network (CNN) SoC implemented in a 28nm FDSOI process. The SoC integrates a host CPU, a 16 DSP array and a convolutional DNN accelerator fed by an on-chip reconfigurable network that reduces on-chip and off-chip memory traffic. It achieves a state-of-the-art efficiency of 2.9 TOPS/W and a peak performance of more than 676GOPS. MIT also presents a low-power standalone speech processor with a voice activity detection mechanism for wake-up, and a feed-forward DNN accelerator for speech recognition. It achieves 4.1× fewer word errors, 3.3× lower core power consumption and 12.7× lower memory bandwidth over the prior art.

Digital Circuits – 2017 Trends

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France*

Demand for higher performance across ubiquitous, connected and energy-constrained platforms ranging from Internet of Everything (IoE) to cloud data-centers continues to drive innovations in all CMOS digital circuit building blocks, with goals of improving energy-efficient performance, lowering cost and design effort, and enhancing security. Classic technology scaling has slowed and circuit design efforts are exploiting technology features, such as body biasing or passive-device advancements, to enable circuit innovation.

Energy Efficiency Techniques and Integrated Voltage Regulators

At ISSCC 2017, energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off-chip, are increasingly being integrated on-chip to reduce cost. Low-dropout (LDO) linear regulators, switched capacitor voltage regulators (SCVR), and now, buck voltage regulators are integrated in scaled process nodes to enable faster and fine-grain DVFS of individual functional blocks. The conversion efficiency and current density (Figure 1) of these integrated voltage regulators continues to improve. As well, variation mitigation has become a major trend in digital circuits in order to improve robustness and power efficiency across Process, Voltage and Temperature (PVT). Specific all-digital sensors and adaptive techniques are currently proposed to mitigate these effects on-chip.

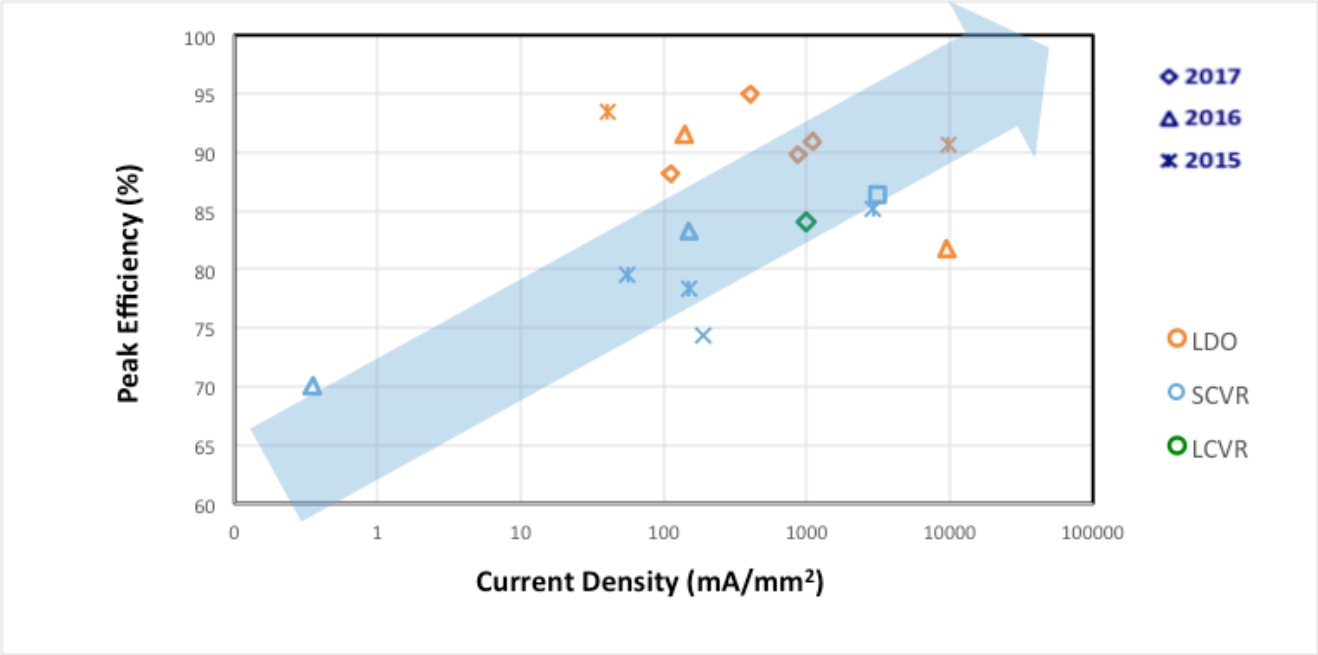

Figure 1 Integrated voltage regulators

Scalable Digital PLLs for Low Jitter Applications

The trend of PLLs is to migrate from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for low jitter PLLs is increasing. The use of more automated digital design flows (e.g. synthesizable and/or standard cells) dramatically reduces development costs but can degrade jitter, requiring new techniques to compensate. Figure 2 highlights metrics for PLLs and DPLLs published at ISSCC over the past 10 years.

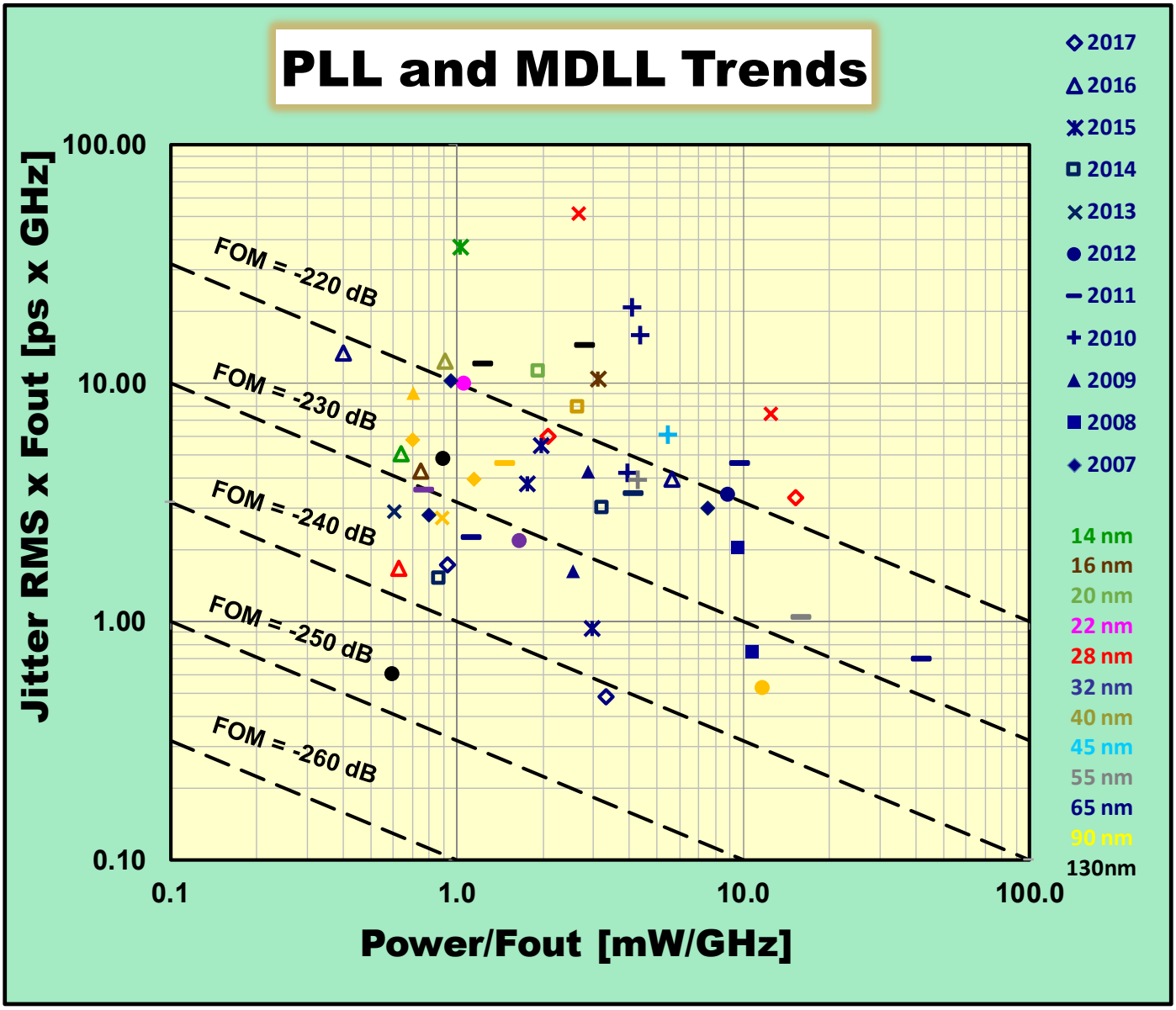

Figure 2. PLL and MDLL trends.

Circuits for Hardware Security

With the increasing risk and cost of information theft, hardware-implemented security has become a common circuit element. Though at ISSCC 2017 focus on cryptographic implementation continues, cost-effective PUFs (Physically Unclonable Functions) are now a focus area, such as smart cards and consumer devices. TRNGs (True Random Number Generators) are leveraged to strengthen secret key generation in cryptographic applications. The figure below shows how energy/b has scaled for such structures in recent years at ISSCC, pursuing both low-energy and stable operation at the same time. Figure 3 illustrates the trends in energy consumption for security circuits over time published at ISSCC.

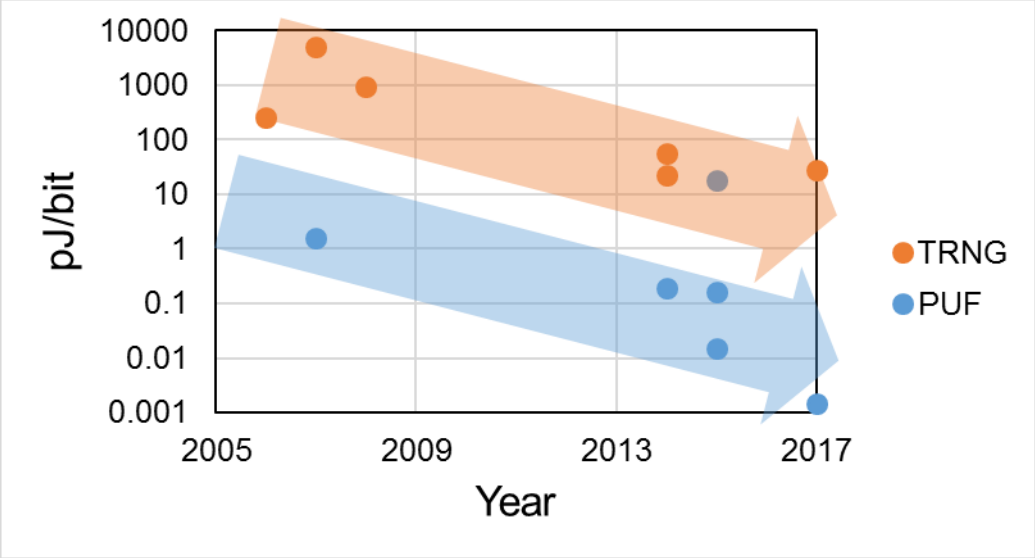

Figure 3. Energy-efficiency evolution in security circuits.

Memory – 2017 Trends

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

The demand for high-density high-bandwidth and low-energy memory systems continues on all fronts from high-performance computing to SoC, wearables and IoE. In embedded memory, record bitcell size SRAM in 7nm operates at the MB level, and a 10nm dual-supply SRAM cache is optimized for power/performance. DRAM high-performance memory interface technologies are enhanced for GDDR5X, LPDDR4 and low-voltage LPDDR4X. STT-MRAM is introduced as a non-volatile memory system matching LPDDR2 interface at a competitive 4Gb size. In non-volatile memory space, a 40nm low-power eFlash and 10nm anti-fuse OTP are introduced for embedded applications, meanwhile 64 layer 3b/cell 3D NAND Flash provides 512Gb capacity.

Some current state-of-the-art papers from ISSCC 2017 include:

- Two sub-0.030μm^2 bitcells in 7nm CMOS are functional at 8Mb and 256Mb array levels.
- An 8Gb GDDR5 is shown to operate at 12Gb/s/pin using a PLL-generated 3GHz clock.
- An 8Gb LPDDR4X DRAM operating at 5Gb/s/pin and 0.6V I/O voltage for low-power high-speed memory access.
- 64 layer 3b/cell 3D NAND Flash at 512Gb with only 132mm^2 die area.
- A 10nm anti-fuse OTP bitcell that achieves reliable operation at the 32kb array level, operating at supplies as low as 0.525V.

SRAM:

For embedded high-speed applications, SRAM continues to be the memory of choice, from mobile to high-performance servers to IoE. This year, at ISSCC 2017, the latest 7nm FinFET technologies with the smallest bitcells achieved to date for SRAM – down to 0.027μm^2. Key industry benchmarks for 10nm SRAM and 14nm TCAMs are also presented. Fig.1 shows SRAM bit cell area and V_{min} scaling trend.

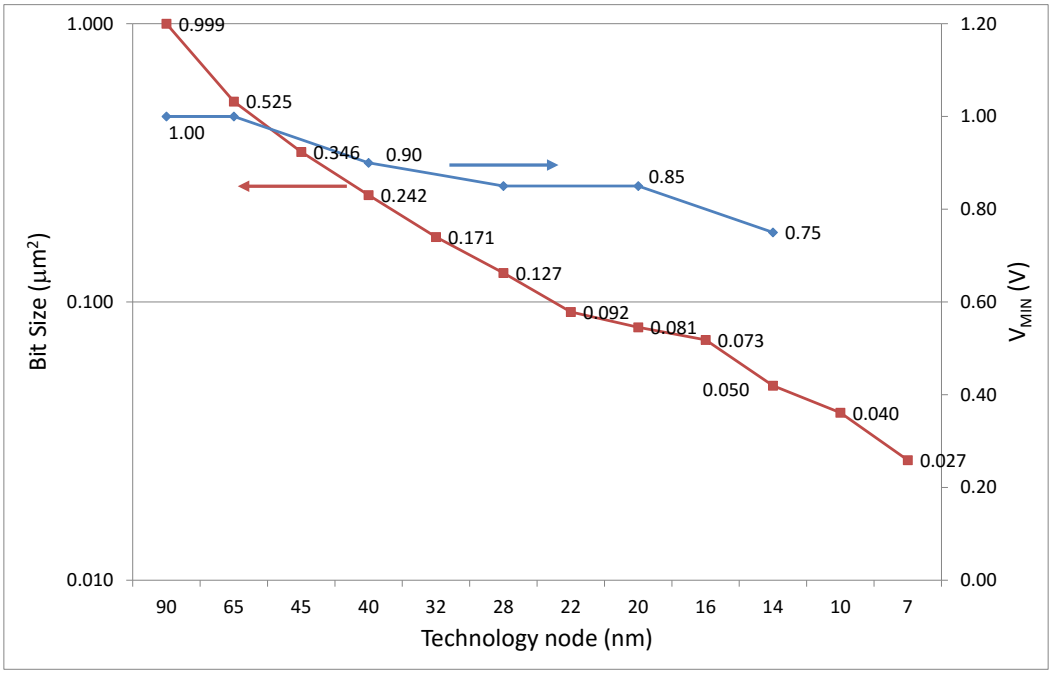

Figure 1 – Bit cell and V_{min} scaling trend of SRAM.

High-Bandwidth DRAM:

In order to maintain the optimal memory hierarchy ratio with respect to storage memory, DRAM continues to scale density, form factor, and bandwidth. This year, at ISCC 2017, benchmarks for the latest interface standards are presented, including GDDR5x for high-bandwidth, low-cost applications and LPDDR4x for low-power applications. Improvements are also demonstrated in very low standby power LPDDR4 DRAMs as well as next-generation transceivers based on time-based circuits and the MIPI C-PHY specification. In addition, a new L4 cache memory tier based on high-bandwidth, low-latency DRAM is shown. Figure 2 shows DRAM bandwidth scaling over the past decade.

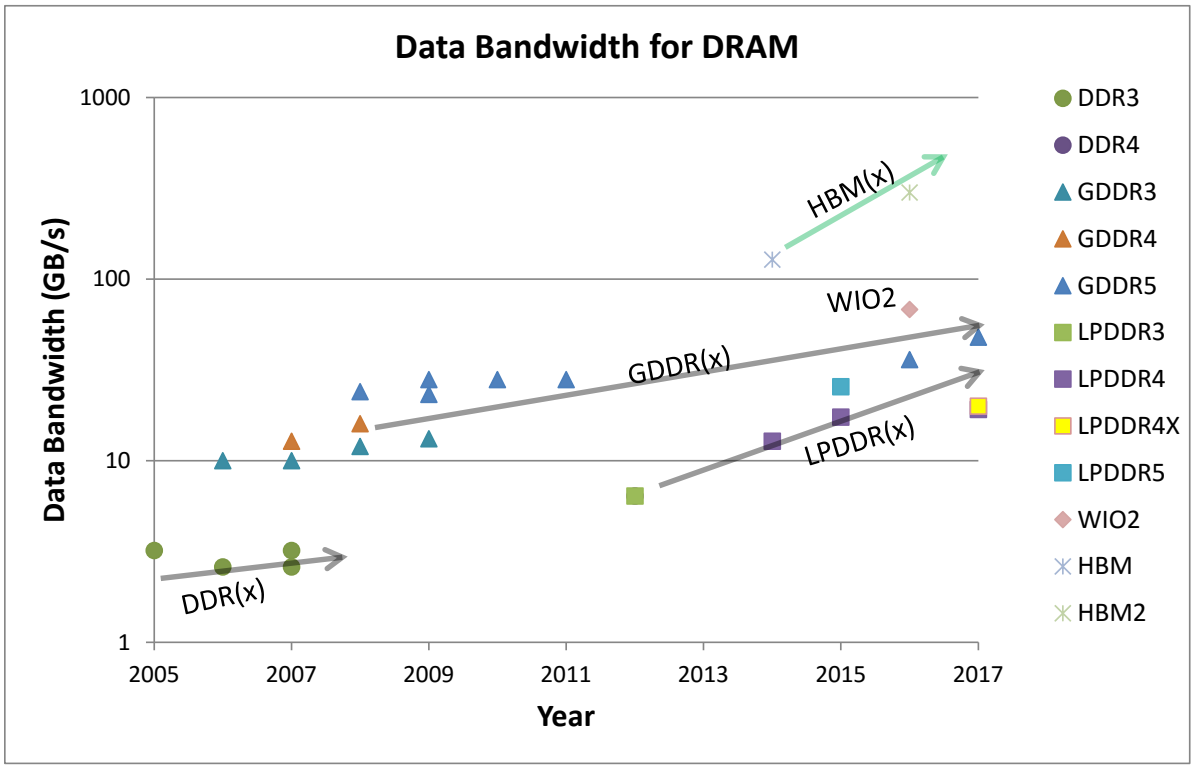

Figure 2 - DRAM data bandwidth trends.

Non-volatile Memories:

In the past decade, significant investment has been made in emerging memories field to find an alternative to floating-gate-based non-volatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (RRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights how 3b/cell (TLC) NAND Flash write throughput and a new STT-MRAM with LPDDR2 interface that continue to improve. Figure 4 shows a significant increase in NAND Flash capacity from 256Gb and 512Gb this year. Such high capacities are achieved through advancements in 3-dimensional vertical bit cell stacking technologies.

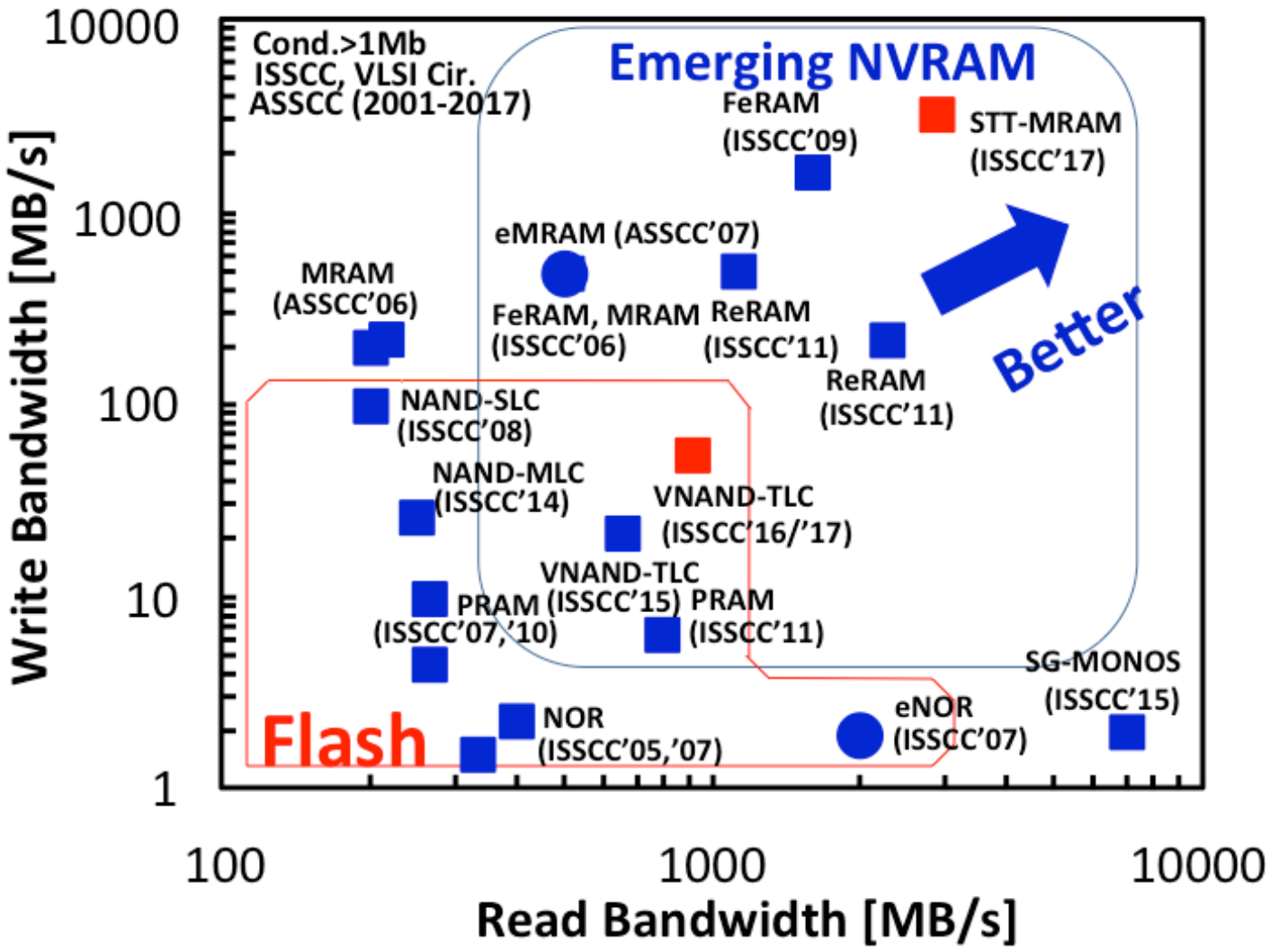

Figure 3 - Read/write bandwidth comparison of non-volatile memories.

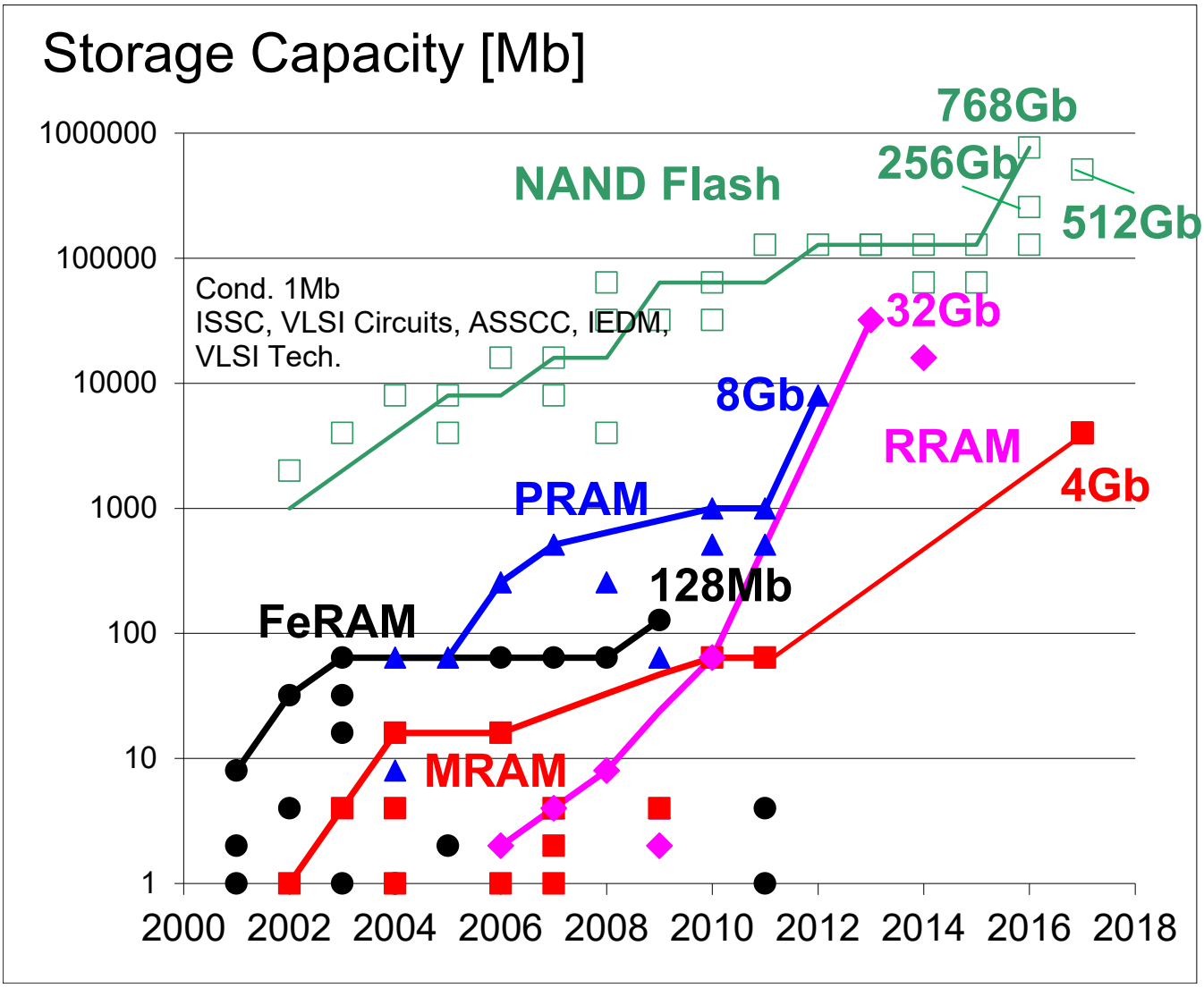

Figure 4 - Memory capacity trend of emerging non-volatile memories

NAND Flash Memory:

As seen at ISSCC 2017, NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). 3D memory technology becomes a mainstream for NAND Flash memory for the first time in mass-production of semiconductor industries. This year, two 512Gb 3b/cell 3D NANDs with 64 stacked WL layers are reported, continuing the trend to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. Not only higher density, but also high performance over 45MB/s program throughput and 1GB/s read throughput with lower I/O voltage from 1.8V to 1.2V. Figure 5 shows the observed trend in NAND Flash capacities at ISSCC over the past 20 years.

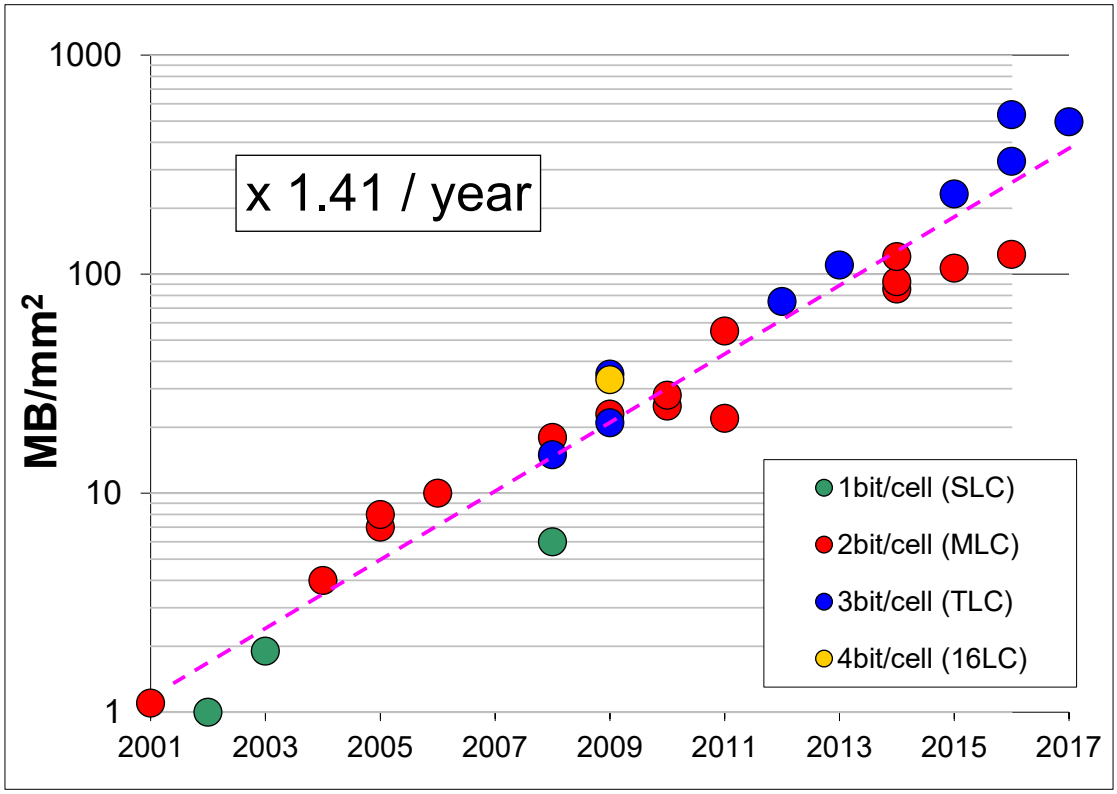

Figure 5 - NAND Flash memory trends.

HISTORICAL TRENDS IN TECHNICAL THEMES

INNOVATIVE TOPICS

IMAGERS/MEMS/MEDICAL/DISPLAYS SUBCOMMITTEE

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

IMMD – 2017 Trends (Sensors, MEMS & Displays)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Sensors are a key building block for the Internet of Everything. They collect the data and are an important part of the value chains that are enabling new services and fueling the need for more internet bandwidth. Increasingly, multiple sensors and their associated interface circuits are being combined on a single chip, or in a single package, allowing multi-parameter sensing and compensation for cross-sensitivity. Digital-centric implementations of sensor interfaces enable these improvements to be maintained in more advanced processes.

MEMS inertial sensors (accelerometer and gyroscopes) are key components used in a wide variety of consumer products, where low power consumption is a key requirement. For automotive applications, reduced vibration sensitivity and drift, but also high precision and reliability, are additional requirements. In addition to consumer applications, with continuing improvements in accuracy, stability and cost, MEMS inertial sensors have emerged as strong contenders for high-performance navigation and positioning-related applications. MEMS microphones continue to improve (the signal-to-noise ratio and linearity), while reducing the size of the sensor.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy and energy-efficiency, supporting wider applications. The new temperature sensors are shown to have accurate calibration on both plastic and ceramic packages.

In an effort to enlarge the application area of touch user interfaces, aside from performance enhancements in noisy environments, natural handwriting with stylus is becoming important to support with a capacitive touch controller. Styluses are classified into two categories: passive and active. Energy-efficient high-SNR readout circuits are required to support a fine tip passive stylus. New touch sensing architectures are being investigated to integrate active stylus functions, such as buttons, pressure, and tilt sensors, with capacitive touch sensors.

IMMD – 2017 Trends (Medical)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

As illustrated at ISSCC 2017, medical imaging is an important field with a growing number of applications. For improved capability and quality, medical ultrasound is moving toward 3D imaging with large arrays. As the number of transducer elements in arrays increases, the number of connections to the front-end circuitry is becoming a bottleneck. The same trend is obvious for the amount of signal processing needed. To resolve these congestions, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together for photoacoustic and volumetric imaging.

Sensors used for noninvasive monitoring of human body parameters, such as electrocardiogram (ECG), electroencephalogram (EEG), or bio-impedance are trending toward multimodal electrical/optical systems-on-chip (SoCs) to provide more holistic information about the state of health and consciousness of the subject. An interesting application for such an SoC is in accurate assessment of the depth of anesthesia in the operating room.

Both sensor and actuator systems for in-body implantable usage continue to evolve toward more robust and energy-efficient operation. New circuit concepts permit recording of weak biopotential signals in the presence of artifacts, paving the way toward autonomous, closed-loop systems that combine sensing, sense-making, and actuation as part of a single implantable device. This will allow therapy to be applied directly, for instance to suppress drug-resistant seizures without any involvement by the patient. Furthermore, technological approaches for wireless powering and bidirectional communication with these implantable devices continue to advance, with ultrasonic powering and communication gaining traction for deeply implanted devices.

IMMD – 2017 Trends (Imagers)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

The CMOS-image-sensor business remains one of the fastest-growing segments of the semiconductor industry. Key applications include cellphone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-video cameras, wearable devices, gaming and biomedical.

As seen at ISSCC 2017, the resolution and miniaturization races are ongoing but slowing down, and while the performance requirements stay constant, pixel size continues to scale down (see Figure 1). A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Wafer stacking of the image array on a CMOS image signal processor is becoming more common in mobile applications. A three-layer stacked CMOS image sensor with DRAM as a frame buffer has been reported for high-speed pixel readout. A high-speed vision chip with 3D-stacked column-parallel ADCs and 140GOPS programmable SIMD column-parallel PEs has been reported for spatio-temporal image processing.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions. A monolithic dynamic vision sensor supporting an event detection rate of 300M events per second has been reported.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. As well, global shutters are being introduced to avoid motion artifacts. A 2592×2054 imager with small pixels, low noise, wide dynamic range and global shutter has been demonstrated. Organic photoconductive film continues to make advances with electrically controllable IR sensitivity.

For precision scientific and medical applications, fluorescent lifetime imaging is extended to capture multiple exponential decays using 4-tap lock in pixel and shared pulse generator. Large pixels have been improved with increased conversion gain. A biochip with a fluorescence-based pixel array with an integrated excitation filter and on-chip heater is implemented for real-time amplicon-probe hybridization detection. We now employ single-photon avalanche diodes (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high-resolution, high-accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors (see Figure 1).

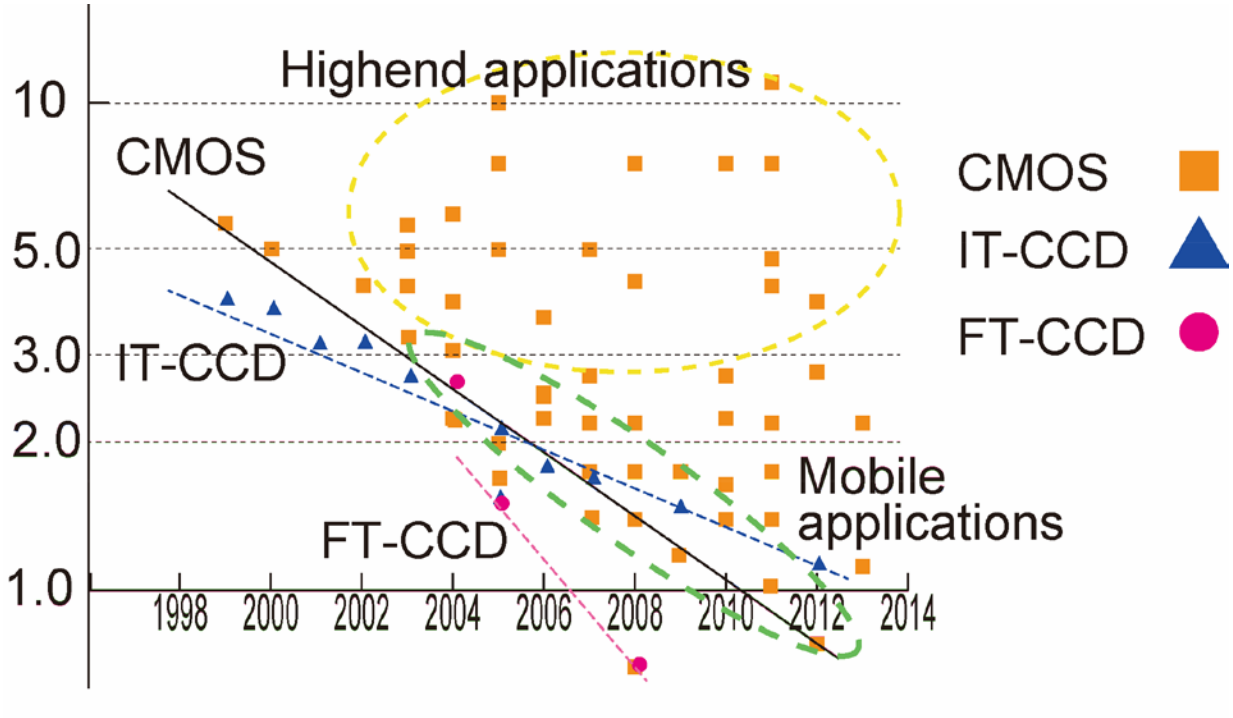

Figure 1: Pixel size trends (microns).

Technology Directions – 2017 Trends

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

Technology innovations bring the promise of enabling completely new system functionalities or substantially greater efficiency of existing ones. It is significant that harnessing such innovations for the solution of real-world problems requires thinking about technologies in the context of systems. Thus, now, with a focus on IoE, trends in Technology Directions emphasize the embedding of functionality in the real world. In this process, there must be a novel emphasis on both form factor and power management.

Large-area Electronics: Large-area electronics provide transformational form factors for electronic systems. The ability to create systems that are thin, form fitting, and capable of spanning large areas enables the integration of rich functionality within the real world. While materials and devices for large-area electronics began emerging well over a decade ago, demonstrations of systems addressing practical applications of societal importance have reached notable sophistication only in the past few years. This has required overcoming challenges on two important fronts: (1) the substantially lower performance of the devices compared with silicon CMOS, the workhorse technology of today; and (2) the role of key application drivers, and the architectures required to enable these.

With regards to the performance of devices, the field of large-area electronics has seen an evolution from amorphous-silicon, to organic, to metal-oxide semiconductors. An important source of this evolution has been a coupling with trends in the flat-panel display industry, where the demand for larger and higher performance displays has driven innovations and engineering refinement in the materials and fabrication methods for large-area technologies. With the flat-panel-display industry moving from amorphous-silicon to metal-oxide semiconductors, large-area thin-film transistors (TFTs) have benefitted from over an order of magnitude enhancement in mobility, from 1cm^2/Vs to well over 10cm^2/Vs. As illustrated at ISSCC 2017, activities in Technology Directions have focused on harnessing these gains far more broadly in displays, towards diverse IoE applications. This has necessitated careful thinking of the applications and systems architectures.

With regards to systems architectures, though designers now have the benefit of higher performance TFTs for implementing the range of functions required, the performance remains well below that of silicon CMOS. This raises important questions about how and which functions to selectively delegate to the large-area domain. While previous efforts in the systems space focused on demonstrating various blocks, including instrumentation amplifiers, ADCs, microprocessors, power converters, etc., today much more directed principles for designing large-area systems have emerged. This has brought selective and concerted focus on specific blocks, functionalities, and subsystems. ISSCC 2017 captures state-of-the-art thinking and demonstrations along these lines.

For example, this year's conference presents the first standard-compliant 13.56MHz NFC barcode tag in metal-oxide technology. This is enabled both by materials and processing enhancements at the TFT level and by careful circuit-level design. In another example, the conference presents clear progression in analog-to-digital converters, now achieving ENOB of 8b with input-signal bandwidth to 300Hz. This is enabled by an architecture for asynchronous delta-sigma modulation that eliminates high-rate input sampling and output bit-stream transitions. In addition, the conference presents a new architecture for large-scale acquisition of distributed large-area sensors to a silicon-CMOS IC, using frequency-hopping injection-locked TFT oscillators. This is enabled by a resonant LC oscillator topology, which exploits the ability to create high-frequency high-spectral-purity oscillations by exploiting high-quality passives (inductors) that can be fabricated in large-area technologies.

Drivers for Gallium-Nitride (GaN) Transistors: With silicon power transistors hitting limits in efficiency, speed, and power handling, wide bandgap semiconductors, most notably GaN, have taken over in applications where silicon leaves off. The past few years have seen a progression, with GaN devices becoming broadly available commercially and deployed in many applications. With this, Technology Directions has seen corresponding advancement in architectures for silicon-CMOS topologies used to drive these devices. This year, ISSCC 2017 offers two solutions in this direction: one addresses the critical issue of reducing EMI noise due to switching high currents at high frequencies by adaptive-slope gate drive control; another focuses on efficiency and fast switching using an integrated capacitor to form a resonant LC gate-drive structure.

INDEX

INDEX

A paper number mentioned in this section follows the convention S.P, where S is the session number and P is the paper number. For example 23.2 will be the second paper in the twenty-third session. You can refer back to the TECHNICAL SESSION OVERVIEWS in this Press Kit for additional details on any given paper. Some of the papers will also be available in the "not-so-technical" SESSION HIGHLIGHTS part of this Press Kit. All sessions and papers are in ascending order in both the Session Overviews and the Session Highlights sections of the Press Kit.

Technical Topics Mapped to Papers

Technical Topic	All papers in the following Sessions
Communication Systems includes Wireless, RF, and Wireline Subcommittees	**2, 6, 7, 13, 17, 18, 19, 24, 29**
Analog Systems includes Analog and Data Converter Subcommittees	**5, 10, 16, 22, 28**
Digital Systems includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees	**3, 8, 11, 12, 14, 20, 23, 26**
Innovative Topics includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees	**4, 9, 15, 21, 25, 27**

Selected Presenting Companies/Institution Mapped to Papers

Chart 4.1

Affiliation	Paper Numbers
Aalto University	13.4, 13.5
AMD	3.2
Ampleon	17.5
Analog Devices	5.7, 16.2, 16.7
ARM	5.6
ASIC North	12.4
AU Optronics	15.2
Ayar Labs	29.3
Boston University	29.3
Broadcom	2.2, 9.1, 28.6, 29.2
Brookman Technology	4.8
Canon	4.5
Carnegie Mellon University	19.3
Catena Microelectronics	9.9
CEA-LETI-MINATEC	7.5, 15.6, 17.8

Chung-Ang University	9.6
Cognionics	21.7
Columbia University	13.10, 17.2, 18.2, 19.4, 20.6, 24.2
CubeWorks	7.4, 14.7
Dartmouth College	10.2
Delft University of Technology	9.1, 9.3, 9.8, 9.9, 15.5, 17.5, 19.6, 24.1
DMCE	13.2
DPMA	13.2
Drexel University	26.2
Eindhoven University of Technology	15.3
Endura Technologies	3.4
EPFL	15.5, 29.1
Ericsson	7.2
ETH Zurich	27.4, 28.5, 29.3
ETH Zurich/University of Zurich	27.4
Fudan University	13.6
Fujitsu Laboratories	6.6, 6.7
Georgia Institute of Technology	2.1, 8.1, 13.8, 17.3, 17.7
Globalfoundries	12.4
Green Mountain Semiconductor	12.4
GSK (GlaxoSmithKline)	27.3
Hahn-Schickard	9.4
Hanyang University	9.6
Harvard University	14.3, 21.5
Hiroshima University	17.9
Hitachi	27.6
Hive Battery Management	10.2
Holst Centre / imec	5.3, 17.4, 24.1, 24.7
Holst Centre / TNO	15.3
Hong Kong University of Science and Technology	2.4, 5.11, 10.6, 20.5, 22.2, 22.8
Huawei Technologies	13.4
IBM	3.1, 26.2, 26.5
IBM Research	7.2, 12.4, 26.2, 29.1
IBM STG	26.2
IBM T. J. Watson Research Center	6.5, 7.2, 10.8
IBM Zurich Research Laboratory	28.5
IIT Madras	25.4, 29.6
imec	15.2, 24.7
Infineon Technologies	9.5
InSilixa	4.2
Institut Supérieur d'Electronique de Paris	15.5
Instituto Superior Tecnico	20.4, 20.5, 22.2, 22.4, 24.4
Instituto Superior Tecnico/University of Lisboa	16.4
Intel	3.3, 8.1, 10.2, 13.2, 13.6, 13.8, 13.9, 15.5, 20.1, 21.4, 23.9
Invensense	21.6
ITRI	23.9
KAIST	5.2, 10.4, 14.2, 14.6, 21.2, 27.2
Keysight Technologies	16.5

K-Healthwear	27.2
Kobe University	15.8
Korea University	29.5
Korea University Guro Hospital	27.2
KU Leuven	10.1, 14.5, 15.2
Leading UI	9.6
LG Display	29.5
Lund University	3.6
Marvell	5.10, 13.7
Massachusetts Institute of Technology	10.8, 14.4, 17.6, 21.1, 21.8, 29.3
MediaTek	2.5, 3.4, 7.1, 7.3, 7.6, 13.1, 17.1, 24.3, 28.1, 28.3
Micron	23.1
MiraeTNS	9.6
Movellus Circuits	13.6
National Chiao Tung University	2.3, 10.5, 14.8, 18.3, 20.2
National Institute of Information and Communications Technology	17.9
National Taiwan University	6.1, 14.8, 18.3
National Tsing Hua University	18.3
National University of Singapore	26.3
New York University	15.7, 21.7
Nokia	13.5
Novelda	7.7
NXP Semiconductors	5.1
Ohio State University	16.6
Oregon State University	29.4
Panasonic	4.7, 17.9
Pennsylvania State University	22.3
Piecemakers Technology	23.9
Pohang University of Science and Technology	5.5, 5.8, 8.2, 8.7, 23.7
Princeton University	15.1, 15.9, 27.8
Purdue University	21.3
Qualcomm	2.7
Qualcomm Atheros	6.2
Radiawave Technologies	13.6
Realtek Semiconductor	2.3, 10.5, 20.2
Renesas Electronics	3.5
Renesas System Design	3.5
Research Institute of Industrial Science & Technology	5.5
Reutlingen University	25.3
Rohm Semiconductor	24.7
Samsung Advanced Institute of Technology	4.1
Samsung Electronics	4.1, 8.7, 11.4, 12.2, 13.3, 23.2, 23.4, 23.6, 23.7, 24.8
Samsung Semiconductor	13.3, 24.8
Seoul National University	8.4, 29.7
Shizuoka University	4.3, 4.8
Sigfox	7.5
SK hynix	20.6, 23.3, 23.8, 29.7

SK hynix Semiconductor	23.5
Sony LSI Design	4.6, 4.9
Sony Semiconductor Manufacturing	4.6
Sony Semiconductor Solutions	4.6, 4.9
South China University of Technology	20.4, 22.4
Southern Methodist University	28.6
Stanford University	17.8, 21.8, 27.5, 27.7
STMicroelectronics	6.4, 14.1, 17.8, 27.5
Synopsys Macau Ltd	16.4, 20.4, 20.5, 22.4
Tampere University of Technology	13.5
Teledyne DALSA Semiconductors	5.1
Teledyne Scientific and Imaging	16.6
Texas A&M University	2.7, 21.4, 21.6
Texas Instruments	5.4, 25.1, 25.2, 25.4, 28.4
Tokyo Institute of Technology	8.5, 24.9
Toronto Western Hospital	27.3
Toshiba	11.1, 28.7
Toshiba Electronics Korea	23.5
TRAIS	9.7
Tsinghua University	15.5
TSMC	5.9, 11.2, 12.1, 19.6, 23.9
TSMC Design Technology	11.3, 12.1, 12.3
Ulm University	9.1
Ulsan National Institute of Science and Technology	19.2
University of Texas at Dallas	10.7, 22.5, 25.1, 25.2, 28.6
University College Dublin	19.6, 24.1
University of California, Berkeley	6.2, 6.3, 15.5, 21.1, 29.3
University of California, Davis	17.10
University of California, Irvine	19.1
University of California, Los Angeles	19.5, 22.7, 24.6, 27.1
University of California, San Diego	2.8, 20.3, 21.7, 24.5, 26.4
University of Electronic Science and Technology of China	28.6
University of Florida	28.2
University of Freiburg - IMTEK	9.4
University of Illinois	8.6, 10.3, 29.6
University of Lisbon	17.8
University of Macau	16.4, 20.4, 20.5, 22.2, 22.4, 24.4
University of Michigan	3.7, 4.4, 7.4, 8.3, 8.4, 9.2, 11.2, 14.7, 20.7, 21.6, 22.6
University of Nice	17.8
University of Oslo	7.7
University of Padova	13.9
University of Pavia	2.6, 6.4
University of Southampton	5.6, 22.1
University of Southern California	15.4
University of Texas	28.4
University of Tokyo	4.9
University of Toronto	6.6, 6.7, 27.3
University of Twente	24.3

University of Washington	18.1
Western Digital	11.1
Xilinx	6.3, 16.1, 16.3
Yonsei University	9.7, 23.8
York University	27.3
Zhejiang University	25.2

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