IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2015 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 22, 23, 24, 25, 26

CONFERENCE THEME:

SILICON SYSTEMS

SMALL CHIPS FOR BIG DATA

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR: ISSCCx

ISSCC PREVIEWS: CIRCUIT & SYSTEM INSIGHTS

SEE PAGE: 61

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: HIGH-SPEED INTERLEAVED ADCs; MEMORY TRENDS: BIG DATA TO WEARABLE

10 TUTORIALS: RF RECEIVERS; DRAM INTERFACES; ULTRA-LOW-POWER WIRELESS; NEAR-THRESHOLD DESIGN; HIGH-SPEED CURRENT-STEERING DACs; CLOCK & DATA RECOVERY; MANY-CORE PROCESSORS; NANO-POWER ANALOG; FREQUENCY SYNTHESIZERS; 3D IMAGING ICs

2 EVENING EVENTS ON GRADUATE STUDENT RESEARCH IN PROGRESS, ICs TALKING TO NEURONS

THURSDAY ALL-DAY

4 FORUMS: ADVANCES IN WIRELESS POWER; LOW POWER FOR IoE; RF TRANSMITTER ADVANCES; 10 @ 25Gb/s & MORE

SHORT-COURSE: CMOS LOW-VOLTAGE CIRCUIT DESIGN

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at thecutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 22nd**, the day before the official opening of the Conference, ISSCC 2015 offers:

- A choice of up to 4 of a total of 10 Tutorials
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, "**Brain-Machine Interfaces: ICs Talking to Neurons**" will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community.

On **Monday, February 23rd**, ISSCC 2015 offers three plenary papers on the theme: "**Silicon Systems - Small Chips for Big Data**". On Monday at 12:15 pm, there will be a Women's Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with the Book Display and Author Interviews, will also include a **Demonstration Session**, featuring posters and live demonstrations for selected papers from industry and academia. Monday evening will include 2 panel sessions on "**Moore's Law Challenges Below 10nm**…" and "**Lost Art? Neat Circuit Tricks with Fewer than a Dozen Transistors**".

On **Tuesday, February 24th**, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with the Book Display and Author Interviews, will also include a second **Demonstration Session**. Tuesday evening sessions include both a panel on "**Innovating on the Tapeout Treadmill**", as well as a Special-Topic Session on "**How to Achieve 1000× More Wireless-Data Capacity. 5G?**".

On **Wednesday, February 25th**, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On **Thursday, February 26th**, ISSCC offers a choice of five all-day events:

- A Short Course on "**Circuit Design in Advanced CMOS Techniques: How to Design with Lower Supply Voltages**"
- Four Advanced-Circuit-Design Forums on
  "Cutting the Last Wire - Advances in Wireless Power";
  "Building the Internet of Everything (IoE): Low-Power Techniques at the Circuit & Systems Level";
  "Advanced RF CMOS Transmitter Techniques ";
  "IO Design at 25Gb/s & Beyond".

Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

TABLE OF CONTENTS

T1: Fundamentals of Modern RF Receivers

To be compliant with multi-standard applications, the RF front-end of a modern transceiver must satisfy several challenging tasks such as large operative bandwidth, low noise, and high linearity. Over the years, addressing such requirements has significantly changed the radio architecture towards an ultimate solution based on current signal processing and passive mixers. In this tutorial, after a brief description of the typical structure of a receiver, the main properties that the radio must satisfy will be defined. After that, voltage and current signal processing will be compared showing why a fully current-mode approach is more suitable in deep-scale technologies. The tutorial will end by describing the most popular RF front-end architectures with a particular emphasis on the noise-canceling technique and the Class-AB solutions.

Instructor: Antonio Liscidini

Antonio Liscidini received the Laurea degree and Ph.D. in Electrical Engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006 respectively. He was a summer intern at National Semiconductor in 2003 (Santa Clara, CA) studying polyphase filters and CMOS LNAs. From 2008 to 2012 he was Assistant Professor at the University of Pavia and consultant for Marvell Semiconductor in the area of integrated circuit design. In December 2012 he joined the Edward S. Rogers Sr. Department of Electrical & Computer Engineering of the University of Toronto. His research interests are in the implementations of transceivers and frequency synthesizers for cellular and ultra-low-power applications.

T2: Basics of DRAM Interfaces

Memories have evolved continuously since the simple days of SDRAM. Back then, one interface standard was dominating and could be adapted to the different system needs. Now, one size no longer fits all. The number of DRAM standards is proliferating since different system environments require different, tailored DRAM-solutions. Examples are DDRn, GDDR5, HBM, LPDDRn, and WIOn. In this tutorial, we give an overview of these interface standards highlighting important details of the specifications, and describe selected design aspects and their system level implications.

Instructor: Martin Brox

Martin Brox received Dipl. and Dr. degrees from the University of Münster in 1988 and 1992. In 1988 he joined Siemens Corporate Research for a project to improve the modeling of hot-carrier degradation on CMOS-circuits. In 1992, he moved to the IBM/Siemens/Toshiba DRAM development alliance initially focusing on design, layout and test of DRAM mini-arrays and later DRAM-design. In 1997, he joined Siemens Semiconductor which later became Infineon and Qimonda where he was responsible for multiple commodity, RDRAM, GDDR3 and GDDR5 designs. In 2009 he joined Elpida (now part of Micron) as the lead design engineer for Micron's GDDR5 development.

T3: Ultra-Low-Power Wireless Systems

Emerging applications such as wearable devices, sensor networks and the 'internet of things' have to operate from very limited power budgets, and thus ultra-low-power operation is becoming increasingly important. This tutorial will address a range of issues that need to be considered in the design of ultra-low-power wireless systems. The tutorial will describe key features of low-power wireless standards such as BTSmart. We will then give an overview of architectures appropriate for very low power implementation including super-regenerative receivers, BAW-based architectures and direct modulation transmitters, and will outline the system trade-offs, which need to be considered for specific applications. We will then consider some key circuit building blocks required in the receiver, transmitter, and peripheral units and outline design techniques that are suitable for very low power implementation.

Instructor: Alison Burdett

Alison Burdett has over 25 years of experience in semiconductor design. She joined Toumaz in 2001 as Technical Director, and is currently responsible for delivering silicon and healthcare technology programs within the company. Prior to joining Toumaz, Alison spent time both in industry as an integrated circuit designer, and also in academia (as Senior Lecturer in Analogue IC Design at Imperial College London) Dr. Burdett is a Chartered Engineer, a Fellow of the Institute of Engineering and Technology (FIET) and a Senior Member of the IEEE. She is European Regional Chair of the Technical Program Committee for the IEEE International Solid State Circuits Conference (ISSCC), a member of the National Microelectronics Institute (NMI) Microelectronics Design Advisory Board, and a Visiting Researcher at the Institute of Biomedical Engineering, Imperial College.

T4: Low-Power Near-threshold Design

Digital circuit energy efficiencies plateaued due to stagnated voltage scaling in sub-90nm technologies. As a result, there is renewed interest in operating circuits at low supply voltages, such as near the device threshold voltage (referred to as near-threshold or NT design). NT operation offers a good balance between performance and energy efficiency, in contrast to sub-threshold design, which sacrifices performance for energy optimality. This tutorial offers design guidelines for near-threshold operation, particularly related to NT design robustness. Design examples from both academia and industry will highlight DSP accelerators, embedded memories, wide-range voltage scalable designs, and variability compensation strategies that scale to NT voltages.

Instructor: Dennis Sylvester

Dennis Sylvester received a Ph.D. from the University of California, Berkeley and is Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, MI. He has published over 375 articles along with one book and several book chapters, and holds 20 US patents. His research interests include the design of millimeter-scale computing systems and energy-efficient near-threshold computing. He is co-founder of Ambiq Micro, a fabless semiconductor company developing ultra-low-power mixed-signal solutions for compact wireless devices. He is an IEEE Fellow.

T5: High-Speed Current-Steering DACs

Among the various existing digital-to-analog converter (DAC) architectures, the current-steering DAC architecture prevails at high sampling rates. Its simple underlying topology makes these DACs well-suited for implementation in deep-submicron CMOS processes, where high-speed switches are readily available. The topological simplicity, however, comes with a substantial sensitivity to many sources of distortion. This tutorial first summarizes the basics of the current-steering architecture. Subsequently, it covers the various distortion mechanisms as well as the design techniques available to overcome their detrimental effects on DAC performance. Finally, measurement techniques required to assess the performance of the eventual DAC design are treated.

Instructor: Jan Mulder

Jan Mulder received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, The Netherlands, in 1994 and 1998, respectively. From 1998 to 2000, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He has published over 60 papers and holds more than 35 U.S. patents in circuit design. He served as an Associate Editor for IEEE Trans. on CAS-1 and is a member of the ISSCC ITPC.

T6: Clock and Data Recovery Architectures and Circuits

This tutorial provides ground theory and practical strategies for the design of clock-and-data-recovery circuits. We begin by relating performance metrics such as jitter transfer, jitter tolerance, and jitter peaking to CDR loop components and use these relationships to elucidate application-specific design challenges and tradeoffs. Following this, we will discuss both architectural- and circuit-level techniques to manage/overcome these tradeoffs. Specifically, we would compare different architectures: bang-bang vs. linear, digital vs. analog vs. hybrid loops, oscillator vs. phase interpolator, and reference-less vs. reference-based CDRs.

Instructor: Pavan Kumar Hanumolu

Pavan Kumar Hanumolu is an Associate Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, Corvallis, in 2006, where he subsequently served as a faculty member until 2013. Dr. Hanumolu's research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, wireline communication systems, and power conversion. He currently serves as an Associate Editor of the Journal of Solid-State Circuits, and is a technical program committee member of the VLSI Circuits Symposium, and International Solid-State Circuits Conference

T7: Basics of Many-Core Processors

This tutorial focuses on the design of many-core processors spanning clients to servers to high-performance computing systems in scaled CMOS process. Key circuits and design techniques are highlighted for robust and variation-tolerant logic, embedded memory arrays and on-die interconnect fabrics. Also presented are design principles that enable a wide dynamic voltage-frequency operating range, spanning multi-threaded high-throughput near-threshold voltage to single-threaded burst performance modes. Fine-grain multi-voltage design and power management techniques are covered, along with smart variation-aware workload mapping schemes to achieve maximum performance under stringent thermal and energy constraints. Real chip design examples are used to illustrate basic design principles and practical considerations.

Instructor: Vivek De

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long-term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 223 publications in refereed international conferences and journals and 195 patents, with 30 more patents filed (pending). He received an Intel Achievement Award for contributions to integrated voltage regulator technology. He received a Best Paper Award at the 1996 IEEE International ASIC Conference, and nominations for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC) and the 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference (DAC) as one of the "Top 10 Cited Papers in 50 Years of DAC". He received a Ph.D. in Electrical Engineering from Rensselaer Polytechnic Institute, Troy, New York. He is a Fellow of the IEEE.

T8: Analog Techniques for Nano-power Circuits

This tutorial presents the design methodology and examples of analog circuits having nanoampere consumption with application in systems with short activity periods followed long standby. They are essential for the area of energy harvesting where the amount of available energy can unpredictably change by orders of magnitude. Low load efficiency of power management becomes a very important parameter in a wide breadth of applications. Circuit examples include biasing, precision voltage references, oscillators, charge pumps, adaptive speed amplifiers and comparators, LDOs, DCDC converters.

Instructor: Vadim Ivanov

Vadim Ivanov received the MSEE and the Ph.D. in 1980 and 1987, respectively, both in the USSR. He designed electronic systems and ASICs for naval navigation equipment from 1980 to 1991 in St. Petersburg, Russia, and mixed-signal ASICs for sensors, GPS/GLONASS receivers and for motor control between 1991 and 1995. He joined Burr Brown (presently Texas Instruments, Tucson) in 1996 as a senior member of technical staff, where he has been involved in the design of the operational, instrumentation, power amplifiers, references, and switching and linear voltage regulators. He has over 80 US patents and applications on analog circuit techniques and authored over 30 technical papers and three books: "Power Integrated Amplifiers" (Leningrad, Rumb, 1987), "Analog system design using ASICs" (Leningrad, Rumb, 1988), both in Russian, and " Operational Amplifier Speed and Accuracy Improvement", Kluwer, 2004.

T9: Frequency Synthesizers for Wireless Transceivers

A frequency synthesizer is a key building block in wireless systems. The $\Delta\Sigma$ fractional-N PLL-based synthesizer plays a critical role in modern transceivers not only as a local oscillator but also as a phase modulator with direct digital modulation. However, the traditional PLL in advanced CMOS technology suffers from poor scalability, loop parameter variability, leakage current and linearity problems. Accordingly, diversified PLL architectures and circuit techniques have been recently proposed in consideration of performance, power and cost, thus making it more difficult than ever for circuit designers to choose the right design solution. This tutorial gives some insight into PLL basics tailored for circuit designers. Then, system perspectives and practical circuit design aspects for frequency synthesis will be presented.

Instructor: Woogeun Rhee

Woogeun Rhee is a Professor at Tsinghua University, China. He received the B.S. degree from Seoul National University in 1991, the M.S. degree from UCLA in 1993, and the Ph.D. degree from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, CA, where he was a Principal Engineer and developed low-power low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, NY and worked on clocking area for high-speed I/O serial links. In August 2006, he joined the faculty of Tsinghua University, China. He currently holds 19 U.S. patents.

T10: CMOS Sensors for 3D Imaging

3D imaging has become a hot research topic in the last few years, driven by the needs of emerging markets looking for next-generation user interfaces based on gesture control. Moreover, 3D vision systems offer amazing possibilities of improvement in many other areas like automotive, security and surveillance, cultural heritage preservation, ambient-assisted living, industrial control, etc., because they significantly increase the robustness of object classification with respect to conventional 2D imagers. This tutorial will introduce participants to the exciting field of 3D imaging, providing an overview about image-sensor architectures capable of distance measurement. An introduction to existing 3D imaging technologies will be given, addressing the peculiarities of each measuring technique and the possible application domains. The focus is on solid-state sensor architectures as enabling technologies to improve the performance of 3D vision systems, with a particular emphasis on time-of-flight implementations. Finally, participants will get some practical tools such as figure of merits and experimental characterizations guidelines for a comprehensive comparison of 3D imager performance and a perspective toward the future challenges in this fast-evolving field.

Instructor: David Stoppa

David Stoppa received the Ph.D. degree in Microelectronics from the University of Trento, Italy. He is the head of the Integrated Radiation and Image Sensors research unit at FBK where he has been working as a research scientist since 2002 and as group leader of the Smart Optical Sensors and Interfaces group from 2010 to 2013.. His research interests are in the field of CMOS image sensors and biosensors. He has published more than 100 papers, and holds several patents in the field of image sensors. He is currently a member of the ISSCC ITPC and was technical committee member of 'International Image Sensors Workshop' in 2009 and 2013. Dr. Stoppa received the 2006 ESSCIRC Best Paper Award.

F1: High-Speed Interleaved ADCs

Organizer: ***Stéphane Le Tual,*** *STmicroelectronics, Crolles, France*

Co-organizer: ***Borivoje Nikolic,*** *University of California, Berkeley, CA*

Committee: ***Tetsuya Iizuka,*** *University of Tokyo, Tokyo, Japan*
Ichiro Fujimori, *Broadcom, Irvine, CA*

Time-interleaved ADCs have become critical components in high-speed wireline and wireless communication systems. This forum will deliver a comprehensive treatment of state-of-the art design techniques for high-speed interleaved ADCs. Topics include transistor-level design techniques, calibration (estimation & correction), as well as the link between system specifications and required ADC performance.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	Introduction by Chair
8:30 AM	**Interleaved ADCs Through the Ages** ***Ken Poulton,*** *Keysight Laboratories, Santa Clara, CA*
9:20 AM	**Mismatch Error Correction for High-Resolution, GS/s time-Interleaved ADCs** ***Per Löwenborg,*** *Signal Processing Devices, Linköping, Sweden*
10:10 AM	Break
10:35 AM	**Highly Accurate Adaptive Digital Calibration for High-Speed High-Resolution Time-Interleaved ADCs** ***Takashi Oshima,*** *Hitachi, Tokyo, Japan*
11:25 AM	**ADC Interleaving Errors Corrected by Adaptive Post-Processing** ***Asad Abidi,*** *University of California, Los Angeles, CA*
12:15 PM	Lunch
1:20 PM	**Specifications vs. Applications: Driving Architectural Choices** ***Aaron Buchwald,*** *Entropic, Irvine, CA*
2:10 PM	**GS/s Time-Interleaved ADCs for Broadband Multi-Carrier Signal Reception** ***Kostas Doris,*** *NXP, Eindhoven, The Netherlands*
3:00 PM	Break
3:20 PM	**Embedded CMOS ADCs for Optical Communications** ***Yuriy M. Greshishchev,*** *Ciena, Ottawa, Canada*
4:10 PM	**Panel** Moderators: ***Bora Nikolic*** *(UC Berkeley)* ***Dave Robertson*** *(ADI)*
5:00 PM	Closing remarks by Chair

F2: Memory Trends: From Big Data to Wearable Devices

Organizer: ***Jonathan Chang,*** *TSMC, Hsinchu, Taiwan*

Committee: ***Jonathan Chang,*** *TSMC, Hsinchu, Taiwan*
Leland Chang, *IBM, Yorktown Heights, NY*
Antoine Dupret, *CEA Leti-LIST, Gif-sur-Yvette, France*
Chulwoo Kim, *Korea University, Seoul, Korea*
Fatih Hamzaoglu, *Intel, Hillsboro, OR*
Takefumi Yoshikawa, *Panasonic, Kyoto, Japan*

Memory continues to be a critical element in the full range of VLSI applications - from big data to mobile applications to wearable devices. Recent trends, including process technology scaling limits, new memory applications, and evolving high-performance and low-power requirements, have driven the development of emerging memories. As both discrete and embedded memory scaling becomes ever more challenging, there is a widespread effort to look for alternative memory technologies to replace the entrenched SRAM, DRAM, or Flash. This forum will bring together systems designers to discuss memory needs for future applications and memory designers to describe the latest developments in emerging and next generation memories.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction**
8:30 AM	**Memory Requirement Trends and Challenges: Servers to Devices** ***Suresh Chittor,*** *Intel, Hillsboro, OR*
9:20 AM	**Memory System Requirements for the Big-Data Application Data-Centric Computing** ***Ken Takeuchi,*** *Chuo University, Tokyo, Japan*
10:10 AM	Break
10:35 AM	**Memory and Storage Requirement and Trend for ChromeOS** ***Eric Shiu,*** *Google, Mountain View, CA*
11:25 AM	**Emerging Memories in Embedded Systems: Opportunities for the Digital Architect, Challenges for the Designers** ***Fabien Clermidy,*** *CEA-Leti, Grenoble, France*
12:15 PM	Lunch
1:20 PM	**3D NAND Flash: from Enterprise to Embedded Storages** ***Ki-Tae Park,*** *Samsung, Hwasung, Korea*
2:10 PM	**Addressing Future Memory Challenges with Device Abstraction** ***J. Thomas Pawlowski,*** *Micron, Boise, ID*
3:00 PM	Break
3:20 PM	**Technology Trends and Applications of MRAM from Big Data to Wearable Devices** ***Shinobu Fujita,*** *Toshiba, Kawasaki, Japan*
4:10 PM	**RRAM for Data Abundant System Technology: Managing Expectations and Minimizing Disappointments** ***Malgorzata Jurczak,*** *IMEC, Leuven, Belgium*
5:00 PM	Conclusion

ES1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 25 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Low-Power Data Converters and High-Speed Links; Biomedical Circuits and Systems; and Energy-Efficient Circuits for Sensors, RF, and Platform.

The Student Research Preview will begin with a brief talk by a distinguished member of the solid-state circuit community, Professor Emerita Lynn Conway of the University of Michigan, Ann Arbor.

Her remarks are scheduled for Sunday, February 22nd, starting at 7:30 pm. SRP is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel**	University of Pennsylvania, USA
Co-Chair:	**SeongHwan Cho**	KAIST, Korea
Co-Chair:	**Marian Verhelst**	Kath. University of Leuven, Belgium
Secretary:	**SeongHwan Cho**	KAIST, Korea
Advisor:	**Kenneth C. Smith**	University of Toronto, Canada
Media/Publications:	**Laura Fujino**	University of Toronto, Canada
A/V:	**John Trnka**	Rochester, MN

Committee Members

Bryan Ackland, Stevens Institute of Technology, USA
Andrea Baschirotto, University of Milan-Bicocca, Italy
William Bowhill, Intel, USA
SeongHwan Cho, KAIST, Korea
Denis Daly, Maxim Integrated, USA
Andreas Demosthenous, University College London, UK
Vincent Gaudet, University of Waterloo, Canada
Manish Goel, Samsung Electronics, USA
Chun-Huat Heng, National University of Singapore, Singapore
Makoto Ikeda, University of Tokyo, Japan
Jaeha Kim, Seoul National University, Korea
Tsung-Hsien Lin, National Taiwan University, Taiwan
Dejan Marković, University of California, Los Angeles, USA
Akira Matsuzawa, Tokyo Institute of Technology, Japan
Shahriar Mirabbasi, University of British Columbia, Canada
Tinoosh Mohsenin, University of Maryland, USA
Nils Pohl, Ruhr-University Bochum, Germany
Patrick Reynaert, University of Leuven, Belgium
Bing Sheu, TSMC, Taiwan
Sameer Sonkusale, Tufts University, USA
Jan Van der Spiegel, University of Pennsylvania, USA
Marian Verhelst, University of Leuven, Belgium
Jeffrey Weldon, Carnegie Mellon University, USA
GuoXing Wang, Shanghai Jiao Tong University, China
Peter (Chung-Yu) Wu, National Chiao Tung University, Taiwan

ES2: Brain-Machine Interfaces: Integrated Circuits Talking to Neurons

Organizer: ***Firat Yazicioglu,*** *IMEC, Leuven, Belgium*
Peng Cong, *Google, Mountain View, CA*
Shahriar Mirabbasi, *University of British Columbia, Vancouver, Canada*

Chair: ***Peng Cong,*** *Google, Mountain View, CA*
Shahriar Mirabbasi, *University of British Columbia, Vancouver, Canada*

We have not unlocked the three pounds of matter sitting in between our ears.

-Barack Obama

The brain is the most complex human organ, with energy efficiency far beyond that of any existing equivalent computing technology. Great efforts are being invested globally into deciphering its functioning. If successful, the resulting knowledge may forever change medical, consumer, and communications semiconductor industry sectors. A first significant challenge on the road towards this goal is the creation of instruments, generally enabled by integrated circuits, which can interact with a large number of the brain neurons and interpret such interactions.

This evening session will discuss technologies and circuit design solutions for connecting integrated circuits to neural circuits and will explore future application opportunities for such brain-machine interfaces. Experts in related technologies, circuit design, and applications from three continents will present an entertaining session on the impact of semiconductor technologies on medical applications and human-machine interaction.

Time	Topic
8:00 PM	**Neural Interfacing: Challenges and Opportunities for Circuit Designers** ***Tim Denison,*** *Medtronic, Minneapolis, MN*
8:25 PM	**CMOS Technology to Interface with Single Neurons and Axons** ***Andreas Hierlemann,*** *ETHZ, Zurich, Switzerland*
8:50 PM	**Circuits and Systems for Implantable Brain Monitoring** ***Jan Rabaey,*** *University of California, Berkeley, CA*
9:15 PM	**Neural Stimulation and Closed-Loop Prosthetics** ***Minkyu Je,*** *Daegu Gyeongbuk Institute of Science & Technology, Daegu, Korea*
9:40 PM	**Panel Discussions**

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair: ***Hoi-Jun Yoo,*** *KAIST, Daejeon, Korea*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 Silicon Technologies and Solutions for the Data-Driven World **8:45 AM**
Kinam Kim, *President, Samsung Electronics, Kiheung, Korea*

Silicon technology has been the core driver of the modern information revolution, forming the foundation on which electronics devices have been built. Advances in silicon-scaling technology have placed general-purpose computing in the palm of one's hand! Despite concerns for the demise of scaling, higher performance in electronic systems for the coming decades is expected, thanks to innovations in materials, structures, and processes. Performance-enhancing technologies, such as TSVs and 3D ICs, will drive the evolution of the fast-expanding data-driven world. As usual, these technological advances will breed new applications and new fields (Internet of Things, mobile healthcare, and others), all of which will catalyze explosive data growth. Both silicon and silicon-system technologies will need to evolve in order to conform to the future data-driven world. Future system-technology directions from the perspectives of servers, clients, and connectivity will also be discussed. Finally, issues associated with this data explosion (such as data security) will be presented.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:25 AM**

BREAK **9:55 AM**

1.2 The Future of IC Design Innovation **10:10 AM**
Sehat Sutardja, *Chairman and CEO, Marvell Technology Group, Santa Clara, CA*

One of the greatest achievements of humankind is undoubtedly our ability to build tiny machines that marry the functionalities of computers and wireless communication devices so cheaply that almost anyone in the world can afford them. Every one of us has at least one such device in our pocket, yet we rarely think about how in the world anyone could have created such a thing! Even the experts in our industry could not have predicted that this would have happened so soon. What we have achieved could be considered nothing short of a miracle, considering that billions of transistors have to work together flawlessly. (Well, sort of.) The reality is that some of these devices are now so complex that we need thousands of engineers for design, validation, and support, which inevitably causes inefficiencies and bugs. Sadly, the way we build these devices has not changed much over the past decades. Integrated-circuit design engineers blindly do what they are told to – integrate as much functionality into a single device, believing that more is better! This more- the-better mentality is not surprising because we saw in the past that the more we integrate, the cheaper things would become. Unfortunately, times have changed. The cost and complexity of building billions of transistors on a single device is finally taking a toll on our engineers. If chip-design engineers had also looked at the financial optimization of the overall design process, they would have built things differently. They should have realized that certain functions are better grouped into highly specialized integrated circuits that could easily and seamlessly talk to each other without compromising the overall system cost. The key to making this happen is what I call the Lego-Block approach of designing integrated circuits. However, in order for the Lego-Block approach to materialize, we need to change the way we architect our devices.

We need to do many things: Define a new chip-to-chip interconnect protocol; take advantage of multi-chip-module packaging and high-speed SerDes technology; redefine the memory hierarchy to take advantage of 3D solid-state memory instead of blindly increasing the DRAM size in our devices; repartition DRAM to serve different logical functions instead of building gigantic single-die DRAM to serve every function; change the way we build DRAMs so that they are optimized more for performance and power efficiency instead of capacity; and redefine what should be done in hardware versus software. In short, we need to change our way of thinking, and be brave enough to reject common wisdom. If we fail to take action, soon we will no longer see cost savings. On the other hand, if we succeed, we will see life beyond the end of Moore's Law!

1.3 Analog CMOS from 5 Micrometer to 5 Nanometer **10:50 AM**

Willy Sansen, *Professor Emeritus, Katholieke Universiteit Leuven, Leuven, Belgium*

Since the early years of analog design in CMOS, expertise has been focused on building blocks, with emphasis on trade-offs among speed, noise, and power consumption. But, present application systems (such as mobile SoC, Internet-of-Things, automotive, biomedical, FPGA interfaces), all require mixed-signal design and digitally-assisted analog. "How much analog has to be combined with how much digital?" is an open question.

This presentation will look back briefly through the history of CMOS analog design and give a projection on how analog may look in future Nanometer CMOS. In these new technologies, the supply voltage keeps on shrinking, making offset and 1/f noise even more important than before.

Nowadays, analog techniques all aim at the cancellation of resistances, to save power. They also try to cancel capacitances, to enhance speed. As well, cancellation of noise and distortion have become commonplace. Such cancellation techniques will be reviewed and compared. In parallel, several technologies such as FinFETs and FD-SOI, are in competition for future Nanometer design. Below gate lengths of 10nm, materials other than Silicon, such as Germanium, need to be considered. Also Nanowires and Nanotubes have become viable candidates for Nanometer Analog.

PRESENTATION TO PLENARY SPEAKERS **11:30 AM**

CONCLUSION **11:35 AM**

RF TX/RX Design Techniques

Session Chair: ***Ehsan Afshari,*** *Cornell University, Ithaca, NY*
Associate Chair: ***Minoru Fujishima,*** *Hiroshima University, Hiroshima, Japan*

2.1 **A Highly Linear Inductorless Wideband Receiver with Phase- and Thermal-Noise Cancellation** **1:30 PM**
H. Wu[1,2], M. Mikhemar[2], D. Murphy[2], H. Darabi[2], M-C. F. Chang[1]
[1]University of California, Los Angeles, CA; [2]Broadcom, Irvine, CA

2.2 **A +70dBm IIP3 Single-Ended Electrical-Balance Duplexer in 0.18µm SOI CMOS** **2:00 PM**
B. van Liempd[1], B. Hershberg[1], K. Raczkowski[1], S. Ariumi[2], U. Karthaus[3], K-F. Bink[3], J. Craninckx[1]
[1]imec, Leuven, Belgium; [2]Murata, Kyoto, Japan
[3]HiSilicon, Leuven, Belgium

2.3 **A 130-to-180GHz 0.0035mm² SPDT Switch with 3.3dB Loss and 23.7dB Isolation in 65nm Bulk CMOS** **2:15 PM**
F. Meng[1], K. Ma[1], K. S. Yeo[1,2]
[1]Nanyang Technological University, Singapore, Singapore
[2]Singapore University of Technology and Design, Singapore, Singapore

2.4 **A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF** **2:30 PM**
Z. Lin[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico, Lisbon, Portugal

2.5 **A 2-to-6GHz Class-AB Power Amplifier with 28.4% PAE in 65nm CMOS Supporting 256QAM** **2:45 PM**
W. Ye[1], K. Ma[1], K. S. Yeo[1,2]
[1]Nanyang Technological University, Singapore, Singapore
[2]Singapore University of Technology and Design, Singapore, Singapore

Break **3:00 PM**

2.6 **Class-O: A Highly Linear Class of Power Amplifiers in 0.13µm CMOS for WCDMA/LTE Applications** **3:15 PM**
A. F. Aref, R. Negra, M. Abdullah Khan
RWTH Aachen University, Aachen, Germany

2.7 **A Hybrid Supply Modulator with 10dB ET Operation Dynamic Range Achieving a PAE of 42.6% at 27.0dBm PA Output Power** **3:45 PM**
S-C. Lee, J-S. Paek, J-H. Jung, Y-S. Youn, S-J. Lee, M-S. Cho, J-J. Han, J-H. Choi, Y-W. Joo, T. Nomiyama, S-H. Lee, I-Y. Sohn, T. B. Cho, B-H. Park, I. Kang
Samsung Electronics, Hwaseong, Korea

2.8 **A Broadband CMOS Digital Power Amplifier with Hybrid Class-G Doherty Efficiency Enhancement** **4:15 PM**
S. Hu[1], S. Kousai[2], H. Wang[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Toshiba, Kawasaki, Japan

2.9 **A 29dBm 18.5% Peak PAE mm-Wave Digital Power Amplifier with Dynamic Load Modulation** **4:45 PM**
K. Datta, H. Hashemi, University of Southern California, Los Angeles, CA

2.10 **A 60GHz 28nm UTBB FD-SOI CMOS Reconfigurable Power Amplifier with 21% PAE, 18.2dBm P_{1dB} and 74mW P_{DC}** **5:00 PM**
A. Larie[1,2], E. Kerhervé[2], B. Martineau[1,3], L. Vogt[1], D. Belot[1,3]
[1]STMicroelectronics, Crolles, France
[2]University of Bordeaux, Talence, France
[3]CEA-LETI-MINATEC, Grenoble, France

Conclusion **5:15 PM**

Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links

Session Chair: ***Ken Chang,*** *Xilinx, San Jose, CA*
Associate Chair: ***Shunichi Kaeriyama,*** *Renesas, Tokyo, Japan*

3.1 **A 28Gb/s Multi-Standard Serial-Link Transceiver for Backplane Applications in 28nm CMOS** — **1:30 PM**
B. Zhang, K. Khanoyan, H. Hatamkhani, H. Tong, K. Hu, S. Fallahi , K. Vakilian, A. Brewster
Broadcom, Irvine, CA

3.2 **Multi-Standard 185fs$_{rms}$ 0.3-to-28Gb/s 40dB Backplane Signal Conditioner with Adaptive Pattern-Match 36-Tap DFE and Data-Rate-Adjustment PLL in 28nm CMOS** — **2:00 PM**
T. Kawamoto[1], T. Norimatsu[1], K. Kogo[1], F. Yuki[1], N. Nakajima[2], M. Tsuge[2], T. Usugi[2], T. Hokari[2], H. Koba[2], T. Komori[2], J. Nasu[2], T. Kawamata[2], Y. Ito[2], S. Umai[2], J. Kumazawa[2], H. Kurahashi[2], T. Muto[2], T. Yamashita[2], M. Hasegawa[2], K. Higeta[2]
[1]Hitachi, Tokyo, Japan
[2]Hitachi, Kanagawa, Japan

3.3 **DS1** **A 0.5-to-32.75Gb/s Flexible-Reach Wireline Transceiver in 20nm CMOS** — **2:30 PM**
P. Upadhyaya, J. Savoj, F-T. An, A. Bekele, A. Jose, B. Xu, D. Wu, D. Turker, H. Aslanzadeh, H. Hedayati, J. Im, S-W. Lim, S. Chen, T. Pham, Y. Frans, K. Chang
Xilinx, San Jose, CA

Break — **3:00 PM**

3.4 **A 36Gb/s PAM4 Transmitter Using an 8b 18GS/s DAC in 28nm CMOS** — **3:15 PM**
A. Nazemi, K. Hu, B. Catli, D. Cui, U. Singh, T. He, Z. Huang, B. Zhang, A. Momtaz, J. Cao
Broadcom, Irvine, CA

3.5 **A 16-to-40Gb/s Quarter-Rate NRZ/PAM4 Dual-Mode Transmitter in 14nm CMOS** — **3:45 PM**
J. Kim, A. Balankutty, A. Elshazly, Y-Y. Huang, H. Song, K. Yu, F. O'Mahony
Intel, Hillsboro, OR

3.6 **A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS** — **4:00 PM**
A. Shafik, E. Zhian Tabasy, S. Cai, K. Lee, S. Hoyos, S. Palermo
Texas A&M University, College Station, TX

3.7 **A 7Gb/s Rapid On/Off Embedded-Clock Serial-Link Transceiver with 20ns Power-On Time, 740µW Off-State Power for Energy-Proportional Links in 65nm CMOS** — **4:15 PM**
T. Anand[1], M. Talegaonkar[1], A. Elkholy[1], S. Saxena[1], A. Elshazly[2], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL
[2]Intel, Hillsboro, OR

3.8 **A 0.45-to-0.7V 1-to-6Gb/s 0.29-to-0.58pJ/b Source-Synchronous Transceiver Using Automatic Phase Calibration in 65nm CMOS** — **4:45 PM**
W-S. Choi[1], G. Shu[1], M. Talegaonkar[1], Y. Liu[1], D. Wei[1], L. Benini[2], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL
[2]University of Bologna, Bologna, Italy

Conclusion — **5:15 PM**

Processors

Session Chair: ***Atsuki Inoue,*** *Fujitsu, Kawasaki, Japan*
Associate Chair: ***Luke (Jinuk) Shin,*** *Oracle, Redwood Shores, CA*

4.1 **22nm Next-Generation IBM System z Microprocessor** **1:30 PM**
J. Warnock[1], B. Curran[2], J. Badar[3], G. Fredeman[2], D. Plass[2], Y. Chan[2], S. Carey[2], G. Salem[4], F. Schroeder[5], F. Malgioglio[2], G. Mayer[5], C. Berry[2], M. Wood[2], Y-H. Chan[2], M. Mayo[2], J. Isakson[3], C. Nagarajan[6], T. Werner[5], L. Sigal[7], R. Nigaglioni[3], M. Cichanowski[3], J. Zitz[8], M. Ziegler[7], T. Bronson[3], G. Strevig[3], D. Dreps[3], R. Puri[7], D. Malone[2], D. Wendel[5], P-K. Mak[2], M. Blake[2]
[1]IBM Systems and Technology, Yorktown Heights, NY
[2]IBM Systems and Technology, Poughkeepsie, NY
[3]IBM Systems and Technology, Austin, TX
[4]IBM Systems and Technology, Williston, VT
[5]IBM Systems and Technology, Boeblingen, Germany
[6]IBM Systems and Technology, Bangalore, India
[7]IBM Research, Yorktown Heights, NY
[8]IBM Systems and Technology, Hopewell Junction, NY

4.2 **A 20nm 32-Core 64MB L3 Cache SPARC M7 Processor** **2:00 PM**
P. Li, J. L. Shin, G. Konstadinidis, F. Schumacher, V. Krishnaswamy, H. Cho, S. Dash, R. Masleid, C. Zheng, Y. D. Lin, P. Loewenstein, H. Park, V. Srinivasan, D. Huang, C. Hwang, W. Hsu, C. McAllister
Oracle, Redwood Shores, CA

4.3 **Fine-Grained Adaptive Power Management of the SPARC M7 Processor** **2:30 PM**
V. Krishnaswamy, J. Brooks, G. Konstadinidis, C. McAllister, H. Pham, S. Turullols, J. L. Shin, Y. YangGong, H. Zhang
Oracle, Redwood Shores, CA

4.4 **DS1** **Energy-Efficient Microserver Based on a 12-Core 1.8GHz 188K-CoreMark 28nm Bulk CMOS 64b SoC for Big-Data Applications with 159GB/s/L Memory Bandwidth System Density** **2:45 PM**
R. Luijten[1], D. Pham[2], R. Clauberg[1], M. Cossale[1], H. N. Nguyen[2], M. Pandya[2]
[1]IBM Research, Rüschlikon, Switzerland
[2]Freescale Semiconductor, Austin, TX

Break **3:00 PM**

4.5 **DS1** **The Xeon® Processor E5-2600 v3: A 22nm 18-Core Product Family** **3:15 PM**
B. Bowhill[1], B. Stackhouse[2], N. Nassif[1], Z. Yang[1], A. Raghavan[1], C. Morganti[2], C. Houghton[1], D. Krueger[2], O. Franza[1], J. Desai[2], J. Crop[2], D. Bradley[2], C. Bostak[2], S. Bhimji[1], M. Becker[1]
[1]Intel, Hudson, MA; [2]Intel, Fort Collins, CO

4.6 **A 1.93TOPS/W Scalable Deep Learning/Inference Processor with Tetra-Parallel MIMD Architecture for Big-Data Applications** **3:45 PM**
S. Park, K. Bong, D. Shin, J. Lee, S. Choi, H-J. Yoo, KAIST, Daejeon, Korea

4.7 **A 409GOPS/W Adaptive and Resilient Domino Register File in 22nm Tri-Gate CMOS Featuring In-Situ Timing Margin and Error Detection for Tolerance to Within-Die Variation, Voltage Droop, Temperature and Aging** **4:15 PM**
J. P. Kulkarni, C. Tokunaga, P. Aseron, T. Nguyen Jr, C. Augustine, J. Tschanz, V. De
Intel, Hillsboro, OR

4.8 **DS1** **A 28nm x86 APU Optimized for Power and Area Efficiency** **4:45 PM**
K. Wilcox[1], D. Akeson[1], H. R. Fair III[1], J. Farrell[1], D. Johnson[2], G. Krishnan[1], H. McIntyre[3], E. McLellan[1], S. Naffziger[2], R. Schreiber[4], S. Sundaram[4], J. White[1]
[1]AMD, Boxborough, MA; [2]AMD, Fort Collins, CO
[3]AMD, Sunnyvale, CA; [4]AMD, Austin, TX

Conclusion **5:15 PM**

Analog Techniques

Session Chair: ***Xicheng Jiang,*** *Broadcom, Irvine, CA*
Associate Chair: ***Ed (Adrianus JM) van Tuijl,*** *University of Twente, Enschede, The Netherlands*

5.1 **A 60V Auto-zero and Chopper Operational Amplifier with 800kHz Interleaved Clocks and Input Bias-Current Trimming** — **1:30 PM**
Y. Kusuda, Analog Devices, San Jose, CA

5.2 **A 110dB SNR ADC with ±30V Input Common-Mode Range and 8μV Offset for Current Sensing Applications** — **2:00 PM**
L. Xu[1], B. Gönen[1], Q. Fan[2], J. H. Huijsing[1], K. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Maxim Integrated Products, Delft, The Netherlands

5.3 **A 2-Channel -83.2dB Crosstalk 0.061mm² CCIA with an Orthogonal Frequency Chopping Technique** — **2:30 PM**
Y-L. Tsai, F-W. Lee, T-Y. Chen, T-H. Lin
National Taiwan University, Taipei, Taiwan

5.4 **A 32nW Bandgap Reference Voltage Operational from 0.5V Supply for Ultra-Low Power Systems** — **2:45 PM**
A. Shrivastava, K. Craig, N. E. Roberts, D. D. Wentzloff, B. H. Calhoun
PsiKick, Charlottesville, VA

Break — **3:00 PM**

5.5 **A Forward-Body-Bias Tuned 450MHz Gm-C 3rd-Order Low-Pass Filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7-to-1V Supply** — **3:15 PM**
J. Lechevallier[1,2], R. Struiksma[1], H. Sherry[2], A. Cathelin[2], E. Klumperink[1], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands
[2]STMicroelectronics, Crolles, France

5.6 **A 0.13μm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range** — **3:45 PM**
S. B. Nasir, S. Gangopadhyay, A. Raychowdhury
Georgia Institute of Technology, Atlanta, GA

5.7 **A 29nW Bandgap Reference Circuit** — **4:15 PM**
J. M. Lee[1], Y. Ji[1], S. Choi[1], Y-C. Cho[2], S-J. Jang[2], J. S. Choi[2], B. Kim[1], H-J. Park[1], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

5.8 **A Digitally Assisted Single-Point-Calibration CMOS Bandgap Voltage Reference with a 3σ Inaccuracy of ±0.08% for Fuel-Gauge Applications** — **4:30 PM**
G. Maderbacher, S. Marsili, M. Motz, T. Jackum, J. Thielmann, H. Hassander, H. Gruber, F. Hus, C. Sandner
Infineon Technologies, Villach, Austria

5.9 **A 37μW Dual-Mode Crystal Oscillator for Single-Crystal Radios** — **4:45 PM**
D. Griffith[1], J. Murdock[1], P. T. Røine[2], T. Murphy[1]
[1]Texas Instruments, Dallas, TX; [2]Texas Instruments, Oslo, Norway

5.10 **A 4.7MHz 53μW Fully Differential CMOS Reference Clock Oscillator with –22dB Worst-Case PSNR for Miniaturized SoCs** — **5:00 PM**
J. Lee[1], P. Park[1], S. Cho[2], M. Je[3]
[1]Institute of Microelectronics, Singapore, Singapore
[2]KAIST, Daejeon, Korea
[3]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

Conclusion — **5:15 PM**

Image Sensors and Displays

Session Chair: ***Yusuke Oike,*** *Sony, Atsugi, Japan*
Associate Chair: ***Young-Sun Na,*** *LG Electronics, Seoul, Korea*

6.1 **A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications** — **1:30 PM**
A. Suzuki[1], N. Shimamura[1], T. Kainuma[1], N. Kawazu[1], C. Okada[1], T. Oka[1], K. Koiso[2], A. Masagaki[1], Y. Yagasaki[3], S. Gonoi[4], T. Ichikawa[1], M. Mizuno[5], T. Sugioka[1], T. Morikawa[1], Y. Inada[1], H. Wakabayashi[1]
[1]Sony, Atsugi, Japan
[2]Sony Semiconductor, Kikuyou, Japan
[3]Sony, Shinagawa, Japan
[4]Sony LSI Design, Fukuoka, Japan
[5]Sony LSI Design, Atsugi, Japan

6.2 **133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs** — **2:00 PM**
R. Funatsu[1], S. Huang[2], T. Yamashita[1], K. Stevulak[2], J. Rysinski[2], D. Estrada[2], S. Yan[2], T. Soeno[1], T. Nakamura[1], T. Hayashida[1], H. Shimamoto[1], B. Mansoorian[2]
[1]NHK Science & Technology Research Laboratories, Tokyo, Japan
[2]Forza Silicon, Pasadena, CA

6.3 **A 45.5μW 15fps Always-On CMOS Image Sensor for Mobile and Wearable Devices** — **2:30 PM**
J. Choi, J. Shin, D. Kang, D-S. Park
Samsung Advanced Institute of Technology, Suwon, Korea

Break — **3:00 PM**

6.4 **Single-Shot 200Mfps 5×3-Aperture Compressive CMOS Imager** — **3:15 PM**
F. Mochizuki[1], K. Kagawa[1], S-I. Okihara[2], M-W. Seo[1], B. Zhang[1], T. Takasawa[1], K. Yasutomi[1], S. Kawahito[1]
[1]Shizuoka University, Hamamatsu, Japan
[2]The Graduate School for the Creation of New Photonics Industries, Hamamatsu, Japan

6.5 **25.3μW at 60fps 240×160-Pixel Vision Sensor for Motion Capturing with In-Pixel Non-Volatile Analog Memory Using Crystalline Oxide Semiconductor FET** — **3:45 PM**
T. Ohmaru[1], T. Nakagawa[1], S. Maeda[1], Y. Okamoto[1], M. Kozuma[1], S. Yoneda[1], H. Inoue[1], Y. Kurokawa[1], T. Ikeda[1], Y. Ieda[1], N. Yamade[1], H. Miyairi[1], M. Ikeda[2], S. Yamazaki[1]
[1]Semiconductor Energy Laboratory, Kanagawa, Japan
[2]University of Tokyo, Tokyo, Japan

6.6 **DS1** **A 240Hz-Reporting-Rate Mutual-Capacitance Touch-Sensing Analog Front-End Enabling Multiple Active/Passive Styluses with 41dB/32dB SNR for 0.5mm Diameter** — **4:00 PM**
M. Hamaguchi, M. Takeda, M. Miyamoto
SHARP, Tenri, Japan

6.7 **A 2.3mW 11cm-Range Bootstrapped and Correlated-Double-Sampling (BCDS) 3D Touch Sensor for Mobile Devices** — **4:15 PM**
L. Du, Y. Zhang, F. Hsiao, A. Tang, Y. Zhao, Y. Li, Z-Z. Chen, L. Huang, M-C. F. Chang
University of California, Los Angeles, CA

6.8 **A Pen-Pressure-Sensitive Capacitive Touch System Using Electrically Coupled Resonance Pen** — **4:45 PM**
C. Park[1,2], S. Park[2], K-D. Kim[1], S. Park[1], J. Park[2], Y. Huh[1], B. Kang[2], G-H. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Suwon, Korea

Conclusion — **5:15 PM**

Demonstration Session 1, Monday February 23rd, 4:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 23rd, and Tuesday February 24th, from 4 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2015, as noted by the symbol **DS1**

Monday, February 23rd

3.3	A 0.5-to-32.75Gb/s Flexible-Reach Wireline Transceiver in 20nm CMOS	2:30 PM
4.4	Energy-Efficient Microserver Based on a 12-Core 1.8GHz 188K-CoreMark 28nm Bulk CMOS 64b SoC for Big-Data Applications with 159GB/s/L Memory Bandwidth System Density	2:45 PM
4.5	The Xeon® Processor E5-2600 v3: A 22nm 18-Core Product Family	3:15 PM
4.8	A 28nm x86 APU Optimized for Power and Area Efficiency	4:45 PM
6.6	A 240Hz-Reporting-Rate Mutual-Capacitance Touch-Sensing Analog Front-End Enabling Multiple Active/Passive Styluses with 41dB/32dB SNR for 0.5mm Diameter	4:00 PM

Tuesday, February 24th

7.7	Enterprise-Grade 6× Fast Read and 5× Highly Reliable SSD with TLC NAND-Flash Memory for Big-Data Storage	11:45 AM
8.2	Batteryless Sub-nW Cortex-M0+ Processor with Dynamic Leakage-Suppression Logic	9:00 AM
9.7	An LTE SAW-Less Transmitter Using 33% Duty-Cycle LO Signals for Harmonic Suppression	11:45 AM
10.1	A 6Gb/s 6pJ/b 5mm-Distance Non-Contact Interface for Modular Smartphones Using Two-Fold Transmission-Line Coupler and EMC-Qualified Pulse Transceiver	8:30 AM
10.2	An FSK Plastic Waveguide Communication Link in 40nm CMOS	9:00 AM
10.3	A 7.5mW 7.5Gb/s Mixed NRZ/Multi-Tone Serial-Data Transceiver for Multi-Drop Memory Interfaces in 40nm CMOS	9:30 AM
11.1	A Time-Divided Spread-Spectrum Code Based 15pW-Detectable Multi-Channel fNIRS IC for Portable Functional Brain Imaging	8:30 AM
11.3	A 160×120-Pixel Analog-Counting Single-Photon Imager with Sub-ns Time-Gating and Self-Referenced Column-Parallel A/D Conversion for Fluorescence Lifetime Imaging	9:30 AM
11.8	Integrated Ultrasonic System for Measuring Body-Fat Composition	12:00 PM
12.6	90% Peak Efficiency Single-Inductor-Multiple-Output DC-DC Buck Converter with Output Independent Gate Drive Control	4:15 PM
13.2	A 3.7mW-RX 4.4mW-TX Fully Integrated Bluetooth Low-Energy/IEEE802.15.4/Proprietary SoC with an ADPLL-Based Fast Frequency Offset Compensation in 40nm CMOS	2:00 PM
13.3	A 10mW Bluetooth Low-Energy Transceiver with On-Chip Matching	2:15 PM
13.7	A +10dBm 2.4GHz Transmitter with Sub-400pW Leakage and 43.7% System Efficiency	4:15 PM

EP1: Moore's Law Challenges Below 10nm: Technology, Design and Economic Implications

Organizers: **Bing Sheu,** *TSMC, Hsinchu, Taiwan*
Kathy Wilcox, *AMD, Boxborough, MA*
Ali Keshavarzi, *Cypress, San Jose, CA*

Moderator: **Dimitri Antoniadis**, *MIT, Cambridge, MA*

Moore's Law has governed advances of silicon technology for more than four decades, providing a tremendous reduction in cost per transistor. Device geometry, packing density, speed performance, and manufacturing cost of a single transistor have scaled together according to Dennard scaling rule. Approaching the sub-10nm era and beyond, Moore's Law faces serious challenges in the near future (5-6 years). Device geometry/density/performance/cost will not scale simultaneously anymore. What are the new scaling rules for logic and memory? Researchers are racing to address 3 scenarios: 1) extending silicon, 2) beyond silicon, and 3) beyond CMOS.

What is the impact of future scaling trends on semiconductor technology and design? How will the industry continue to attract the hundreds of billions of dollars of investment necessary to continue the pace of scaling we have been accustomed to, and also attract young talent to the semiconductor industry? Will 2.5D/3D integration and system innovations come to the rescue? How do we continue to scale power efficiently? How do we manage cost and economic considerations going forward?

Panelists: **Mark Bohr,** *Intel, Hillsboro, OR*
Jack Sun, *TSMC, Hsinchu, Taiwan*
Liam Madden, *Xilinx, San Jose, CA*
Mark Hill, *University of Wisconsin, Madison, WI*
Geoffrey Yeap, *Qualcomm, San Diego, CA*
Jo De Boeck, *imec, Heverlee, Belgium*

EP2: Lost Art? Analog Tricks and Techniques from the Masters

Organizers: **Tsung-Hsien Lin,** *National Taiwan University, Taipei, Taiwan*
Carlo Samori, *Politecnico di Milano, Milano, Italy*
Richard Schreier, *Analog Devices, Toronto, Canada*

Moderator: **Richard Schreier,** *Analog Devices, Toronto, Canada*

This panel will showcase analog circuits and techniques considered to be Lost Art by several of the analog circuit community's most respected members. On the circuit side we have ringmaster Gilbert with his amazing translinear circus, Kawahito with efficient circuits from imaging applications, and Castello with a power-efficient rail-to-rail amplifier. Under the banner of design techniques we have Abidi illustrating the power of intuitive understanding, Wang considering the merits of the RF approach and Craninckx demonstrating that what calibration lacks in elegance it makes up for with robustness and effectiveness. Come watch the sparks fly!

Panelists: **Asad Abidi**, *University of California Los Angeles, Los Angeles, CA*
Barrie Gilbert, *Analog Devices, Portland, OR*
Jan Craninckx, *IMEC, Leuven, Belgium*
Shoji Kawahito, *Shizuoka University, Shizuoka, Japan*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Huei Wang, *National Taiwan University, Taipei, Taiwan*

Non-Volatile Memory Solutions

Session Chair: ***Fatih Hamzaoglu,*** *Intel, Hillsboro, OR*
Associate Chair: ***Takashi Kono,*** *Renesas Electronics, Hyogo, Japan*

7.1 **A Low-Power 64Gb MLC NAND-Flash Memory in 15nm CMOS Technology** — **8:30 AM**
M. Sako[1], Y. Watanabe[1], T. Nakajima[1], J. Sato[1], K. Muraoka[1], M. Fujiu[1], F. Kouno[1], M. Nakagawa[1], M. Masuda[1], K. Kato[1], Y. Terada[1], Y. Shimizu[1], M. Honma[1], A. Imamoto[1], T. Araya[1], H. Konno[1], T. Okanaga[1], T. Fujimura[1], X. Wang[1], M. Muramoto[1], M. Kamoshida[1], M. Kohno[1], Y. Suzuki[1], T. Hashiguchi[1], T. Kobayashi[1], M. Yamaoka[1], R. Yamashita[2]
[1]Toshiba Semiconductor and Storage Products, Yokohama, Japan
[2]Sandisk, Yokohama, Japan

7.2 **A 128Gb 3b/cell V-NAND Flash Memory with 1Gb/s I/O Rate** — **9:00 AM**
J-W. Im, W-P. Jeong, D-H. Kim, S-W. Nam, D-K. Shim, M-H. Choi, H-J. Yoon, D-H. Kim, Y-S. Kim, H-W. Park, D-H. Kwak, S-W. Park, S-M. Yoon, W-G. Hahn, J-H. Ryu, S-W. Shim, K-T. Kang, S-H. Choi, J-D. Ihm, Y-S. Min, I-M. Kim, D-S. Lee, J-H. Cho, O-S. Kwon, J-S. Lee, M-S. Kim, S-H. Joo, J-H. Jang, S-W. Hwang, D-S. Byeon, H-J. Yang, K-T. Park, K-H. Kyung, J-H. Choi
Samsung Electronics, Hwaseong, Korea

7.3 **A 28nm Embedded SG-MONOS Flash Macro for Automotive Achieving 200MHz Read Operation and 2.0MB/s Write Throughput at T_j of 170°C** — **9:30 AM**
Y. Taito[1], M. Nakano[1], H. Okimoto[1], D. Okada[2], T. Ito[1], T. Kono[1], K. Noguchi[1], H. Hidaka[1], T. Yamauchi[1]
[1]Renesas Electronics, Itami, Japan
[2]Renesas Electronics, Hitachinaka, Japan

Break — **10:00 AM**

7.4 **A Covalent-Bonded Cross-Coupled Current-Mode Sense Amplifier for STT-MRAM with 1T-1MTJ Common Source-Line Structure Array** — **10:15 AM**
C. Kim[1], K. Kwon[2], C. Park[1], S. Jang[1], J. Choi[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]Sungkyunkwan University, Suwon, Korea

7.5 **A 3.3ns-Access-Time 71.2µW/MHz 1Mb Embedded STT-MRAM Using Physically Eliminated Read-Disturb Scheme and Normally-Off Memory Architecture** — **10:45 AM**
H. Noguchi, K. Ikegami, K. Kushida, K. Abe, S. Itai, S. Takaya, N. Shimomura, J. Ito, A. Kawasumi, H. Hara, S. Fujita
Toshiba, Kawasaki, Japan

7.6 **1GB/s 2Tb NAND Flash Multi-Chip Package with Frequency-Boosting Interface Chip** — **11:15 AM**
H-J. Kim, J-D. Lim, J-W. Lee, D-H. Na, J-H. Shin, C-H. Kim, S-W. Yu, J-Y. Shin, S-K. Lee, D. Rajagopal, S-T. Kim, K-T. Kang, J-J. Park, Y-J. Kwon, M-J. Lee, S-H. Kim, S-H. Shin, H-G. Kim, J-T. Kim, K-S. Kim, H-S. Joo, C-J. Park, J-H. Kim, M-J. Lee, D-K. Kim, H-J. Yang, D-S. Byeon, K-T. Park, K-H. Kyung, J-H. Choi
Samsung Electronics, Hwaseong, Korea

7.7 **DS1** **Enterprise-Grade 6× Fast Read and 5× Highly Reliable SSD with TLC NAND-Flash Memory for Big-Data Storage** — **11:45 AM**
T. Tokutomi, M. Doi, S. Hachiya, A. Kobayashi, S. Tanakamaru, K. Takeuchi
Chuo University, Tokyo, Japan

Conclusion — **12:15 PM**

Low-Power Digital Techniques

Session Chair: ***Victor Zyuban,*** *IBM T.J. Watson, Yorktown Heights, NY*
Associate Chair: ***Peter Nilsson,*** *Lund University, Lund, Sweden*

8.1 **An 80nW Retention 11.7pJ/Cycle Active Subthreshold ARM Cortex-M0+ Subsystem in 65nm CMOS for WSN Applications** — **8:30 AM**
J. Myers, A. Savanth, D. Howard, R. Gaddh, P. Prabhat, D. Flynn
ARM, Cambridge, United Kingdom

8.2 **DS1** **Batteryless Sub-nW Cortex-M0+ Processor with Dynamic Leakage-Suppression Logic** — **9:00 AM**
W. Lim, I. Lee, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

8.3 **A 10.5µA/MHz at 16MHz Single-Cycle Non-Volatile Memory-Access Microcontroller with Full State Retention at 108nA in a 90nm Process** — **9:30 AM**
V. K. Singhal, V. Menezes, S. Chakravarthy, M. Mehendale
Kilby Labs, Texas Instruments, Bangalore, India

Break — **10:00 AM**

8.4 **A 0.33V/-40°C Process/Temperature Closed-Loop Compensation SoC Embedding All-Digital Clock Multiplier and DC-DC Converter Exploiting FDSOI 28nm Back-Gate Biasing** — **10:15 AM**
S. Clerc[1], M. Saligane[1,2,3], F. Abouzeid[1], M. Cochet[1,2], J-M. Daveau[1], C. Bottoni[1], D. Bol[4], J. De-Vos[4], D. Zamora[5], B. Coeffic[1], D. Soussan[1], D. Croain[1], M. Naceur[6], P. Schamberger[6], P. Roche[1], D. Sylvester[3]
[1]STMicroelectronics, Crolles, France
[2]Aix-Marseille University, Marseille, France
[3]University of Michigan, Ann Arbor, MI
[4]Universite Catholique de Louvain, Louvain La Neuve, Belgium
[5]MAYA Technologies, Grenoble, France
[6]EASii-IC, Grenoble, France

8.5 **A 16nm Auto-Calibrating Dynamically Adaptive Clock Distribution for Maximizing Supply-Voltage-Droop Tolerance Across a Wide Operating Range** — **10:45 AM**
K. Bowman, S. Raina, T. Bridges, D. Yingling, H. Nguyen, B. Appel, Y. Kolla, J. Jeong, F. Atallah, D. Hansquine
Qualcomm, Raleigh, NC

8.6 **Enabling Wide Autonomous DVFS in a 22nm Graphics Execution Core Using a Digitally Controlled Hybrid LDO/Switched-Capacitor VR with Fast Droop Mitigation** — **11:15 AM**
S. T. Kim, Y-C. Shih, K. Mazumdar, R. Jain, J. F. Ryan, C. Tokunaga, C. Augustine, J. P. Kulkarni, K. Ravichandran, J. W. Tschanz, M. M. Khellah, V. De
Intel, Hillsboro, OR

8.7 **Dual-Use Low-Drop-Out Regulator / Power Gate with Linear and On-Off Conduction Modes for Microprocessor On-Die Supply Voltages in 14nm** — **11:45 AM**
K. Luria, J. Shor, M. Zelikson, A. Lyakhov
Intel, Yakum, Israel

Conclusion — **12:15 PM**

High-Performance Wireless

Session Chair: ***Li Lin,*** *Marvell, Saratoga, CA*
Associate Chair: ***Chun-Huat Heng,*** *National University of Singapore, Singapore, Singapore*

9.1 **A 13mm² 40nm Multiband GSM/EDGE/HSPA+/TDSCDMA/LTE Transceiver** — **8:30 AM**

T. Georgantas[1], K. Vavelidis[1], N. Haralabidis[1], S. Bouras[1], I. Vassiliou[1], C. Kapnistis[1], Y. Kokolakis[1], H. Peyravi[1], G. Theodoratos[1], K. Vryssas[1], N. Kanakaris[1], C. Kokozidis[1], S. Kavadias[1], S. Plevridis[1], P. Mudge[2], I. Elgorriaga[2], A. Kyranas[1], S. Liolis[1], E. Kytonaki[1], G. Konstantopoulos[1], P. Robogiannakis[1], K. Tsilipanos[1], M. Margaras[1], P. Betzios[1], R. Magoon[2], I. Bouras[1], M. Rofougaran[2], R. Rofougaran[2]
[1]Broadcom, Athens, Greece
[2]Broadcom, Irvine, CA

9.2 **A Single-Chip HSPA Transceiver with Fully Integrated 3G CMOS Power Amplifiers** — **9:00 AM**

J. Moreira[1], S. Leuschner[1], N. Stevanovic[1], H. Pretl[2], P. Pfann[1], R. Thüringer[1], M. Kastner[1], C. Pröll[2], A. Schwarz[2], F. Mrugalla[1], J. Saporiti[2], U. Basaran[3], A. Langer[1], T. D. Werth[1], T. Gossmann[1], B. Kapfelsperger[1], J. Pletzer[2]
[1]Intel, Neubiberg, Germany
[2]DMCE, Linz, Austria
[3]AVL, Gebze, Turkey

9.3 **A Transmitter with 10b 128MS/s Incremental-Charge-Based DAC Achieving -155dBc/Hz Out-of-Band Noise** — **9:30 AM**

P. E. Paro Filho[1,2], M. Ingels[1], P. Wambacq[1,2], J. Craninckx[1]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

Break — **10:00 AM**

9.4 **A 28nm CMOS Digital Fractional-N PLL with -245.5dB FOM and a Frequency Tripler For 802.11abgn/ac Radio** — **10:15 AM**

X. Gao, L. Tee, W. Wu, K-S. Lee, A. A. Paramanandam, A. Jha, N. Liu, E. Chan, L. Lin
Marvell, Santa Clara, CA

9.5 **Efficient Digital Quadrature Transmitter Based on IQ Cell Sharing** — **10:45 AM**

H. Jin[1], D. Kim[2], S. Jin[1], H. Lee[1], K. Moon[1], H. Kim[2], B. Kim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwaseong, Korea

9.6 **A 5.3GHz 16b 1.75GS/s Wideband RF Mixing-DAC Achieving IMD<-82dBc up to 1.9GHz** — **11:15 AM**

E. Bechthum[1], G. Radulov[1], J. Briaire[2], G. Geelen[2], A. van Roermund[1]
[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]Integrated Device Technology, Eindhoven, The Netherlands

9.7 **DS1** **An LTE SAW-Less Transmitter Using 33% Duty-Cycle LO Signals for Harmonic Suppression** — **11:45 AM**

Y-H. Chen[1], N. Fong[2], B. Xu[3], C. Wang[3]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, San Jose, CA
[3]MediaTek, Austin, TX

Conclusion — **12:00 PM**

Advanced Wireline Techniques and PLLs

Session Chair: ***Gerrit den Besten,*** *NXP Semiconductors, Eindhoven, The Netherlands*

Associate Chair: ***Nicola Da Dalt,*** *Infineon, Villach, Austria*

10.1 DS1 **A 6Gb/s 6pJ/b 5mm-Distance Non-Contact Interface for Modular Smartphones Using Two-Fold Transmission-Line Coupler and EMC-Qualified Pulse Transceiver** — **8:30 AM**
A. Kosuge, S. Ishizuka, J. Kadomoto, T. Kuroda
Keio University, Yokohama, Japan

10.2 DS1 **An FSK Plastic Waveguide Communication Link in 40nm CMOS** — **9:00 AM**
W. Volkaerts, N. Van Thienen, P. Reynaert
KU Leuven, Leuven, Belgium

10.3 DS1 **A 7.5mW 7.5Gb/s Mixed NRZ/Multi-Tone Serial-Data Transceiver for Multi-Drop Memory Interfaces in 40nm CMOS** — **9:30 AM**
K. Gharibdoust[1], A. Tajalli[1,2], Y. Leblebici[1]
[1]EPFL, Lausanne, Switzerland
[2]Kandou Bus, Lausanne, Switzerland

Break — **10:00 AM**

10.4 **A 5.8Gb/s Adaptive Integrating Duobinary-Based DFE Receiver for Multi-Drop Memory Interface** — **10:15 AM**
H-W. Lim[1,2], S-W. Choi[1,2], S-K. Lee[2], C-H. Baek[2], J-Y. Lee[2], G-C. Hwang[2], Y-H. Jun[2], B-S. Kong[1]
[1]Sungkyunkwan University, Suwon, Korea
[2]Samsung Electronics, Hwaseong, Korea

10.5 **A 5.9pJ/b 10Gb/s Serial Link with Unequalized MM-CDR in 14nm Tri-Gate CMOS** — **10:45 AM**
R. Dokania[1], A. Kern[1], M. He[2], A. Faust[1], R. Tseng[1], S. Weaver[1], K. Yu[1], C. Bi[3], T. Liang[3], F. O'Mahony[1]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA
[3]Intel, Hudson, MA

10.6 **Continuous-Time Linear Equalization with Programmable Active-Peaking Transistor Arrays in a 14nm FinFET 2mW/Gb/s 16Gb/s 2-Tap Speculative DFE Receiver** — **11:15 AM**
P. A. Francese, T. Toifl, M. Braendli, C. Menolfi, M. Kossel, T. Morf, L. Kull, T. M. Andersen, H. Yueksel, A. Cevrero, D. Luu
IBM Zurich, Rüschlikon, Switzerland

10.7 **A 6.75-to-8.25GHz 2.25mW 190fs$_{rms}$ Integrated-Jitter PVT-Insensitive Injection-Locked Clock Multiplier Using All-Digital Continuous Frequency-Tracking Loop in 65nm CMOS** — **11:30 AM**
A. Elkholy, M. Talegaonkar, T. Anand, P. K. Hanumolu
University of Illinois, Urbana, IL

10.8 **A Wideband Fractional-N Ring PLL Using a Near-Ground Pre-Distorted Switched-Capacitor Loop Filter** — **11:45 AM**
C-F. Liang, P-Y. Wang
MediaTek, Hsinchu, Taiwan

10.9 **A 13.1-to-28GHz Fractional-N PLL in 32nm SOI CMOS with a $\Delta\Sigma$ Noise-Cancellation Scheme** — **12:00 PM**
M. Ferriss, B. Sadhu, A. Rylyakov, H. Ainspan, D. Friedman
IBM Research, Yorktown Heights, NY

Conclusion — **12:15 PM**

Sensors and Imagers for Life Sciences

Session Chair: ***Makoto Ikeda,*** *University of Tokyo, Tokyo, Japan*
Associate Chair: ***Sam Kavusi,*** *Bosch Research and Technology Center, Palo Alto, CA*

11.1 DS1 **A Time-Divided Spread-Spectrum Code Based 15pW-Detectable Multi-Channel fNIRS IC for Portable Functional Brain Imaging** — **8:30 AM**
J-K. Choi, J-M. Kim, G. Hwang, J. Yang, M-G. Choi, H-M. Bae
KAIST, Daejeon, Korea

11.2 **A 10.8ps-Time-Resolution 256×512 Image Sensor with 2-Tap True-CDS Lock-In Pixels for Fluorescence Lifetime Imaging** — **9:00 AM**
M-W. Seo[1], K. Kagawa[1], K. Yasutomi[1], T. Takasawa[1], Y. Kawata[1], N. Teranishi[1], Z. Li[1], I. A. Halin[2], S. Kawahito[1]
[1]Shizuoka University, Hamamatsu, Japan
[2]Putra University, Selangor Darul Ehsan, Malaysia

11.3 DS1 **A 160×120-Pixel Analog-Counting Single-Photon Imager with Sub-ns Time-Gating and Self-Referenced Column-Parallel A/D Conversion for Fluorescence Lifetime Imaging** — **9:30 AM**
M. Perenzoni, N. Massari, D. Perenzoni, L. Gasparini, D. Stoppa
Fondazione Bruno Kessler (FBK), Trento, Italy

Break — **10:00 AM**

11.4 **A 67,392-SPAD PVTB-Compensated Multi-Channel Digital SiPM with 432 Column-Parallel 48ps 17b TDCs for Endoscopic Time-of-Flight PET** — **10:15 AM**
A. Carimatto, S. Mandai, E. Venialgo, T. Gong, G. Borghi, D. R. Schaart, E. Charbon
Delft University of Technology, Delft, The Netherlands

11.5 **A Time-Correlated Single-Photon-Counting Sensor with 14GS/s Histogramming Time-to-Digital Converter** — **10:45 AM**
N. A. W. Dutton[1,2], S. Gnecchi[1,2], L. Parmesan[1,2], A. J. Holmes[2], B. Rae[2], L. A. Grant[2], R. K. Henderson[1]
[1]University of Edinburgh, Edinburgh, United Kingdom
[2]STMicroelectronics, Edinburgh, United Kingdom

11.6 **A Multi-Channel Neural-Recording Amplifier System with 90dB CMRR Employing CMOS-Inverter-Based OTAs with CMFB Through Supply Rails in 65nm CMOS** — **11:15 AM**
K. A. Ng, Y. P. Xu
National University of Singapore, Singapore, Singapore

11.7 **A Multimodality CMOS Sensor Array for Cell-Based Assay and Drug Screening** — **11:45 AM**
J. S. Park, T. Chi, J. Butts, T. Hookway, T. McDevitt, H. Wang
Georgia Institute of Technology, Atlanta, GA

11.8 DS1 **Integrated Ultrasonic System for Measuring Body-Fat Composition** — **12:00 PM**
H-Y. Tang[1], Y. Lu[2], S. Fung[2], D. A. Horsley[2], B. E. Boser[1]
[1]University of California, Berkeley, CA
[2]University of California, Davis, CA

Conclusion — **12:15 PM**

Inductor-Based Power Conversion

Session Chair: ***Makoto Takamiya,*** *University of Tokyo, Tokyo, Japan*
Associate Chair: ***Dragan Maksimovic,*** *University of Colorado, Boulder, CO*

12.1 **A 0.518mm² Quasi-Current-Mode Hysteretic Buck DC-DC Converter with 3µs Load Transient Response in 0.35µm BCDMOS** — **1:30 PM**
S-H. Lee[1], J-S. Bang[1], K-S. Yoon[1], S-W. Hong[2], C-S. Shin[1], M-Y. Jung[1], G-H. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Suwon, Korea

12.2 **A 1.8V 30-to-70MHz 87% Peak-Efficiency 0.32mm² 4-Phase Time-Based Buck Converter Consuming 3µA/MHz Quiescent Current in 65nm CMOS** — **2:00 PM**
S. J. Kim[1], R. K. Nandwana[1], Q. Khan[2], R. Pilawa-Podgurski[1], P. K. Hanumolu[1]
[1]University of Illinois, Urbana, IL; [2]Qualcomm, San Diego, CA

12.3 **PWM Buck Converter with >80% PCE in 45µA-to-4mA Loads Using Analog-Digital Hybrid Control for Implantable Biomedical Systems** — **2:30 PM**
S-Y. Park, J. Cho, K. Lee, E. Yoon, University of Michigan, Ann Arbor, MI

Break — **3:00 PM**

12.4 **A 7.5W-Output-Power 96%-Efficiency Capacitor-Free Single-Inductor 4-Channel All-Digital Integrated DC-DC LED Driver in a 0.18µm Technology** — **3:15 PM**
S. Dietrich, S. Strache, B. Mohr, J. H. Mueller, L. Rolff, R. Wunderlich, S. Heinen
RWTH Aachen University, Aachen, Germany

12.5 **An Error-Based Controlled Single-Inductor 10-Output DC-DC Buck Converter with High Efficiency at Light Load Using Adaptive Pulse Modulation** — **3:45 PM**
M-Y. Jung, S-H. Park, J-S. Bang, D-C. Park, S-U. Shin, G-H. Cho
KAIST, Daejeon, Korea

12.6 **DS1** **90% Peak Efficiency Single-Inductor-Multiple-Output DC-DC Buck Converter with Output Independent Gate Drive Control** — **4:15 PM**
Y-P. Su[1], C-H. Lin[1], S-Y. Peng[1], R-Y. Huang[1], T-F. Yang[1], S-H. Chen[1], T-J. Lo[1], K-H. Chen[1], C-L. Wey[1], Y-H. Lin[2], C-C. Lee[2], J-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan

12.7 **A Power-Management ASIC with Q-Modulation Capability for Efficient Inductive Power Transmission** — **4:30 PM**
M. Kiani[1], B. Lee[2], P. Yeon[2], M. Ghovanloo[2]
[1]Pennsylvania State University, University Park, PA
[2]Georgia Institute of Technology, Atlanta, GA

12.8 **Wireless Power Transfer System Using Primary Equalizer for Coupling- and Load-Range Extension in Bio-Implant Applications** — **4:45 PM**
X. Li, C-Y. Tsui, W-H. Ki
Hong Kong University of Science and Technology, Hong Kong, China

12.9 **A Fully Integrated 6W Wireless Power Receiver Operating at 6.78MHz with Magnetic Resonance Coupling** — **5:00 PM**
K. Moh[1], F. Neri[2], S. Moon[1], P. Yeon[3], J. Yu[1], Y. Cheon[1], Y-S. Roh[1], M. Ko[1], B-H. Park[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]U-blox, Thalwil, Switzerland
[3]Georgia Institute of Technology, Atlanta, GA

Conclusion — **5:15 PM**

Energy-Efficient RF Systems

Session Chair: ***Ali Afsahi,*** *Broadcom, San Diego, CA*
Associate Chair: ***Jan van Sinderen,*** *NXP Semiconductors, Eindhoven, The Netherlands*

13.1 **A 227pJ/b -83dBm 2.4GHz Multi-Channel OOK Receiver Adopting Receiver-Based FLL** **1:30 PM**
L. Jae-Seung[1], K. Joo-Myoung[1], L. Jae-Sup[2], H. Seok-Kyun[1], L. Sang-Gug[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Advanced Institute of Technology, Suwon, Korea

13.2 **DS1** **A 3.7mW-RX 4.4mW-TX Fully Integrated Bluetooth Low-Energy/IEEE802.15.4/Proprietary SoC with an ADPLL-Based Fast Frequency Offset Compensation in 40nm CMOS** **2:00 PM**
Y-H. Liu[1], C. Bachmann[1], X. Wang[1], Y. Zhang[1], A. Ba[1], B. Busze[1], M. Ding[1], P. Harpe[2], G-J. van Schaik[1], G. Selimis[1], H. Giesen[1], J. Gloudemans[1], A. Sbai[1], L. Huang[1], H. Kato[3], G. Dolmans[1], K. Philips[1], H. de Groot[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands
[3]Renesas Electronics, Kawasaki, Japan

13.3 **DS1** **A 10mW Bluetooth Low-Energy Transceiver with On-Chip Matching** **2:15 PM**
J. Prummel, M. Papamichail, M. Ancis, J. Willms, R. Todi, W. Aartsen, W. Kruiskamp, J. Haanstra, E. Opbroek, S. Rievers, P. Seesink, H. Woering, C. Smit
Dialog Semiconductor, 's-Hertogenbosch, The Netherlands

13.4 **A 6.3mW BLE Transceiver Embedded RX Image-Rejection Filter and TX Harmonic-Suppression Filter Reusing On-Chip Matching Network** **2:30 PM**
T. Sano[1], M. Mizokami[1], H. Matsui[2], K. Ueda[1], K. Shibata[2], K. Toyota[2], T. Saitou[3], H. Sato[1], K. Yahagi[2], Y. Hayashi[4]
[1]Renesas Electronics, Itami, Japan; [2]Renesas Electronics, Kawasaki, Japan
[3]Renesas System Design, Kawasaki, Japan
[4]Renesas Electronics, Sagamihara, Japan

Break **3:00 PM**

13.5 **A -97dBm-Sensitivity Interferer-Resilient 2.4GHz Wake-Up Receiver Using Dual-IF Multi-N-Path Architecture in 65nm CMOS** **3:15 PM**
C. Salazar[1,2,3], A. Kaiser[3], A. Cathelin[1], J. Rabaey[2]
[1]STMicroelectronics, Crolles, France
[2]University of California, Berkeley, CA; [3]University of Lille, Lille, France

13.6 **A 600µW Bluetooth Low-Energy Front-End Receiver in 0.13µm CMOS Technology** **3:45 PM**
A. Selvakumar[1], M. Zargham[1,2], A. Liscidini[1]
[1]University of Toronto, Toronto, ON, Canada
[2]*Now at Qualcomm, San Diego, CA

13.7 **DS1** **A +10dBm 2.4GHz Transmitter with Sub-400pW Leakage and 43.7% System Efficiency** **4:15 PM**
A. Paidimarri, N. Ickes, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

13.8 **A 5.8GHz RF-Powered Transceiver with a 113µW 32-QAM Transmitter Employing the IF-based Quadrature Backscattering Technique** **4:45 PM**
A. Shirane, H. Tan, Y. Fang, T. Ibe, H. Ito, N. Ishihara, K. Masu
Tokyo Institute of Technology, Tokyo, Japan

Conclusion **5:15 PM**

Digital PLLs and SoC Building Blocks

Session Chair: ***Anthony Hill,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Hiroo Hayashi,*** *Toshiba, Kawasaki, Japan*

14.1 **A 0.048mm² 3mW Synthesizable Fractional-N PLL with a Soft Injection-Locking Technique** — **1:30 PM**
W. Deng, D. Yang, A. T. Narayanan, K. Nakata, T. Siriburanon, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

14.2 **A Physically Unclonable Function with BER <10^{-8} for Robust Chip Authentication Using Oscillator Collapse in 40nm CMOS** — **2:00 PM**
K. Yang, Q. Dong, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

14.3 **15fJ/b Static Physically Unclonable Functions for Secure Chip Identification with <2% Native Bit Instability and 140× Inter/Intra PUF Hamming Distance Separation in 65nm** — **2:30 PM**
A. Alvarez, W. Zhao, M. Alioto
National University of Singapore, Singapore, Singapore

14.4 **A 5GHz -95dBc-Reference-Spur 9.5mW Digital Fractional-N PLL Using Reference-Multiplied Time-to-Digital Converter and Reference-Spur Cancellation in 65nm CMOS** — **2:45 PM**
H. Kim[1], J. Sang[2], H. Kim[1], Y. Jo[1], T. Kim[2], H. Park[2], S. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Break — **3:00 PM**

14.5 **A 1.22ps Integrated-Jitter 0.25-to-4GHz Fractional-N ADPLL in 16nm FinFET CMOS** — **3:15 PM**
T-H. Tsai[1], M-S. Yuan[1], C-H. Chang[1], C-C. Liao[1], C-C. Li[1], R. B. Staszewski[2]
[1]TSMC, Hsinchu, Taiwan
[2]Delft University of Technology, Delft, The Netherlands

14.6 **An All-Digital Power-Delivery Monitor for Analysis of a 28nm Dual-Core ARM Cortex-A57 Cluster** — **3:45 PM**
P. N. Whatmough, S. Das, Z. Hadjilambrou, D. M. Bull
ARM, Cambridge, United Kingdom

14.7 **In-Situ Techniques for In-Field Sensing of NBTI Degradation in an SRAM Register File** — **4:15 PM**
T. Yang, D. Kim, P. R. Kinget, M. Seok
Columbia University, New York, NY

14.8 **A 0.009mm² 2.06mW 32-to-2000MHz 2nd-Order ΔΣ Analogous Bang-Bang Digital PLL with Feed-Forward Delay-Locked and Phase-Locked Operations in 14nm FinFET Technology** — **4:30 PM**
M. Song, T. Kim, J. Kim, W. Kim, S-J. Kim, H. Park
Samsung Electronics, Hwaseong, Korea

14.9 **A Sub-Sampling All-Digital Fractional-N Frequency Synthesizer with -111dBc/Hz In-Band Phase Noise and an FOM of -242dB** — **4:45 PM**
Z-Z. Chen[1], Y-H. Wang[1], J. Shin[1], Y. Zhao[1], S. A. Mirhaj[1], Y-C. Kuan[1], H-N. Chen[2], C-P. Jou[2], M-H. Tsai[2], F-L. Hsueh[2], M-C. F. Chang[1]
[1]University of California, Los Angeles, CA
[2]TSMC, Hsinchu, Taiwan

Conclusion — **5:15 PM**

Data-Converter Techniques

Session Chair: ***Seung-Tak Ryu,*** *KAIST, Daejeon, Korea*
Associate Chair: ***Matt Straayer,*** *Maxim Integrated Products, North Chelmsford, MA*

15.1 **An 85dB-DR 74.6dB-SNDR 50MHz-BW CT MASH ΔΣ Modulator in 28nm CMOS** **1:30 PM**
D-Y. Yoon[1], S. Ho[2], H-S. Lee[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]MediaTek, Woburn, MA

15.2 **A 4.5mW CT Self-Coupled ΔΣ Modulator with 2.2MHz BW and 90.4dB SNDR Using Residual ELD Compensation** **2:00 PM**
C-Y. Ho[1], C. Liu[2], C-L. Lo[1], H-C. Tsai[1], T-C. Wang[1], Y-H. Lin[1]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Hefei, China

15.3 **A 115dB-DR Audio DAC with –61dBFS Out-of-Band Noise** **2:30 PM**
H. Westerveld[1], D. Schinkel[2,3], E. van Tuijl[1,3]
[1]University of Twente, Enschede, The Netherlands
[2]Delectronics, Enschede, The Netherlands
[3]Teledyne DALSA Semiconductors, Enschede, The Netherlands

15.4 **A 0.8V 10b 80kS/s SAR ADC with Duty-Cycled Reference Generation** **2:45 PM**
M. Liu, P. Harpe, R. van Dommele, A. van Roermund
Eindhoven University of Technology, Eindhoven, The Netherlands

Break **3:00 PM**

15.5 **A 0.6V 1.17ps PVT-Tolerant and Synthesizable Time-to-Digital Converter Using Stochastic Phase Interpolation with 16× Spatial Redundancy in 14nm FinFET Technology** **3:15 PM**
S-J. Kim, W. Kim, M. Song, J. Kim, T. Kim, H. Park
Samsung Electronics, Hwaseong, Korea

15.6 **A 12b 250MS/s Pipelined ADC with Virtual Ground Reference Buffers** **3:45 PM**
H. H. Boo, D. S. Boning, H-S. Lee
Massachusetts Institute of Technology, Cambridge, MA

15.7 **A 14b 35MS/s SAR ADC Achieving 75dB SNDR and 99dB SFDR with Loop-Embedded Input Buffer in 40nm CMOS** **4:15 PM**
M. Krämer[1], E. Janssen [2], K. Doris[2], B. Murmann[1]
[1]Stanford University, Stanford, CA
[2]NXP Semiconductors, Eindhoven, The Netherlands

15.8 **A 90dB-SFDR 14b 500MS/s BiCMOS Switched-Current Pipelined ADC** **4:45 PM**
DS2
M. El-Chammas, X. Li, S. Kimura, J. Coulon, J. Hu, D. Smith, P. Landman, M. Weaver
Texas Instruments, Dallas, TX

Conclusion **5:15 PM**

Emerging Technologies Enabling Next-Generation Systems

Session Chair: ***Jan Genoe,*** *imec, Leuven, Belgium*
Associate Chair: ***Koichi Nose,*** *Renesas Electronics, Tokyo, Japan*

16.1 **An Ultra-Thin Flexible CMOS Stress Sensor Demonstrated on an Adaptive Robotic Gripper** — **1:30 PM**
Y. Mahsereci[1], S. Saller[2], H. Richter[3], J. Burghartz[3]
[1]University of Stuttgart, Stuttgart, Germany
[2]Festo, Esslingen, Germany; [3]IMS CHIPS, Stuttgart, Germany

16.2 **A Large-Area Image Sensing and Detection System Based on Embedded Thin-Film Classifiers** — **2:00 PM**
W. Rieutort-Louis, T. Moy, Z. Wang, S. Wagner, J. C. Sturm, N. Verma
Princeton University, Princeton, NJ

16.3 DS2 **Flexible Thin-Film NFC Tags Powered by Commercial USB Reader Device at 13.56MHz** — **2:30 PM**
K. Myny[1], B. Cobb[2], J-L. van der Steen[2], A. K. Tripathi[2], J. Genoe[1,3], G. Gelinck[2], P. Heremans[1,3]
[1]imec, Heverlee, Belgium; [2]Holst Centre / TNO, Eindhoven, The Netherlands
[3]KU Leuven, Leuven, Belgium

16.4 **Energy-Autonomous Fever Alarm Armband Integrating Fully Flexible Solar Cells, Piezoelectric Speaker, Temperature Detector, and 12V Organic Complementary FET Circuits** — **2:45 PM**
H. Fuketa[1,2], M. Hamamatsu[1,2], T. Yokota[1,2], W. Yukita[1,2], T. Someya[1,2], T. Sekitani[2,3], M. Takamiya[1,2], T. Someya[1,2], T. Sakurai[1,2]
[1]University of Tokyo, Tokyo, Japan
[2]JST/ERATO, Tokyo, Japan; [3]Osaka University, Osaka, Japan

Break — **3:00 PM**

16.5 DS2 **A NEMS-Array Control IC for Sub-Attogram Gravimetric Sensing Applications in 28nm CMOS Technology** — **3:15 PM**
N. Delorme[1], C. Le Blanc[1], A. Dezzani[1], M. Bely[1], A. Ferret[1], S. Laminette[1], J. Roudier[1], E. Colinet[2]
[1]Asygn, Grenoble, France; [2]Apix Analytics, Grenoble, France

16.6 DS2 **A Double-Side CMOS-CNT Biosensor Array with Padless Structure for Simple Bare-Die Measurements in a Medical Environment** — **3:45 PM**
J. Ahn[1], J. Lim[1], S-H. Kim[1], J-Y. Yun[1], C. Kim[1], S-H. Hong[2], M-J. Lee[3], Y. Park[1]
[1]Seoul National University, Seoul, Korea
[2]Kyung Hee University, Yongin, Korea
[3]Chonnam National University, Gwangju, Korea

16.7 **A 20V 8.4W 20MHz Four-Phase GaN DC-DC Converter with Fully On-Chip Dual-SR Bootstrapped GaN FET Driver Achieving 4ns Constant Propagation Delay and 1ns Switching Rise Time** — **4:15 PM**
M. K. Song[1], L. Chen[1], J. Sankman[1], S. Terry[2], D. Ma[1]
[1]University of Texas, Dallas, TX; [2]Texas Instruments, Dallas, TX

16.8 **1GHz GaN-MMIC Monolithically Integrated MEMS-Based Oscillators** — **4:45 PM**
B. W. Bahr, L. C. Popa, D. Weinstein
Massachusetts Institute of Technology, Cambridge, MA

16.9 **A 128kb 4b/cell Nonvolatile Memory with Crystalline In-Ga-Zn Oxide FET Using V_t Cancel Write Method** — **5:00 PM**
T. Matsuzaki[1], T. Onuki[1], S. Nagatsuka[1], H. Inoue[1], T. Ishizu[1], Y. Ieda[1], N. Yamade[1], H. Miyairi[1], M. Sakakura[1], T. Atsumi[1], Y. Shionoiri[1], K. Kato[1], T. Okuda[1], Y. Yamamoto[1], M. Fujita[2], J. Koyama[1], S. Yamazaki[1]
[1]Semiconductor Energy Laboratory, Kanagawa, Japan
[2]University of Tokyo, Tokyo, Japan

Conclusion — **5:15 PM**

Demonstration Session 2, Tuesday, February 24th 4:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 23rd, and Tuesday February 24th, from 4 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2015, as noted by the symbol **DS2**

Tuesday, February 24th

15.8	**A 90dB-SFDR 14b 500MS/s BiCMOS Switched-Current Pipelined ADC**	**4:45 PM**
16.3	**Flexible Thin-Film NFC Tags Powered by Commercial USB Reader Device at 13.56MHz**	**2:30 PM**
16.5	**A NEMS-Array Control IC for Sub-Attogram Gravimetric Sensing Applications in 28nm CMOS Technology**	**3:15 PM**
16.6	**A Double-Side CMOS-CNT Biosensor Array with Padless Structure for Simple Bare-Die Measurements in a Medical Environment**	**3:45 PM**

Wednesday, February 25th

18.1	**A 2.71nJ/Pixel 3D-Stacked Gaze-Activated Object-Recognition System for Low-Power Mobile HMD Applications**	**8:30 AM**
18.6	**A 0.5nJ/Pixel 4K H.265/HEVC Codec LSI for Multi-Format Smartphone Applications**	**11:15 AM**
19.4	**A 2.7-to-3.7GHz Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter**	**10:15 AM**
20.6	**Electromagnetic Vibration Energy Harvester Interface IC with Conduction-Angle-Controlled Maximum-Power-Point Tracking and Harvesting Efficiencies of up to 90%**	**10:15 AM**
20.8	**A 500nW Batteryless Integrated Electrostatic Energy Harvester Interface Based on a DC-DC Converter with 60V Maximum Input Voltage and Operating From 1µW Available Power, Including MPPT and Cold Start**	**11:15 AM**
21.4	**A Microfluidic-CMOS Platform with 3D Capacitive Sensor and Fully Integrated Transceiver IC for Palmtop Dielectric Spectroscopy**	**10:15 AM**
22.2	**A 25Gb/s Hybrid Integrated Silicon Photonic Transceiver in 28nm CMOS and SOI**	**2:00 PM**
24.2	**Context-Aware Hierarchical Information-Sensing in a 6µW 90nm CMOS Voice Activity Detector**	**3:45 PM**
27.3	**A 3-Axis Open-Loop Gyroscope with Demodulation Phase Error Correction**	**2:30 PM**
27.8	**A 4600µm² 1.5°C (3σ) 0.9kS/s Thermal-Diffusivity Temperature Sensor with VCO-Based Readout in 0.16µm CMOS**	**4:30 PM**

TIMETABLE OF ISSCC 2015 SESSIONS

Sunday, February 22nd	ISSCC 2015 TUTORIALS		
8:30AM	**T1:** Fundamentals of Modern RF Receivers	**T2:** Basics of DRAM Interfaces	**T3:** Ultra-Low-Power Wireless Systems
10:30AM	**T4:** Low-Power Near-Threshold Design	**T5:** High-Speed Current-Steering DACs	**T6**: Clock and Data Recovery Architectures and Circuits
1:30PM	**T7:** Basics of Many-Core Processors	**T8:** Analog Techniques for Nano-Power Circuits	
3:30PM	**T9**: Frequency Synthesizers for Wireless Transceivers	**T10:** CMOS Sensors for 3D Imaging	
	ISSCC 2015 FORUMS		
8:00AM	**F1:** High-Speed Interleaved ADCs	**F2:** Memory Trends: From Big Data to Wearable Devices	

Events below in Bold Box included in Conference registration

	ISSCC 2015 EVENING SESSIONS				
	7:30 PM ES1: Student Research Peview: Short Presentations with Poster Session		**8:00 PM ES2:** Brain-Machine Interfaces: ICs Talking to Neurons		
Monday, February 23rd	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 1:** Plenary Session				
1:30PM	**Session 2:** RF TX/RX Design Techniques	**Session 3:** Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links	**Session 4:** Processors	**Session 5:** Analog Techniques	**Session 6:** Image Sensors & Displays
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour				
	ISSCC 2015 EVENING SESSIONS				
8:00PM	**EP1:** Moore's Law Challenges Below 10nm: Technology, Design, & Economic Implications		**EP2:** Lost Art? Analog Tricks and Techniques from the Masters		
Tuesday, February 24th	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 7:** Non-Volatile Memory Solutions	**Session 8:** Low-Power Digital Techniques	**Session 9:** High-Performance Wireless	**Session 10:** Advanced Wireline Techniques & PLLs	**Session 11:** Sensors & Imagers for Life Sciences
1:30PM	**Session 12:** Inductor-Based Power Conversion	**Session 13:** Energy-Efficient RF Systems	**Session 14:** Digital PLLs & SoC Building Blocks	**Session 15:** Data-Converter Techniques	**Session 16:** Emerging Technologies Enabling Next-Generation Systems
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour				
	ISSCC 2015 EVENING SESSIONS				
8:00PM	**EP3:** Innovating on the Tapeout Treadmill		**ES3:** How to Achieve 1000x More Wireless-Data Capacity. 5G?		
Wednesday, February 25th	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 17:** Embedded Memory & DRAM I/O	**Session 18:** SoCs for Mobile, Vision, Sensing, & Communications	**Session 19:** Advanced Wireless Techniques	**Session 20:** Energy Harvesting & SC Power Conversion	**Session 21:** Innovative Personalized Biomedical Systems
1:30PM	**Session 22:** High Speed Optical Links	**Session 23:** Low-Power SoCs **Session 24:** Secure, Efficient Circuits for the Internet of Things (IoT)	**Session 25:** RF Frequency Generation from GHz to THz	**Session 26:** Nyquist-Rate Converters	**Session 27:** Physical Sensors
5:15 PM	Author Interviews				

Thursday, February 26th	ISSCC 2015 SHORT COURSE			
8:00 AM	**SC1:** Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages			
	ISSCC 2015 FORUMS			
8:00AM	**F3:** Cutting The Last Wire – Advances in Wireless Power	**F4:** Building the Internet of Everything (IoE): Low-Power Techniques at the Circuit & System Levels	**F5:** Advanced RF CMOS Transmitter Techniques	**F6:** IO Design at 25Gb/s and Beyond

EP3: Innovating on the Tapeout Treadmill

Organizer: **Jack Kenney,** *Analog Devices,Somerset, NJ*
Co-Organizer: **Frank O'Mahony**, *Intel, Hillsboro, OR*

Moderator: **Jack Kenney,** *Analog Devices, Somerset, NJ*

The semiconductor industry is highly competitive where mistakes in product execution can hurt a company's revenue stream. A conservative strategy is to make minor increments on existing designs to guarantee performance and delivery dates. Over the long term, engineers get burnt out and competitors who do innovate gain market share. Innovation requires taking risks. The question we pose is: "How do IC companies encourage innovation while meeting tight product development schedules?"

Panelists: **Uming Ko**, *MediaTek, Austin, TX*
Chris Mangelsdorf, *Analog Devices, San Diego, CA*
Michael Neuhauser, *Infineon Technologies, Neubiberg, Germany*
Jinho Park, *Terasquare, Seoul, Korea*
Liesbet Van der Perre, *IMEC, Heverlee, Belgium*
Myles Wakayama, *Broadcom, Irvine, CA*

ES3: How to Achieve 1000× more Wireless Data Capacity? 5G?

Organizer/Chair: **Eric Klumperink,** *Univ. of Twente, Enschede, The Netherlands*

Co-organizers: **Sven Mattisson,** *Ericsson, Lund, Sweden*
Vojkan Vidojkovic *Intel, Duisburg, Germany*

Exponential growth cannot go on for ever, but wireless data growth still does. Especially video and Cloud services drive wireless data consumption, and 1000x in data capacity is targeted in the next 10 years. 5G is in the process of being defined and may include data-rates in Gb/s, seamless integration of wireless LAN, short latencies, expansion into mm-Wave, and massive MIMO. The envisioned systems likely reach the limits of Shannon's capacity and will exploit additional degrees of freedom. A group of experts has been invited to share their thoughts on key new technologies and their path to implementation.

Time	Topic
8:00 PM	**Challenges and Ideas for Wireless Networks** **Marcus Weldon,** *Alcatel-Lucent, Murray Hill, NJ*
8:30 PM	**Shannon's Capacity Meets Moore's Law-The 5G Terminal Perspective** **Asha Keddy,** *Intel, Beaverton, OR*
9:00 PM	**More Bits via the Same Spectrum - Massive MIMO Opportunities** **Fredrik Tufvesson,** *Lund University, Lund, Sweden*
9:30 PM	**5G-Radio Access – Requirements, Concept, and Technical Challenges** **Yoshihisa Kishiyama,** *NTT DOCOMO, Yokosuka, JAPAN*
10:00 PM	**Closing Questions**

Embedded Memory and DRAM I/O

Session Chair: ***Leland Chang,*** *IBM T.J. Watson, Yorktown Heights, NY*
Associate Chair: ***Takefumi Yoshikawa,*** *Panasonic, Nagaokakyo, Japan*

17.1 **A 0.6V 1.5GHz 84Mb SRAM Design in 14nm FinFET CMOS Technology** — **8:30 AM**
E. Karl, Z. Guo, J. W. Conary, J. L. Miller, Y-G. Ng, S. Nalam, D. Kim, J. Keane, U. Bhattacharya, K. Zhang
Intel, Hillsboro, OR

17.2 **A 64kb 16nm Asynchronous Disturb Current Free 2-Port SRAM with PMOS Pass-Gates for FinFET Technologies** — **9:00 AM**
H. Fujiwara, L-W. Wang, Y-H. Chen, K-C. Lin, D. Sun, S-R. Wu, J-J. Liaw, C-Y. Lin, M-C. Chiang, H-J. Liao, S-Y. Wu, J. Chang
TSMC, Hsinchu, Taiwan

17.3 **A 28nm 256kb 6T-SRAM with 280mV Improvement in V_{MIN} Using a Dual-Split-Control Assist Scheme** — **9:30 AM**
M-F. Chang[1], C-F. Chen[1], T-H. Chang[1], C-C. Shuai[1], Y-Y. Wang[1], H. Yamauchi[2]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Fukuoka Institute of Technology, Fukuoka, Japan

Break — **10:00 AM**

17.4 **A 14nm 1.1Mb Embedded DRAM Macro with 1ns Access** — **10:15 AM**
G. Fredeman[1], D. Plass[1], A. Mathews[2], K. Reyer[1], T. Knips[1], T. Miller[1], E. Gerhard[3], D. Kannambadi[1], C. Paone[3], D. Lee[1], D. Rainey[3], M. Sperling[1], M. Whalen[1], S. Burns[4]
[1]IBM, Poughkeepsie, NY
[2]IBM, Austin, TX
[3]IBM, Rochester, MN
[4]IBM, Williston, VT

17.5 **A 3T1R Nonvolatile TCAM Using MLC ReRAM with Sub-1ns Search Time** — **10:45 AM**
M-F. Chang[1], C-C. Lin[1], A. Lee[1], C-C. Kuo[2], G-H. Yang[3], H-J. Tsai[3], T-F. Chen[3], S-S. Sheu[2], P-L. Tseng[2], H-Y. Lee[2], T-K. Ku[2]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]ITRI, Hsinchu, Taiwan
[3]National Chiao Tung University, Hsinchu, Taiwan

17.6 **1V 10Gb/s/pin Single-Ended Transceiver with Controllable Active-Inductor-Based Driver and Adaptively Calibrated Cascade-DFE for Post-LPDDR4 Interfaces** — **11:15 AM**
J. Song[1], H-W. Lee[2], J. Kim[1], S. Hwang[1], C. Kim[1]
[1]Korea University, Seoul, Korea
[2]Hynix Semiconductor, Icheon, Korea

17.7 **A Digital DLL with Hybrid DCC Using 2-Step Duty Error Extraction and 180° Phase Aligner for 2.67Gb/s/pin 16Gb 4-H Stack DDR4 SDRAM with TSVs** — **11:45 AM**
W-J. Yun, I. Song, H. Jeoung, H. Choi, S-H. Lee, J-B. Kim, C-W. Kim, J-H. Choi, S-J. Jang, J. S. Choi
Samsung Electronics, Hwaseong, Korea

Conclusion — **12:15 PM**

SoCs for Mobile Vision, Sensing and Communications

Session Chair: ***Michael Polley,*** *Samsung Research America, Garland, TX*
Associate Chair: ***Paul Liang,*** *MediaTek, Hsinchu, Taiwan*

18.1 DS2 **A 2.71nJ/Pixel 3D-Stacked Gaze-Activated Object-Recognition System for Low-Power Mobile HMD Applications** — **8:30 AM**
I. Hong, K. Bong, D. Shin, S. Park, K. Lee, Y. Kim, H-J. Yoo
KAIST, Daejeon, Korea

18.2 **A 1.9TOPS and 564GOPS/W Heterogeneous Multicore SoC with Color-Based Object Classification Accelerator for Image-Recognition Applications** — **9:00 AM**
J. Tanabe, S. Toru, Y. Yamada, T. Watanabe, M. Okumura, M. Nishiyama, T. Nomura, K. Oma, N. Sato, M. Banno, H. Hayashi, T. Miyamori
Toshiba, Kawasaki, Japan

18.3 **A 0.5V 54μW Ultra-Low-Power Recognition Processor with 93.5% Accuracy Geometric Vocabulary Tree and 47.5% Database Compression** — **9:30 AM**
Y. Kim, I. Hong, H-J. Yoo
KAIST, Daejeon, Korea

Break — **10:00 AM**

18.4 **A Matrix-Multiplying ADC Implementing a Machine-Learning Classifier Directly with Data Conversion** — **10:15 AM**
J. Zhang, Z. Wang, N. Verma
Princeton University, Princeton, NJ

18.5 **A Configurable 12-to-237KS/s 12.8mW Sparse-Approximation Engine for Mobile ExG Data Aggregation** — **10:45 AM**
F. Ren, D. Marković
University of California, Los Angeles, CA

18.6 DS2 **A 0.5nJ/Pixel 4K H.265/HEVC Codec LSI for Multi-Format Smartphone Applications** — **11:15 AM**
C-C. Ju, T-M. Liu, K-B. Lee, Y-C. Chang, H-L. Chou, C-M. Wang, T-H. Wu, H-M. Lin, Y-H. Huang, C-Y. Cheng, T-A. Lin, C-C. Chen, Y-K. Lin, M-H. Chiu, W-C. Li, S-J. Wang, Y-C. Lai, P. Chao, C-D. Chien, M-J. Hu, P-H. Wang, F-C. Yeh, Y-C. Huang, S-H. Chuang, L-F. Chen, H-Y. Lin, M-L. Wu, C-H. Chen, R. Chen, H. Hsu, K. Jou
MediaTek, Hsinchu, Taiwan

18.7 **A 2.4mm² 130mW MMSE-Nonbinary-LDPC Iterative Detector-Decoder for 4×4 256-QAM MIMO in 65nm CMOS** — **11:45 AM**
C-H. Chen, W. Tang, Z. Zhang
University of Michigan, Ann Arbor, MI

Conclusion — **12:15 PM**

Advanced Wireless Techniques

Session Chair: ***Stefano Pellerano,*** *Intel, Hillsboro, OR*
Associate Chair: ***Koji Takinami,*** *Panasonic, Yokohama, Japan*

19.1 **Reconfigurable Receiver with >20MHz Bandwidth Self-Interference Cancellation Suitable for FDD, Co-Existence and Full-Duplex Applications** — **8:30 AM**
J. Zhou, T-H. Chuang, T. Dinc, H. Krishnaswamy
Columbia University, New York, NY

19.2 **A Self-Interference-Cancelling Receiver for In-Band Full-Duplex Wireless with Low Distortion Under Cancellation of Strong TX Leakage** — **9:00 AM**
D-J. V. D. Broek, E. A. Klumperink, B. Nauta
University of Twente, Enschede, The Netherlands

19.3 **Reconfigurable SDR Receiver with Enhanced Front-End Frequency Selectivity Suitable for Intra-Band and Inter-Band Carrier Aggregation** — **9:30 AM**
R. Chen, H. Hashemi
University of Southern California, Los Angeles, CA

Break — **10:00 AM**

19.4 DS2 **A 2.7-to-3.7GHz Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter** — **10:15 AM**
R. T. Yazicigil[1], T. Haque[1,2], M. R. Whalen[1], J. Yuan[1], J. Wright[1], P. R. Kinget[1]
[1]Columbia University, New York, NY
[2]InterDigital Communications, Melville, NY

19.5 **An HCI-Healing 60GHz CMOS Transceiver** — **10:45 AM**
R. Wu, S. Kawai, Y. Seo, K. Kimura, S. Sato, S. Kondo, T. Ueno, N. Fajri, S. Maki, N. Nagashima, Y. Takeuchi, T. Yamaguchi, A. Musa, M. Miyahara, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

19.6 **A 1.9mm-Precision 20GS/s Real-Time Sampling Receiver Using Time-Extension Method for Indoor Localization** — **11:15 AM**
H. G. Han, B. G. Yu, T. W. Kim
Yonsei University, Seoul, Korea

19.7 **A 79GHz Binary Phase-Modulated Continuous-Wave Radar Transceiver with TX-to-RX Spillover Cancellation in 28nm CMOS** — **11:45 AM**
D. Guermandi[1], Q. Shi[1,2], A. Medra[1,2], T. Murata[3], W. Van Thillo[1], A. Bourdoux[1], P. Wambacq[1,2], V. Giannini[1]
[1]imec, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium
[3]Panasonic, Yokohama, Japan

Conclusion — **12:00 PM**

Energy Harvesting and SC Power Conversion

Session Chair: ***Makoto Nagata,*** *Kobe University, Kobe, Japan*
Associate Chair: ***Stefano Stanzione,*** *IMEC-NL, Eindhoven, The Netherlands*

20.1 **A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter with 94.7% Efficiency While Delivering 100mW at 3.3V** — **8:30 AM**
H. Meyvaert[1], G. Villar Piqué[2], R. Karadi[2], H. J. Bergveld[2], M. Steyaert[1]
[1]KU Leuven, Leuven, Belgium
[2]NXP Semiconductors, Eindhoven, The Netherlands

20.2 **A Variable-Conversion-Ratio 3-Phase Resonant Switched Capacitor Converter with 85% Efficiency at 0.91W/mm² Using 1.1 nH PCB-Trace Inductors** — **9:00 AM**
C. Schaef, K. Kesarwani, J. T. Stauth, Dartmouth College, Hanover, NH

20.3 **A Feedforward Controlled On-Chip Switched-Capacitor Voltage Regulator Delivering 10W in 32nm SOI CMOS** — **9:15 AM**
T. M. Andersen[1,2], F. Krismer[2], J. W. Kolar[2], T. Toifl[1], C. Menolfi[1], L. Kull[1], T. Morf[1], M. Kossel[1], M. Brändli[1], P. A. Francese[1]
[1]IBM Research, Rüschlikon, Switzerland; [2]ETH Zürich, Zürich, Switzerland

20.4 **A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors** — **9:30 AM**
Y. Lu[1,2], J. Jiang[1], W-H. Ki[1], C. P. Yue[1], S-W. Sin[2], S-P. U[2,3], R. P. Martins[2,4]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]University of Macau, Macao, China; [3]Synopsys, Macao, China
[4]Instituto Superior Tecnico, Lisbon, Portugal

20.5 **A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement** — **9:45 AM**
J. Jiang[1], Y. Lu[1,2], C. Huang[1], W-H. Ki[1], P. K. T. Mok[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]University of Macau, Macao, China

Break — **10:00 AM**

20.6 DS2 **Electromagnetic Vibration Energy Harvester Interface IC with Conduction-Angle-Controlled Maximum-Power-Point Tracking and Harvesting Efficiencies of up to 90%** — **10:15 AM**
J. Leicht[1], M. Amayreh[1], C. Moranz[1], D. Maurath[1], T. Hehn[2], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]HSG-IMIT, Villingen-Schwenningen, Germany

20.7 **A 0.45-to-3V Reconfigurable Charge-Pump Energy Harvester with Two-Dimensional MPPT for Internet of Things** — **10:45 AM**
X. Liu, E. Sanchez-Sinencio, Texas A&M University, College Station, TX

20.8 DS2 **A 500nW Batteryless Integrated Electrostatic Energy Harvester Interface Based on a DC-DC Converter with 60V Maximum Input Voltage and Operating From 1µW Available Power, Including MPPT and Cold Start** — **11:15 AM**
S. Stanzione[1], C. V. Liempd[1], M. Nabeto[2], F. R. Yazicioglu[3], C. V. Hoof[1,4]
[1]Holst Centre / imec, Eindhoven, The Netherlands; [2]OMRON, Kizugawa, Japan
[3]imec, Heverlee, Belgium; [4]KU Leuven, Leuven, Belgium

20.9 **An Energy-Recycling Three-Switch Single-Inductor Dual-Input Buck/Boost DC-DC Converter with 93% Peak Conversion Efficiency and 0.5mm² Active Area for Light Energy Harvesting** — **11:30 AM**
H-J. Chen, Y-H. Wang, P-C. Huang, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

20.10 **A 50nW-to-10mW Output Power Tri-Mode Digital Buck Converter with Self-Tracking Zero Current Detection for Photovoltaic Energy Harvesting** — **11:45 AM**
P-H. Chen, C-S. Wu, K-C. Lin, National Chiao Tung University, Hsinchu, Taiwan

Conclusion — **12:15 PM**

Innovative Personalized Biomedical Systems

Session Chair: ***David Ruffieux,*** *CSEM, Neuchatel, Switzerland*
Associate Chair: ***Antoine Dupret,*** *CEA-LETI - MINATEC, Gif-sur-Yvette, France*

21.1 **A 79pJ/b 80Mb/s Full-Duplex Transceiver and a 42.5μW 100kb/s Super-Regenerative Transceiver for Body Channel Communication** — **8:30 AM**
H. Cho, H. Kim, M. Kim, J. Jang, J. Bae, H-J. Yoo
KAIST, Daejeon, Korea

21.2 **A 3nW Signal-Acquisition IC Integrating an Amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC** — **9:00 AM**
P. Harpe, H. Gao, R. van Dommele, E. Cantatore, A. van Roermund
Eindhoven University of Technology, Eindhoven, The Netherlands

21.3 **A 6.45μW Self-Powered IoT SoC with Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios** — **9:30 AM**
A. Klinefelter[1], N. E. Roberts[2], Y. Shakhsheer[1], P. Gonzalez[1], A. Shrivastava[1], A. Roy[1], K. Craig[1], M. Faisal[2], J. Boley[1], S. Oh[2], Y. Zhang[1], D. Akella[1], D. D. Wentzloff[2], B. H. Calhoun[1]
[1]University of Virginia, Charlottesville, VA
[2]University of Michigan, Ann Arbor, MI

Break — **10:00 AM**

21.4 DS2 **A Microfluidic-CMOS Platform with 3D Capacitive Sensor and Fully Integrated Transceiver IC for Palmtop Dielectric Spectroscopy** — **10:15 AM**
M. Bakhshiani, M. A. Suster, P. Mohseni
Case Western Reserve University, Cleveland, OH

21.5 **A Portable Micro Gas Chromatography System for Volatile Compounds Detection with 15ppb of Sensitivity** — **10:45 AM**
T-H. Tzeng, C-Y. Kuo, S-Y. Wang, P-K. Huang, P-H. Kuo, Y-M. Huang, W-C. Hsieh, S-A. Yu, Y. J. Tseng , W-C. Tian, S-C. Lee, S-S. Lu
National Taiwan University, Taipei, Taiwan

21.6 **A Smart CMOS Assay SoC for Rapid Blood Screening Test of Risk Prediction** — **11:15 AM**
P-H. Kuo[1], J-C. Kuo[1], H-T. Hsueh[1], J-Y. Hsieh[1], Y-C. Huang[1], T. Wang[2], Y-H. Lin[3], C-T. Lin[1], Y-J. Yang[1], S-S. Lu[1]
[1]National Taiwan University, Taipei, Taiwan
[2]Chang Gung University, Taoyuan, Taiwan
[3]National Taiwan University Hospital, Taipei, Taiwan

21.7 **A 0.036mbar Circadian and Cardiac Intraocular Pressure Sensor for Smart Implantable Lens** — **11:30 AM**
A. Donida[1], G. Di Dato[1], P. Cunzolo[1], M. Sala[1], F. Piffaretti[1,2], P. Orsatti[2], D. Barrettino[1]
[1]University of Applied Sciences of Southern Switzerland, Manno, Switzerland
[2]Oculox Technology, Bioggio, Switzerland

21.8 **A 16-ch Patient-Specific Seizure Onset and Termination Detection SoC with Machine-Learning and Voltage-Mode Transcranial Stimulation** — **11:45 AM**
M. A. B. Altaf, C. Zhang, J. Yoo
Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates

21.9 **A Wearable EEG-HEG-HRV Multimodal System with Real-Time tES Monitoring for Mental Health Management** — **12:00 PM**
U. Ha, Y. Lee, H. Kim, T. Roh, J. Bae, C. Kim, H-J. Yoo
KAIST, Daejeon, Korea

Conclusion — **12:15 PM**

High-Speed Optical Links

Session Chair: ***Azita Emami,*** *California Institute of Technology, Pasadena, CA*
Associate Chair: ***Hyeon-Min Bae,*** *KAIST, Daejeon, Korea*

22.1 **A 25Gb/s Burst-Mode Receiver for Rapidly Reconfigurable Optical Networks** **1:30 PM**
A. Rylyakov, J. Proesel, S. Rylov, B. Lee, J. Bulzacchelli, A. Ardey, B. Parker, M. Beakes, C. Baks, C. Schow, M. Meghelli
IBM T.J. Watson, Yorktown Heights, NY

22.2 DS2 **A 25Gb/s Hybrid Integrated Silicon Photonic Transceiver in 28nm CMOS and SOI** **2:00 PM**
Y. Chen[1], M. Kibune[1], A. Toda[2], A. Hayakawa[1,3,4], T. Akiyama[1,3,4], S. Sekiguchi[1,3,4], H. Ebe[1,3,4], N. Imaizumi[1], T. Akahoshi[1], S. Akiyama[3], S. Tanaka[3], T. Simoyama[3], K. Morito[1,3,4], T. Yamamoto[2], T. Mori[1], Y. Koyanagi[1], H. Tamura[1]*
[1]Fujitsu Laboratories, Kawasaki, Japan; [2]Fujitsu Laboratories of America, Sunnyvale, CA
[3]Photonics Electronics Technology Research Association, Tsukuba, Japan
[4]Fujitsu Limited, Kawasaki, Japan

22.3 **A 4-to-11GHz Injection-Locked Quarter-Rate Clocking for an Adaptive 153fJ/b Optical Receiver in 28nm FDSOI CMOS** **2:30 PM**
M. Raj, S. Saeedi, A. Emami, California Institute of Technology, Pasadena, CA

22.4 **A 24Gb/s 0.71pJ/b Si-Photonic Source-Synchronous Receiver with Adaptive Equalization and Microring Wavelength Stabilization** **2:45 PM**
K. Yu[1], H. Li[2], C. Li[3], A. Titriku[1], A. Shafik[1], B. Wang[1], Z. Wang[4], R. Bai[2], C-H. Chen[3], M. Fiorentino[3], P. Y. Chiang[2,4], S. Palermo[1]
[1]Texas A&M University, College Station, TX; [2]Oregon State University, Corvallis, OR
[3]Hewlett-Packard Labs, Palo Alto, CA; [4]Fudan University, Shanghai, China

Break **3:00 PM**

22.5 **A 4×20Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver** **3:15 PM**
M. Rakowski[1,2], M. Pantouvaki[1], P. De Heyn[1], P. Verheyen[1], M. Ingels[1], H. Chen[1,3], J. De Coster[1], G. Lepage[1], B. Snyder[1], K. De Meyer[1,2], M. Steyaert[2], N. Pavarelli[3], J. S. Lee[4], P. O'Brien[4], P. Absil[1], J. Van Campenhout[1]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium
[3]imec - Ghent University, Ghent, Belgium; [4]Tyndall National Institute, Cork, Ireland

22.6 **A 25Gb/s 4.4V-Swing AC-Coupled Si-Photonic Microring Transmitter with 2-Tap Asymmetric FFE and Dynamic Thermal Tuning in 65nm CMOS** **3:45 PM**
H. Li[1], Z. Xuan[2], A. Titriku[3], C. Li[4], K. Yu[3], B. Wang[3], A. Shafik[3], N. Qi[1], Y. Liu[5], R. Ding[5], T. Baehr-Jones[5], M. Fiorentino[4], M. Hochberg[5], S. Palermo[3], P. Y. Chiang[1,6]
[1]Oregon State University, Corvallis, OR; [2]University of Delaware, Newark, DE
[3]Texas A&M University, College Station, TX; [4]Hewlett-Packard, Palo Alto, CA
[5]Coriant Advanced Technology Group, New York, NY
[6]Fudan University, Shanghai, China

22.7 **4×25.78Gb/s Retimer ICs for Optical Links in 0.13µm SiGe BiCMOS** **4:15 PM**
T. Shibasaki, Y. Tsunoda, H. Oku, S. Ide, T. Mori, Y. Koyanagi, K. Tanaka, T. Ishihara, H. Tamura
Fujitsu Laboratories, Kawasaki, Japan

22.8 **A 24-to-35Gb/s ×4 VCSEL Driver IC with Multi-Rate Referenceless CDR in 0.13µm SiGe BiCMOS** **4:45 PM**
Y. Tsunoda, T. Shibasaki, S. Ide, T. Mori, Y. Koyanagi, K. Tanaka, T. Ishihara, H. Tamura
Fujitsu Laboratories, Kawasaki, Japan

22.9 **A 1310nm 3D-Integrated Silicon Photonics Mach-Zehnder-Based Transmitter with 275mW Multistage CMOS Driver Achieving 6dB Extinction Ratio at 25Gb/s** **5:00 PM**
M. Cignoli[1], G. Minoia[2], M. Repossi[2], D. Baldi[2], A. Ghilioni[1], E. Temporiti[2], F. Svelto[1]
[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Pavia, Italy

Conclusion **5:15 PM**

Low-Power SoCs

Session Chair: ***Andy Charnas,*** *Nvidia, Santa Clara, CA*
Associate Chair: ***Youngmin Shin,*** *Samsung, Hwaseong, Korea*

23.1 **20nm High-κ Metal-Gate Heterogeneous 64b Quad-Core CPUs and Hexa-Core GPU for High-Performance and Energy-Efficient Mobile Application Processor** **1:30 PM**

J. Pyo, Y. Shin, H-J. Lee, S-I. Bae, M-S. Kim, K. Kim, K. Shin, Y. Kwon, H. Oh, J. Lim, D-W. Lee, J. Lee, I. Hong, K. Chae, H-H. Lee, S-W. Lee, S. Song, C-H. Kim, J-S. Park, H. Kim, S. Yun, U-R. Cho, J. C. Son, S. Park
Samsung Electronics, Hwaseong, Korea

23.2 **A 1920×1080 30fps 611mW Five-View Depth-Estimation Processor for Light-Field Applications** **2:00 PM**

H-H. Chen[1], C-T. Huang[2], S-S. Wu[1], J-L. Huang[1], T-C. Ma[1], L-G. Chen[1]
[1]National Taiwan University, Taipei, Taiwan
[2]National Tsing Hua University, Hsinchu, Taiwan

23.3 **A Highly Integrated Smartphone SoC Featuring a 2.5GHz Octa-Core CPU with Advanced High-Performance and Low-Power Techniques** **2:30 PM**

H. Mair[1], G. Gammie[1], A. Wang[2], S. Gururajarao[1], I. Lin[1], H. Chen[1], W. Kao[2], A. Rajagopalan[1], W-Z. Ge[1], R. Lagerquist[1], S. Rahman[1], C. Chung[1], S. Wang[2], L-K. Wong[2], Y-C. Zhuang[2], K. Li[1], J. Wang[1], M. Chau[1], Y. Liu[1], D. Dia[1], M. Peng[2], U. Ko[2]
[1]MediaTek, Austin, TX
[2]MediaTek, Hsinchu, Taiwan

Break

Secure, Efficient Circuits for IoT

Session Chair: ***Chris Nicol,*** *Wave Semiconductor, Campbell, CA*
Associate Chair: ***Shinichiro Mutoh,*** *NTT, Kanagawa, Japan*

24.1 **Circuit Challenges from Cryptography** **3:15 PM**
I. Verbauwhede, J. Balasch, S. Sinha Roy, A. Van Herrewege
KU Leuven, Heverlee, Belgium

24.2 **Context-Aware Hierarchical Information-Sensing in a 6µW 90nm CMOS Voice Activity Detector** **3:45 PM**
DS2
K. Badami, S. Lauwereins, W. Meert, M. Verhelst
KU Leuven, Leuven, Belgium

24.3 **20k-spin Ising Chip for Combinational Optimization Problem with CMOS Annealing** **4:15 PM**
M. Yamaoka, C. Yoshimura, M. Hayashi, T. Okuyama, H. Aoki, H. Mizuno
Hitachi, Tokyo, Japan

24.4 **A 6.5Gb/s Shared Bus Using Electromagnetic Connectors for Downsizing and Lightening Satellite Processor System by 60%** **4:45 PM**
A. Kosuge[1], S. Ishizuka[1], M. Abe[2], S. Ichikawa[2], T. Kuroda[1]
[1]Keio University, Yokohama, Japan
[2]Japan Aerospace Exploration Agency, Tsukuba, Japan

Conclusion **5:15 PM**

RF Frequency Generation from GHz to THz

Session Chair: ***Payam Heydari,*** *University of California, Irvine, CA*
Associate Chair: ***Taizo Yamawaki,*** *Hitachi, Tokyo, Japan*

25.1 **A Highly Digital Frequency Synthesizer Using Ring-Oscillator Frequency-to-Digital Conversion and Noise Cancellation** **1:30 PM**
C. Weltin-Wu[1,2], G. Zhao[2], I. Galton[2]
[1]Analog Devices, San Jose, CA
[2]University of California, San Diego, CA

25.2 **A 2.2GHz -242dB-FOM 4.2mW ADC-PLL Using Digital Sub-Sampling Architecture** **2:00 PM**
T. Siriburanon, S. Kondo, K. Kimura, T. Ueno, S. Kawashima, T. Kaneko, W. Deng, M. Miyahara, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

25.3 **A VCO with Implicit Common-Mode Resonance** **2:30 PM**
D. Murphy, H. Darabi, H. Wu
Broadcom, Irvine, CA

25.4 **A 1/f Noise Upconversion Reduction Technique Applied to Class-D and Class-F Oscillators** **2:45 PM**
M. Shahmohammadi, M. Babaie, R. B. Staszewski
Delft University of Technology, Delft, The Netherlands

Break **3:00 PM**

25.5 **A 320GHz Phase-Locked Transmitter with 3.3mW Radiated Power and 22.5dBm EIRP for Heterodyne THz Imaging Systems** **3:15 PM**
R. Han[1,2], C. Jiang[1], A. Mostajeran[1], M. Emadi[1], H. Aghasi[1], H. Sherry[3], A. Cathelin[3], E. Afshari[1]
[1]Cornell University, Ithaca, NY
[2]Massachusetts Institute of Technology, Cambridge, MA
[3]STMicroelectronics, Crolles, France

25.6 **A 70.5-to-85.5GHz 65nm Phase-Locked Loop with Passive Scaling of Loop Filter** **3:45 PM**
Z. Huang[1], H. C. Luong[1], B. Chi[2], Z. Wang[2], H. Jia[2]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Tsinghua University, Beijing, China

25.7 **A 2.4GHz 4mW Inductorless RF Synthesizer** **4:15 PM**
L. Kong, B. Razavi
University of California, Los Angeles, CA

25.8 **A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz Offset Frequencies in 0.13µm CMOS Using an ISF Manipulation Technique** **4:30 PM**
A. Mostajeran[1,2], M. Sharif Bakhtiar[1], E. Afshari[2]
[1]Sharif University of Technology, Tehran, Iran
[2]Cornell University, Ithaca, NY

25.9 **A ±3ppm 1.1mW FBAR Frequency Reference with 750MHz Output and 750mV Supply** **4:45 PM**
K. A. Sankaragomathi[1], J. Koo[1], R. Ruby[2], B. P. Otis[1]
[1]University of Washington, Seattle, WA
[2]Avago Technologies, San Jose, CA

Conclusion **5:15 PM**

Nyquist-Rate Converters

Session Chair: ***Hae-Seung Lee,*** *Massachusetts Institute of Technology, Cambridge, MA*

Associate Chair: ***Seng-Pan U,*** *University of Macau, Macau, China*

26.1 **A 1mW 71.5dB SNDR 50MS/s 13b Fully Differential Ring-Amplifier-Based SAR-Assisted Pipeline ADC** — **1:30 PM**

Y. Lim[1,2], M. P. Flynn[1]
[1]University of Michigan, Ann Arbor, MI
[2]Samsung Electronics, Yongin, Korea

26.2 **A 5.5fJ/conv-step 6.4MS/s 13b SAR ADC Utilizing a Redundancy-Facilitated Background Error-Detection-and-Correction Scheme** — **2:00 PM**

M. Ding[1], P. Harpe[2], Y-H. Liu[1], B. Busze[1], K. Philips[1], H. de Groot[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

26.3 **An 800MS/s 10b/13b Receiver for 10GBASE-T Ethernet in 28nm CMOS** — **2:30 PM**

D. Vecchi[1], J. Mulder[1], Y. Ke[1], S. Bozzola[1], M. Core[2], N. Saputra[3], Q. Zhang[1], J. Riley[1], H. Yan[1], M. Introini[1], S. Wang[1], C. M. Ward[1], J. Westra[1], J. Wan[1], K. Bult[1]
[1]Broadcom, Bunnik, The Netherlands
[2]Broadcom, Irvine, CA
[3]Qualcomm, San Diego, CA

Break — **3:00 PM**

26.4 **A 21fJ/conv-step 9 ENOB 1.6GS/s 2× Time-Interleaved FATI SAR ADC with Background Offset and Timing-Skew Calibration in 45nm CMOS** — **3:15 PM**

B-R-S. Sung[1], D-S. Jo[1], I-H. Jang[1], D-S. Lee[2], Y-S. You[2], Y-H. Lee[2], H-J. Park[2], S-T. Ryu[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

26.5 **A 5.5mW 6b 5GS/s 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS** — **3:45 PM**

C-H. Chan[1], Y. Zhu[1], S-W. Sin[1], S-P. U[1,2], R. Martins[1,3]
[1]University of Macau, Macao, China
[2]Synopsys, Macao, China
[3]Instituto Superior Tecnico, Universidade de Lisboa, Portugal

26.6 **A 5GS/s 150mW 10b SHA-Less Pipelined/SAR Hybrid ADC in 28nm CMOS** — **4:15 PM**

M. Brandolini[1], Y. Shin[1], K. Raviprakash[1], T. Wang[1], R. Wu[1], H. M. Geddada[1], Y-J. Ko[2], Y. Ding[2], C-S. Huang[2], W-T. Shih[2], M-H. Hsieh[2], W-T. Chou[1], T. Li[1], A. Shrivastava[1], Y-C. Chen[1], J-J. Hung[1], G. Cusmai[1], J. Wu[1], M. M. Zhang[1], G. Unruh[1], A. Venes[1], H. S. Huang[2], C-Y. Chen[1]
[1]Broadcom, Irvine, CA
[2]Broadcom, Hsinchu, Taiwan

26.7 **A 2.6b/cycle-Architecture-Based 10b 1.7GS/s 15.4mW 4×-Time-Interleaved SAR ADC with a Multistep Hardware-Retirement Technique** — **4:45 PM**

H-K. Hong[1], H-W. Kang[1], D-S. Jo[1], D-S. Lee[2], Y-S. You[2], Y-H. Lee[2], H-J. Park[2], S-T. Ryu[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion — **5:15 PM**

Physical Sensors

Session Chair: ***Ralf Brederlow,*** *Texas Instruments, Freising, Germany*
Associate Chair: ***Michiel Pertijs,*** *Delft University of Technology, Delft, The Netherlands*

27.1 **A 3-Axis Gyroscope for Electronic Stability Control with Continuous Self-Test** — **1:30 PM**
G. K. Balachandran[1], V. P. Petkov[1], T. Mayer[2], T. Balslink[2]
[1]Robert Bosch, Palo Alto, CA
[2]Robert Bosch, Reutlingen, Germany

27.2 **A 1.2μg/√Hz-Resolution 0.4μg-Bias-Instability MEMS Silicon Oscillating Accelerometer with CMOS Readout Circuit** — **2:00 PM**
X. Wang[1], J. Zhao[1,2], Y. Zhao[1,2], G. M. Xia[2], A. P. Qiu[2], Y. Su[2], Y. P. Xu[1]
[1]National University of Singapore, Singapore, Singapore
[2]Nanjing University of Science and Technology, Nanjing, China

27.3 DS2 **A 3-Axis Open-Loop Gyroscope with Demodulation Phase Error Correction** — **2:30 PM**
C. D. Ezekwe[1], W. Geiger[2], T. Ohms[3]
[1]Robert Bosch, Palo Alto, CA
[2]Robert Bosch, Reutlingen, Germany
[3]Bosch Sensortec, Reutlingen, Germany

27.4 **A 0.8mm³ ±0.68psi Single-Chip Wireless Pressure Sensor for TPMS Applications** — **2:45 PM**
M. B. Nagaraju[1], A. R. Lingley[1], S. Sridharan[2], J. Gu[1], R. Ruby[2], B. P. Otis[1]
[1]University of Washington, Seattle, WA
[2]Avago Technologies, San Jose, CA

Break — **3:00 PM**

27.5 **A 30ppm <80nJ Ring-Down-Based Readout Circuit for Resonant Sensors** — **3:15 PM**
H. Jiang, Z-Y. Chang, M. Pertijs
Delft University of Technology, Delft, The Netherlands

27.6 **A 0.7pF-to-10nF Fully Digital Capacitance-to-Digital Converter Using Iterative Delay-Chain Discharge** — **3:45 PM**
W. Jung, S. Jeong, S. Oh, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

27.7 **A 0.05mm² 1V Capacitance-to-Digital Converter Based on Period Modulation** — **4:15 PM**
Y. He, Z-Y. Chang, L. Pakula, S. H. Shalmany, M. Pertijs
Delft University of Technology, Delft, The Netherlands

27.8 DS2 **A 4600μm² 1.5°C (3σ) 0.9kS/s Thermal-Diffusivity Temperature Sensor with VCO-Based Readout** — **4:30 PM**
R. Quan, U. Sonmez, F. Sebastiano, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

27.9 **A 200kS/s 13.5b Integrated-Fluxgate Differential-Magnetic-to-Digital Converter with an Oversampling Compensation Loop for Contactless Current Sensing** — **4:45 PM**
M. Kashmiri[1], W. Kindt[2], F. Witte[2], R. Kearey[2], D. Carbonell[3]
[1]Texas Instruments, Santa Clara, CA
[2]Texas Instruments, Delft, The Netherlands
[3]Texas Instruments, Greenock, United Kingdom

Conclusion — **5:15 PM**

Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages

Wim Dehaene, *KU Leuven, Leuven, Belgium*

Technology scaling brings lower supply voltages. For advanced CMOS technology nodes of 40nm and beyond, this leads to specific challenges. In particular, analog circuits require specialized design approaches and innovative techniques. Maintaining high precision with reduced available signal swing while keeping energy consumption within reasonable bounds has presented challenges for many circuit designers. Increased technological variability and leakage only make this worse.

This short course provides an overview of the challenges and solutions of modern circuit design in advanced technologies with low supply voltage. The course will start with a system overview of the problem. Then, several types of circuits will be discussed. General analog and mixed-mode building blocks, A/D converters and RF components each are the subject of a separate talk.

A Roadmap to Lower Supply Voltages – A System Perspective

Jan Rabaey, *University of California, Berkeley, CA*

A novel class of devices that broadly fall under the rubrics of “Internet-of-things” and “wearable” may soon upend the unprecedented growth in mobile devices that we have witnessed over the past decades. For these devices to be viable, however, a continuous reduction in energy-per-operation is necessary. Unfortunately, the flattening of traditional semiconductor scaling means that only a small part of this reduction can be expected from technology advances. The good news is that one design parameter that has a huge impact on energy consumption - the supply voltage - is still substantially above the fundamental limits (at least for digital circuits). Hence this leaves ample room for innovative design techniques to explore further lowering of the supply voltage.

The largest hindrances to low supply voltages are leakage and uncertainty. The presence of leakage sets a minimum voltage (and energy) for digital operation in a given technology. Going beyond that requires an aggressive energy-management strategy. Addressing uncertainty (arising from process variations, temporal changes and data statistics) typically requires margins to ensure functionality and correctness. Hence techniques to minimize margining while guaranteeing correct operation are important. Both leakage and uncertainty management can be performed at many layers of the design hierarchy. In this lecture, we will present an overview of commonly used and emerging techniques, illustrated with industrial and academic examples.

About the presenter:
Jan Rabaey received his Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Belgium. In 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. He is currently the scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the founding director of the Berkeley Ubiquitous SwarmLab.

Prof. Rabaey has made widely recognized contributions to a number of domains, including advanced wireless systems, sensor networks, configurable circuits and low-power design. His current interests include the conception and implementation of next-generation integrated wireless systems over a very broad range of applications, as well as exploring the interaction between the cyber and the biological world.

He is the recipient of a wide range of major awards, including the Semiconductor Industry Association (SIA) University Researcher Award. He is an IEEE Fellow and a member of the Royal Flemish Academy of Sciences and Arts of Belgium, and has been involved in a broad variety of start-up ventures.

Designing Ultra-Low-Voltage Analog and Mixed-Signal Circuits

Peter Kinget, *Columbia University, New York, NY*

This talk focuses on the challenges and solutions for designing analog circuits at supply voltages well below 1V. Fundamental limitations of the MOS transistor force us to rethink the most basic analog circuit configurations. At the same time, low-voltage operation offers new opportunities to use all four terminals of the transistor while the speed of nanoscale devices allows for different representations for analog signal information. The lecture discusses solutions for analog building blocks like amplifiers operating at ultra-low supply voltages, and how they can be used to build complete analog signal processing systems like filters, track-and-hold circuits or analog-to-digital converters.

About the presenter:
Peter R. Kinget received an engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium. He has worked in industrial research and development at Bell Laboratories, Broadcom, Celight and Multilink before joining the faculty of the Department of Electrical Engineering, Columbia University, NY in 2002, where he is currently a Professor. He is also a consulting expert on patent litigation and a technical consultant to industry. His research interests are in analog, RF and power integrated circuits and the applications they enable in communications, sensing, and power management.

Dr. Kinget is a Fellow of the IEEE and is widely published. He is a co-recipient of several awards including the "First Prize" in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge and the "2011 IEEE Communications Society Award for Advances in Communication." He has been a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society (SSCS), and an Associate Editor of the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems II. He has served on the program committees of many of the major solid-state circuits conferences and currently is an elected member of the IEEE SSCS Adcom.

ADC Design in Scaled Technologies

Andrea Baschirotto, *University of Milan-Bicocca, Milan, Italy*

This talk focuses on recent developments in ADCs, which are one of the primary components in any mixed-signal integrated system.

The first part reviews the most relevant changes in MOS transistor behaviour when realized in scaled technologies (V_{DD} reduction, gain reduction, V_{TH} deviation, higher speed, etc.), focusing on how they affect ADC design.

After this, general trends in ADCs in the recent literature are analyzed, and the reported ADC implementations in the 32nm or below technologies are presented, looking at their innovative solutions, emphasizing the common trends and the difference between the several implementations.

About the presenter:
Andrea Baschirotto received his Ph.D. in electronics engineering in 1994 from Univ. Pavia. He is an Associate Professor at Univ. Milan-Bicocca, Italy. His main research interests are in the design of CMOS mixed analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He participated in several research collaborations (also funded by National and European projects) and several collaboration between Universities and Industries. In 2010 he co-founded the start-up sparklingIC, of which he serves as CTO.

He has authored or co-authored more than 190 papers in international journals and presentations at international conferences, 6 book chapters, and holds 35 US patents. In addition, he has co-authored more than 120 papers within research collaborations on high-energy physics experiments.

Andrea Baschirotto has been Associate Editor of several IEEE journals. He has been the Technical Program Committee Chairman for ESSCIRC 2002. He is or was member of the Technical Program Committee of several international conferences (ISSCC, ESSCIRC, AACD, DATE, etc.). Since 2005, he is serving the ESSCIRC TPC as Data Converter Subcommittee Chairman. He has been the secretary of the European Committee of ISSCC Technical Program Committee. He is an IEEE Fellow (2013). He is the founder (2006) and the Chairman of the IEEE Solid-State Circuit Society Italian Chapter.

Ultra-Low-Voltage RF Circuits and Transceivers

Hyunchol Shin, *Kwangwoon University, Seoul, Korea*

The continuing scaling of CMOS technology and the growing needs for single-cell battery operation drive the supply voltage of RF circuits toward the sub-1V region. As the supply voltage approaches only 2-3 times V_{th}, many traditional RF circuit topologies are becoming ineffective. Much effort has been spent rethinking the conventional circuit topologies and radio architectures for RF applications. This presentation focuses on the design issues and recent progress in transceiver architectures and building blocks to meet the sub-1V challenge.

The first part reviews several sub-1V design techniques that can be applied to many RF circuits. The second part covers the receiver and its key building blocks (LNA and mixer) discussing design fundamentals, advanced circuit topologies, and recent implementation examples for sub-1V operation. The third part covers the most power-hungry parts in RF transceivers, namely the VCO, frequency divider, and PLL synthesizer. The presentation concludes by explaining the opportunities that are yet to come.

About the presenter:
Hyunchol Shin received the Ph.D. degree in electrical engineering from KAIST, Korea in 1998. After his Ph.D., he had gained professional experience at several institutions and companies, such as Samsung Electronics, Korea, University of California, Los Angeles, CA, Qualcomm, San Diego, CA, all working on RF/analog circuit design for wireless communications. Since 2003, he has been with Kwangwoon University, Seoul, Korea, where he is currently a Professor. From 2010 to 2011, he took a sabbatical leave at Qualcomm Corporate R&D, San Diego, CA. His research focuses on CMOS RF/analog/microwave circuits and PLL frequency synthesizers.

Prof. Shin has (co)authored over 70 journal and conference papers and holds 30 patents in the field of RF/analog circuit design. He is a Senior Member of the IEEE, and has served on the technical program committees of several IEEE conferences such as ISSCC, A-SSCC, MWSCAS, RFIT, ISOCC, and IWS.

F3: Cutting the Last Wire – Advances in Wireless Power

Organizer: **Marco Berkhout,** *NXP Semiconductors, Nijmegen, The Netherlands*

Committee: **Anton Bakker,** *Integrated Device Technology, Morgan Hill, CA*
Christoph Sandner, *Infineon Technologies, Villach, Austria*
Wentai Liu, *UCLA, Los Angeles, CA*
Chih-Ming Hung, *Mediatek, Taipei, Taiwan*
Bill Redman-White, *University of Southampton, Southampton, United Kingdom*

In recent years the availability of products for wireless charging of mobile devices has increased rapidly. The introduction of the Qi standard for wireless power transfer has marked the beginning of what could be a revolution in the way we charge our smartphones and tablets. Wireless power transfer is considered for use in applications ranging from biomedical implants that require a couple of milliWatts to electrical vehicles that require kiloWatts. The vision of a future where we can conveniently, efficiently and safely charge our devices and vehicles anywhere without having to drag adapters and cables with us is gradually starting to become more realistic. This forum aims to give an overview of the state-of-the art in wireless power transfer. The fundamentals of different wireless power transfer techniques will be discussed, including not only inductive and resonant magnetic, but also capacitive power transfer and RF energy harvesting.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	Introduction by the Chair
8:30 AM	**Wireless Power Transfer - Introduction and History** ***Grant Covic,*** *University of Auckland, Auckland, New Zealand*
9:20 AM	**Capacitive Power Transfer – Efficient Power and Data** ***Seth Sanders,*** *University of California, Berkeley, CA*
10:10 AM	Break
10:35 AM	**Midfield Powering for Bioelectronics Medicines** ***Ada Poon,*** *Stanford University, Stanford, CA*
11:25 AM	**Wireless Power Delivery for Medical Applications** ***Chi-Ying Tsui,*** *The Hong Kong University of Science and Technology, Hong Kong, China*
12:15 PM	Lunch
1:20 PM	**Comparison of Magnetic Charging Techniques for Mobile Devices** ***Matteo Agostinelli,*** *Infineon Technologies, Villach, Austria*
2:10 PM	**Magnetic "Inductive" Charging and the Qi Standard** ***Dries van Wageningen,*** *Philips Research, Eindhoven, The Netherlands*
3:00 PM	Break
3:20 PM	**Magnetic Resonant Charging and the A4WP Standard** ***Francesco Carobolante,*** *Qualcomm Technologies, San Diego, CA*
4:10 PM	**The Confluence of Resonant Switching Topologies and Wireless Charging** ***Sanjaya Maniktala,*** *Integrated Device Technology, Morgan Hill, CA*
5:00 PM	Conclusion

F4: Building the Internet of Everything (IoE): Low-Power Techniques at the Circuit and System Levels

Organizers: **Marian Verhelst,** *KU Leuven, Leuven, Belgium*
Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

Committee: **Makoto Takamiya,** *University of Tokyo, Tokyo, Japan*
Michael Clinton, *TSMC, Austin, TX*
Kathy Wilcox, *AMD, Boxborough, MA*
Koichi Nose, *Renesas Electronics, Tokyo, Japan*

Current projections estimate there will be 25-30 billion devices on the Internet of Things (IoT) by 2020. While technology scaling no longer brings automatic system energy savings, emerging big-data and wearable-monitoring applications require compact autonomous devices. These divergent requirements steer research towards new energy efficiency strategies for compact wireless devices at the circuit (analog, digital), architectural, and system levels.

This forum brings together recent developments towards next-generation energy-scarce SoCs for wearables and the IoT, together forming the Internet of Everything (IoE). The speakers will cover recent low-energy strategies, including energy harvesting and power management techniques, novel processor and compute architectures, low-power memory options and smart integration approaches.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction**
8:30 AM	**Low-Power Integrated Circuit and System Design for Wearable Healthcare Applications** ***Mario Konijnenburg,*** *imec / Holst Centre, Eindhoven, The Netherlands*
9:20 AM	**Ambient Energy Harvesting for the Internet of Everything** ***Po-Hung Chen,*** *National Chiao-Tung University, Hsinchu, Taiwan*
10:10 AM	Break
10:35 AM	**Embedded Voltage Regulation and Energy Management for IoT/IoE** ***Gerard Villar Piqué,*** *NXP, Eindhoven, The Netherlands*
11:25 AM	**Wearable Architectures: What IoT Means for Circuit Design** ***Rob Aitken,*** *ARM, San Jose, CA*
12:15 PM	Lunch
1:20 PM	**Memory Innovations for the Internet of Things** ***Sudhanshu Khanna,*** *Texas Instruments, Dallas, TX*
2:10 PM	**Nonvolatile Logic-in-Memory Architecture for Ultra-Low Power VLSI Systems** ***Takahiro Hanyu,*** *Tohoku University, Sendai, Japan*
3:00 PM	Break
3:20 PM	**Smart Sensor Microsystems: Application-Dependent Integration Approaches** ***Minkyu Je,*** *DGIST, Daegu, Korea*
4:10 PM	**Miniature IoT Sensor System Design and Integration Challenges** ***David Blaauw,*** *University of Michigan, Ann Arbor, MI*
5:00 PM	Conclusion

F5: Advanced RF CMOS Transmitter Techniques

Organizer: **Piet Wambacq,** imec, Leuven, Belgium

Committee: **Stefano Pellerano,** *Intel, Hillsboro, OR*
Sven Mattisson, *Ericsson, Lund, Sweden*
Shouhei Kousai, *Toshiba, Kawasaki, Japan*
Ali Afsahi, *Broadcom, San Diego, CA*
Taizo Yamawaki, *Hitachi, Tokyo, Japan*

Integrated transmitters for mobile applications face increasingly stringent specifications due to increasing modulation bandwidth and dynamic range for higher data rates and reduced out-of-band emissions and noise for coexistence. Long battery life, low cost and small form factor require high efficiency and large integration levels.

On the other hand, the digital-analog boundary comes closer to the antenna. Further, new scaling-friendly paradigms are coming up, such as the use of switched capacitors in transmitters.

This forum presents the latest advancements in high-bandwidth, high-efficiency CMOS-based transmitters targeted for mobile devices, from both system architecture and building-block design perspectives.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Piet Wambacq,*** *imec, Leuven, Belgium*
8:30 AM	**A Technical Foundation for RF CMOS Transmitters** ***Earl McCune,*** *RF Communications Consulting, San Francisco, CA*
9:20 AM	**Cellular High-Power PAs and SOI Switches** ***Kohei Onizuka,*** *Toshiba, Kawasaki, Japan*
10:10 AM	Break
10:35 AM	**RF Transmitters Must Byte the Digit** ***Ali Niknejad,*** *University of California, Berkeley, CA*
11:25 AM	**Charge-Based Signal Processing for Wireless Transmitters** ***Jan Craninckx,*** *imec, Leuven, Belgium*
12:15 PM	Lunch
1:20 PM	**Digital Operation of Base-Station PAs Enabled by Extended Drain CMOS** ***Mustafa Acar,*** *NXP, Nijmegen, The Netherlands*
2:10 PM	**Digital Polar PAs Using Switched-Capacitor Circuits** ***Jeff Walling,*** *University of Utah, Salt Lake City, UT*
3:00 PM	Break
3:20 PM	**Envelope-Tracking Operation of CMOS PAs** ***Bumman Kim,*** *Postech, Pohang, Korea*
4:10 PM	**Wideband Radio Base-Station Transmitter Trends** ***Mats Klingberg,*** *Ericsson, Stockholm, Sweden*
5:00 PM	Closing remarks

F6: I/O Design at 25Gb/s and Beyond: Enabling the Future Communication Infrastructure for Big Data

Organizer: **Ken Chang,** *Xilinx, San Jose, CA*

Chair: **Frank O'Mahony,** *Intel, Hillsboro, OR*

Committee: **Elad Alon,** *University of California, Berkeley, CA*
Hyeon-Min Bae, *KAIST, Daejeon, Korea*
Nicola Da Dalt, *Infineon, Germany*
Eric Fluhr, *IBM, Austin, TX*
Frank O'Mahony, *Intel, Hillsboro, OR*

The demand for ultra-high speed transceivers continues to rise exponentially due to the insatiable demand for high-throughput interconnect. Standards between 25 and 32Gb/s are rapidly approaching maturity, and available products and IPs at these rates are iterating to push down power while extending channel-loss recovery limits. Predictably, specifications are now in early stages for extending per-lane bandwith to between 40 and 64Gb/s. Meeting these 25Gb/s+ targets, especially for long-reach applications, is stressing the capabilities of both the underlying circuitry and the communication channels, and has caused significant rethinking of the overall system and circuit architectures for these links. In particular, the debate about multi-level (PAM4) versus binary (PAM2) signaling and which path offers the best energy-efficiency/data-rate scalability has returned to the foreground. Similarly, the emergence of high-speed ADCs with sufficient resolution for link applications has driven renewed interest in DSP-based approaches, while other efforts have pushed more analog/mixed-signal link components to over 60Gb/s/lane. To further ensure low BER operations, sophisticated coding such as FEC is brought into the discussion. Even in the domain of optical communications, significant challenges related to the bandwidth capabilities of the optical devices as well as the back end processing are currently being addressed. In fact, some of the highest speed optical links are limited by the short electrical interconnect between the driver circuitry and the optical module itself. This forum presents state-of-the-art I/O techniques enabling such high line rates across both optical and electrical interfaces as well as a number of emerging standards such as 802.3bj, various flavors of CEI, and HMC (hybrid memory cube).

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** ***Frank O'Mahony,*** *Intel, Hillsboro, OR*
8:30 AM	**Challenges and Solutions for Next-Generation 40 to 56Gb/s Transceivers** ***Adam Healey,*** *Avago Technologies, San Jose, CA*
9:20 AM	**Link Modeling and Design at 40Gb/s and Beyond** ***Bryan Casper,*** *Intel, Hillsboro, OR*
10:10 AM	Break
10:35 AM	**56Gb/s SerDes Transceiver Design: NRZ, PAM4, and Others** ***Jri Lee,*** *National Taiwan University, Taipei, Taiwan*
11:25 AM	**ADC-and-DAC-Based Transceivers for 100Gb Ethernet** ***Jun Cao,*** *Broadcom, Irvine, CA*
12:15 PM	Lunch
1:20 PM	**Low-Power CMOS ADCs for 100+Gb/s Wireline Communications** ***Lukas Kull,*** *IBM Research, Zurich, Switzerland*
2:10 PM	**Digital Signal Processing Chips for 100-to-400Gb/s Optical Communications** ***Oscar Agazzi,*** *Clariphy Communications, Irvine, CA*
3:00 PM	Break
3:20 PM	**Analog/mixed Signal Designs for Over-25Gb/s Server Links** ***Hirotaka Tamura,*** *Fujitsu Laboratory, Kawasaki, Japan*
4:10 PM	**Power-Efficient Design Approaches for >60Gb/s Transceivers** ***Chih-Kong Ken Yang,*** *University of California, Los Angeles, CA*
5:00 PM	Closing Remarks (Chair)

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

EXECUTIVE COMMITTEE

CONFERENCE CHAIR
Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

EXECUTIVE COMMITTEE SECRETARY, PRESS COORDINATOR
Siva Narendra, Tyfone, Portland, OR

DIRECTOR OF FINANCE AND BOOK DISPLAY COORDINATOR
Bryant Griffin, Penfield, NY

PROGRAM CHAIR
Hoi-Jun Yoo, KAIST, Daejeon, Korea

PROGRAM VICE-CHAIR
Kevin Zhang, Intel, Hillsboro, OR

STUDENT FORUM CHAIR AND UNIVERSITY RECEPTIONS
Jan van der Spiegel, University of Pennsylvania, Philadelphia, PA

DEMONSTRATION SESSION CHAIR
Uming Ko, MediaTek, Austin TX

ITPC FAR EAST REGIONAL CHAIR
Jae-Youl Lee, Samsung, Gyeonggi-Do, Korea

ITPC FAR EAST REGIONAL VICE-CHAIR
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan

ITPC EUROPEAN REGIONAL CHAIR
Alison Burdett, Toumaz Microsystems, Oxfordshire, United Kingdom

ITPC EUROPEAN REGIONAL VICE CHAIR
Maurits Ortmanns, University of Ulm, Institute of Microelectronics, Ulm, Germany

ADCOM REPRESENTATIVE
Bryan Ackland, Stevens Institute of Technology, Hoboken, NJ

DIRECTOR OF PUBLICATIONS AND PRESENTATIONS
Laura Fujino, University of Toronto, Toronto, Canada

DIRECTOR OF AUDIOVISUAL SERVICES
John Trnka, Rochester, MN

PRESS LIAISON AND ARC CHAIR
Kenneth C. Smith, University of Toronto, Toronto, Canada

FORUMS CHAIR
Bram Nauta, University of Twente, Enschede, The Netherlands

EDUCATIONAL EVENTS CHAIR (SHORT COURSE/TUTORIALS)
Ali Sheikholeslami, University of Toronto, Toronto, Canada

DIRECTOR OF OPERATIONS
Melissa Widerkehr, Widerkehr and Associates, Montgomery Village, MD

WEBSITE/DATA MANAGEMENT
Trudy Stetzler, Houston, TX

TECHNICAL EDITORS

Jason H. Anderson, University of Toronto, Toronto, Canada
Dustin Dunwell, Kapik Integration, Toronto, Canada
Vincent Gaudet, University of Waterloo, Waterloo, Canada
Glenn Gulak, University of Toronto, Toronto, Canada
James W. Haslett, The University of Calgary, Calgary, Canada
Kostas Pagiamtzis, Semtech, Burlington, Canada
Kenneth C. Smith, University of Toronto, Toronto, Canada

MULTI-MEDIA COORDINATOR

Dave Halupka, Kapik Integration, Toronto, Canada

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

PROGRAM CHAIR:
Hoi-Jun Yoo, KAIST, Daejeon, Korea

PROGRAM VICE CHAIR:
Kevin Zhang, Intel, Hillsboro, OR

ANALOG SUBCOMMITTEE

Chair: Axel Thomsen, Silicon Laboratories, Austin, TX
Anton Bakker, IDT, Morgan Hill, CA
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Vadim Ivanov, Texas Instruments, Tucson, AZ
Xicheng Jiang, Broadcom, Irvine, CA
Jae-Youl Lee, Samsung, Gyeonggi-Do, Korea
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan
Saska Lindfors, Neonode, Stockholm, Sweden
Dragan Maksimovic, University of Colorado, Boulder, CO
Piero Malcovati, University of Pavia, Pavia, Italy
Philip Mok, HKUST, Kowloon, Hong Kong
Makoto Nagata, Kobe University, Kobe, Japan
Edgar Sanchez-Sinencio, Texas A&M University, College Station, TX
Christoph Sandner, Infineon Technologies Austria, Villach, Austria
Stefano Stanzione, IMEC-NL, Eindhoven, The Netherlands
Makoto Takamiya, University of Tokyo, Tokyo, Japan
Ed (Adrianus JM) van Tuijl, University of Twente, Enschede, Twente, The Netherlands
Young-Jin Woo, Silicon Works, Daejeon, Korea

DATA CONVERTERS SUBCOMMITTEE

Chair: Boris Murmann, Stanford University, Stanford, CA
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Pieter Harpe, Eindhoven University, of Technology, Eindhoven, The Netherlands
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
John Khoury, Silicon Laboratories, Austin, TX
Stéphane Le Tual, STmicroelectronics, Crolles Cedex, France
Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA
Takahiro Miki, Renesas Electronics, Hyogo, Japan
Gerhard Mitterregger, Intel Mobile, St. Magdalen, Austria
Jan Mulder, Broadcom, Bunnik, The Netherlands
Ken Nishimura, Agilent, Santa Clara, CA
Maurits Ortmanns, University of Ulm, Ulm, Germany
Seung-Tak Ryu, KAIST, Daejeon, Korea
Richard Schreier, Analog Devices, Toronto, Canada
Venkatesh Srinivasan, Texas Instruments, Dallas, TX
Matt Straayer, Maxim Integrated Products, North Chelmsford, MA
Seng-Pan U (Ben), University of Macau, Taipa, Macau
Jieh-Tsorng Wu, National Chiao-Tung University, Hsin-Chu, Taiwan

EED SUBCOMMITTEE

Chair: Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO
Edith Beigné, CEA-LETI, Grenoble, France
Takashi Hashimoto, Panasonic, Fukuoka, Japan
Paul Liang, MediaTek, Hsinchu, Taiwan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Peter Nilsson, Lund University, Lund, Sweden
Yongha Park, Samsung, Yongin, Korea
Michael Polley, Samsung, Richardson, TX
Bing Sheu, TSMC, Hsinchu, Taiwan
Dennis Sylvester, University of Michigan, Ann Arbor, MI
Marian Verhelst, KULeuven, Heverlee, Belgium
Victor Zyuban, IBM T. J. Watson, Research Center, Yorktown Heights, NY

HP DIGITAL SUBCOMMITTEE

Chair: Stefan Rusu, Intel, Santa Clara, CA
Andy Charnas, Nvidia, Santa Clara, CA
Vivek De, Intel, Hillsboro, OR
Eric Fluhr, IBM, Austin, TX
Hiroo Hayashi, Toshiba Semiconductor, Kawasaki, Japan
Anthony Hill, Texas Instruments, Dallas, TX
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Tobias Noll, RWTH Aachen University, Aachen, Germany
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
Luke (Jinuk) Shin, Oracle, Santa Clara, CA
Youngmin Shin, Samsung, Hwansung, Korea
Kathy Wilcox, AMD, Boxborough, MA

IMMD SUBCOMMITTEE

Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan
Ralf Brederlow, Texas Instruments Deutschland GmbH, Freising, Germany
Peng Cong, Google, Mountain View, CA
Roman Genov, University of Toronto, Toronto, Canada
Robert Johansson, OmniVision, Oslo, Norway
Sam Kavusi, Robert Bosch, Palo Alto, CA
TaeChan Kim, Korea University, Yongin, Korea
Wentai Liu, UCLA, Los Angeles, CA
Young-Sun Na, LG Electronics, Seoul, Korea
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Yusuke Oike, Sony, Kanagawa, Japan
Aaron Partridge, SiTime, Sunnyvale, CA
Michiel Pertijs, TU Delft, Delft, The Netherlands
Joseph Shor, Intel Israel, Yakum, Israel
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Peter Chung-Yu Wu, National Chiao Tung University,Hsinchu, Taiwan
Yong Ping Xu, National University of Singapore, Singapore
Refet Firat Yazicioglu, IMEC, Leuven, Belgium

MEMORY SUBCOMMITTEE

Chair: Joo Sun Choi, Samsung Electronics, Hwasung, Korea
Martin Brox, Micron, Munchen, Germany
Jonathan Chang, TSMC, Hsinchu, Taiwan
Leland Chang, IBM T. J. Watson Research Center, Yorktown Heights, NY
Sungdae Choi, SK Hynix Semiconductor, Icheon-si, Korea
Michael Clinton, TSMC Technology, Austin, TX
Fatih Hamzaoglu, Intel, Hillsboro, OR
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
Takashi Kono, Renesas Electronics, Hyogo, Japan
Hugh Mair, MediaTek, Fairview, TX
James Sung, Etron Technology, Hsinchu, Taiwan
Takefumi Yoshikawa, Panasonic, Kyoto, Japan

RF SUBCOMMITTEE

Chair: Andreia Cathelin, STMicroelectronics, Crolles Cedex, France
Ali Afsahi, Broadcom, San Diego, CA
Ehsan Afshari, Cornell University, Ithaca, NY
Minoru Fujishima, Hiroshima University, Higashi-hiroshima, Japan
Payam Heydari, University of California, Irvine, Irvine, CA
Chih-Ming Hung, Mediatek, Taipei, Taiwan
Tae Wook Kim, Yonsei University, Seoul, Korea
Antonio Liscidini, University of Toronto, Toronto, Canada
Andrea Mazzanti, University of Pavia, Pavia, Italy
Ahmad Mirzaei, Broadcom, Irvine, CA
Borivoje Nikolic, University of California, Berkeley, Berkeley, CA
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Hyunchol Shin, Kwangwoon University, Seoul, Korea
Vojkan Vidojkovic, Intel Mobile Communications, North Rhine-Westphalia, Germany
Piet Wambacq, imec, Heverlee, Belgium
Taizo Yamawaki, Hitachi, Tokyo, Japan

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Alison Burdett, Toumaz Microsystems, Abingdon, United Kingdom
Antoine Dupret, CEA, Gif-sur-Yvette, France
Jan Genoe, imec, Leuven, Belgium
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Ali Keshavarzi, Cypress, Los Altos, CA
Donghyun Kim, KAIST, Daejeon, Korea
Shahriar Mirabbasi, University of British Columbia, Vancouver, Canada
Shinichiro Mutoh, NTT, Kanagawa, Japan
Shuichi Nagai, Panasonic, Osaka, Japan
Chris Nicol, Wave Semiconductor, Sunnyvale, CA
Koichi Nose, Renesas Electronics, Tokyo, Japan
Pirooz Pavarandeh, Maxim Integrated, Products, San Jose, CA
Yogesh K. Ramadass, Texas Instruments, Dallas, TX
David Ruffieux, CSEM, Neuchated, Switzlerland
Alice Wang, MediaTek, Hsin-Chu, Taiwan

WIRELESS SUBCOMMITTEE

Chair: Aarno Pärssinen, University of Oulu, Espoo, Finland
Gangadhar Burra, Qualcomm-Atheros, San Jose, CA
Pierre Busson, ST Microelectronics, Crolles, France
Jan Crols, AnSem, Heverlee, Belgium
Guang-Kaai Dehng, Mediatek, Hsinchu, Taiwan
Hossein Hashemi, University of Southern California, Los Angeles, CA
Chun-Huat Heng, National University of Singapore, Singapore
Eric Klumperink, University of Twente, Enschede, The Netherlands
Shouhei Kousai, Toshiba, Kawasaki, Japan
Li Lin, Marvell Semiconductor, Santa Clara, CA
Sven Mattisson, Ericsson AB, Lund, Sweden
Alyosha Molnar, Cornell University, Ithaca, NY
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Stefano Pellerano, Intel, Hillsboro, OR
Woogeun Rhee, Tsinghua University, Beijing, China
Koji Takinami, Panasonic, Yokohama, Japan
Jan Van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands

WIRELINE SUBCOMMITTEE

Daniel Friedman, IBM Thomas J. Watson Research Center, Yorktown Heights, NY
Elad Alon, University of California, Berkeley, Berkeley, CA
Ajith Amerasekera, Texas Instruments, Dallas, TX
Hyeon-Min Bae, KAIST, Daejong, Korea
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Ken Chang, Xilinx, San Jose, CA
Nicola Da Dalt, Infineon, Villach, Austria
Azita Emami, California Institute of Technology, Pasadena, CA
Ichiro Fujimori, Broadcom, Irvine, CA
Pavan Kumar Hanumolu, University of Illinois, Urbana-Champlain, Urbana, IL
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Shunichi Kaeriyama, Renesas, Tokyo, Japan
Jack Kenney, Analog Devices, Somerset, NY
Jaeha Kim, Seoul National University, Seoul, Korea
Hideyuki Nosaka, NTT, Atsugi-shi, Japan
Frank O'Mahony, Intel, Hillsboro, OR
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan

EUROPEAN REGIONAL SUBCOMMITTEE

ITPC EUROPEAN REGIONAL CHAIR

Alison Burdett, Toumaz Microsystems, Abingdon, United Kingdom

ITPC EUROPEAN REGIONAL VICE CHAIR

Maurits Ortmanns, University of Ulm, Ulm, Germany

ITPC EUROPEAN REGIONAL SECRETARY

David Stoppa, Fondazione Bruno Kessler, Trento, Italy

Edith Beigné, CEA-LETI, Grenoble, France
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Ralf Brederlow, Texas Instruments Deutschland GmbH, Freising, Germany
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Martin Brox, Micron, Munchen, Germany
Pierre Busson, ST Microelectronics, Crolles, France
Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Andreia Cathelin, STMicroelectronics, Crolles Cedex, France
Jan Crols, AnSem, Heverlee, Belgium
Nicola Da Dalt, Infineon, Villach, Austria
Antoine Dupret, CEA Saclay Nano-INNOV, Gif-sur-Yvette, France
Jan Genoe, imec, Leuven, Belgium
Pieter Harpe, Eindhoven University of Technology, Eindhoven, The Netherlands
Robert Johansson, OmniVision, Oslo, Norway
Eric Klumperink, University of Twente, Enschede, The Netherlands
Stéphane Le Tual, STmicroelectronics, Crolles Cedex, France
Saska Lindfors, Neonode, Stockholm, Sweden
Piero Malcovati, University of Pavia, Pavia, Italy
Sven Mattisson, Ericsson AB, Lund, Sweden
Andrea Mazzanti, University of Pavia, Pavia, Italy
Gerhard Mitterregger, Intel Mobile Communications Austria, St. Magdalen, Austria
Jan Mulder, Broadcom, Bunnik, The Netherlands
Peter Nilsson, Lund University, Lund, Sweden
Tobias Noll, RWTH Aachen University, Aachen, Germany
Aarno Pärssinen, Broadcom, Helsinki, Finland
Michiel Pertijs, TU Delft, Delft, The Neterlands
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
David Ruffieux, CSEM, Neuchated, Switzerland
Jussi Ryynanen, Aalto University, Espoo, Finland

European Members (continued):

Carlo Samori, Politecnico di Milano, Milano, Italy
Christoph Sandner, Infineon Technologies Austria AG, Villach, Austria
Joseph Shor, Intel Israel, Yakum, Israel
Stefano Stanzione, IMEC-NL, Eindhoven, The Netherlands
Jan Van Sinderen, NXP, Eindhoven, The Netherlands
Ed (Adrianus JM) van Tuijl, University of Twente, Enschede, The Netherlands
Marian Verhelst, KULeuven, Heverlee, Belgium
Vojkan Vidojkovic, Intel Mobile, Communications, Duisburg, Germany
Piet Wambacq, imec, Heverlee, Belgium
Refet Firat Yazicioglu, IMEC, Leuven, Belgium

FAR EAST REGIONAL SUBCOMMITTEE

ITPC FAR EAST REGIONAL CHAIR
Jae-Youl Lee, Samsung, Yongin-City, Korea

ITPC FAR EAST REGIONAL VICE-CHAIR
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan

ITPC FAR EAST REGIONAL SECRETARY
Atsuki Inoue, Fujitsu, Kawasaki, Japan

Hyeon-Min Bae, KAIST, Daejong, Korea
Jonathan Chang, TSMC, Hsinchu, Taiwan
Joo Sun Choi, Samsung Electronics, Hwasung-city, Korea
Sungdae Choi, SK Hynix Semiconductor, Icheon-si, Korea
Guang-Kaai Dehng, Mediatek, Hsinchu, Taiwan
Minoru Fujishima, Hiroshima University, Higashi-hiroshima, Japan
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Takashi Hashimoto, Panasonic, Fukuoka, Japan
Hiroo Hayashi, Toshiba Corporation Semiconductor, Kawasaki, Japan
Chun-Huat Heng, National University of Singapore, Singapore
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Chih-Ming Hung, Mediatek, Taipei, Taiwan
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
Makoto Ikeda, University of Tokyo, Tokyo, Japan
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Shunichi Kaeriyama, Renesas, Tokyo, Japan
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
Donghyun Kim, KAIST, Daejeon, Korea
Jaeha Kim, Seoul National University, Seoul, Korea
TaeChan Kim, Korea University, Yongin, Korea
Tae Wook Kim, Yonsei University, Seoul, Korea
Takashi Kono, Renesas Electronics, Hyogo, Japan
Shouhei Kousai, Toshiba, Kawasaki, Japan
Paul Liang, MediaTek, Hsinchu, Taiwan
Takahiro Miki, Renesas Electronics, Hyogo, Japan
Philip Mok, HKUST, Kowloon, Hong Kong
Shinichiro Mutoh, NTT, Kanagawa, Japan
Young-Sun Na, LG Electronics, Seoul, Korea
Shuichi Nagai, Panasonic, Osaka, Japan
Makoto Nagata, Kobe University, Hyogo, Japan
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Hideyuki Nosaka, NTT, Atsugi-shi, Japan
Koichi Nose, Renesas Electronics, Tokyo, Japan
Yusuke Oike, Sony, Kanagawa, Japan
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Yongha Park, Samsung, Yongin, Korea
Woogeun Rhee Tsinghua University, Beijing, China
Seung-Tak Ryu, KAIST, Daejeon, Korea
Bing Sheu, TSMC, Hsinchu, Taiwan
Yasuhisa Shimazaki, Renesas, Tokyo, Japan
Hyunchol Shin, Kwangwoon University, Seoul, Korea
Youngmin Shin, Samsung, Hwansung, Korea
James Sung, Etron Technology, Hsinchu, Taiwan
Makoto Takamiya, University of Tokyo, Tokyo, Japan
Koji Takinami, Panasonic, Yokohama, Japan
Seng-Pan U (Ben), University of Macau, Taipa, Macau
Alice Wang, MediaTek, Hsin-Chu, Taiwan
Young-Jin Woo, Silicon Works, Daejeon, Korea
Jieh-Tsorng Wu, National Chiao-Tung University, Taiwan
Peter Chung-Yu Wu, National Chiao Tung University, Hsinchu, Taiwan
Yong Ping Xu, National University of Singapore, Singapore
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kanagawa, Japan
Taizo Yamawaki, Hitachi, Tokyo, Japan
Takefumi Yoshikawa, Panasonic, Kyoto, Japan

HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2015 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2015". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2015 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday, February 21	4:00 pm to 7:00 pm
Sunday, February 22	6:30 am to 8:30 pm
Monday, February 23	6:30 am to 3:00 pm
Tuesday, February 24	8:00 am to 3:00 pm
Wednesday, February 25	8:00 am to 3:00 pm
Thursday, February 26	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 16, 2015.** After January 16th, and on or before 11:59 pm Pacific Time Monday February 2, 2015, registrations will be processed **at the Late Registration rates. After February 2nd, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Monday February 2, 2015,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time February 2, 2015.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE Membership Saves on ISSCC Registration

Take advantage of reduced ISSCC fees by joining the Solid-State Circuits Society today, or by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email by using the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

SSCS Membership – a Valuable Professional Resource for your Career Growth

Get Connected! Stay Current! Invest in your Career! Membership in the Solid-State Circuit Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

SSCS Membership delivers:

- Networking with peers - Educational development - Leadership opportunities
- Tools for career growth - Recognition for your achievements

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuit Society where you can:

-Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid-State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and member-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. New publications included in your SSCS membership are the "RFIC Virtual Journal" and the "Journal on Exploratory Solid-State Computational Devices and Circuits", a new open access publication.

SSCS Membership Saves Even More on ISSCC Registration

This year, SSCS members will again receive an exclusive benefit of a $40 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuit Society today at sscs.ieee.org – you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

ISSCC Power Bank: A convenient rechargeable power bank for your portable devices will be given to all Conference registrants.

Publications: Conference registration includes:

-The **Digest of Technical Papers** in hard copy and by download. The Digest book will be distributed during registration hours beginning on Sunday at 10:00 am.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2015 for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to hear from an accomplished speaker, get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. This event is open to women only at a discounted fee.

OPTIONAL PUBLICATIONS

ISSCC 2015 Publications: The following ISSCC 2015 publications can be purchased in advance or on site:

2015 ISSCC Download USB: All of the downloads included in conference registration **(mailed in March).**

2015 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**

2015 Short Course DVD: "Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages" **(mailed in May)**.

Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVD contains a pdf file of the presentations suitable for printing, and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the order form for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $249 for a single/double, $269 for a triple and $289 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2015 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 30, 2015 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 30th, the group rates may no longer be available and reservations will be filled at the best available rate.**

Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

ISSCCx -- NEW THIS YEAR!

This year, for the first time, ISSCC will offer an online course titled ISSCC Previews: Circuit and System Insights, powered by the edX platform on the IEEEx school site. The online course will be provided at no cost to the public and will introduce several key circuit concepts and trends in a tutorial fashion, allowing participants to understand and appreciate the broad themes covered at ISSCC. The course is open to everyone for pre-registration at www.issccx.org and the lectures will be available December 1, 2014 until February 28, 2015.

These Previews will be in the form of eleven, 10-to-18 minute modules taught by leading experts that will establish the current state-of-the-art in several fields, including wireless and wireline communication, analog, digital, and memory. Each module will have a few optional questions to test the participant's understanding of the material covered.

REFERENCE INFORMATION

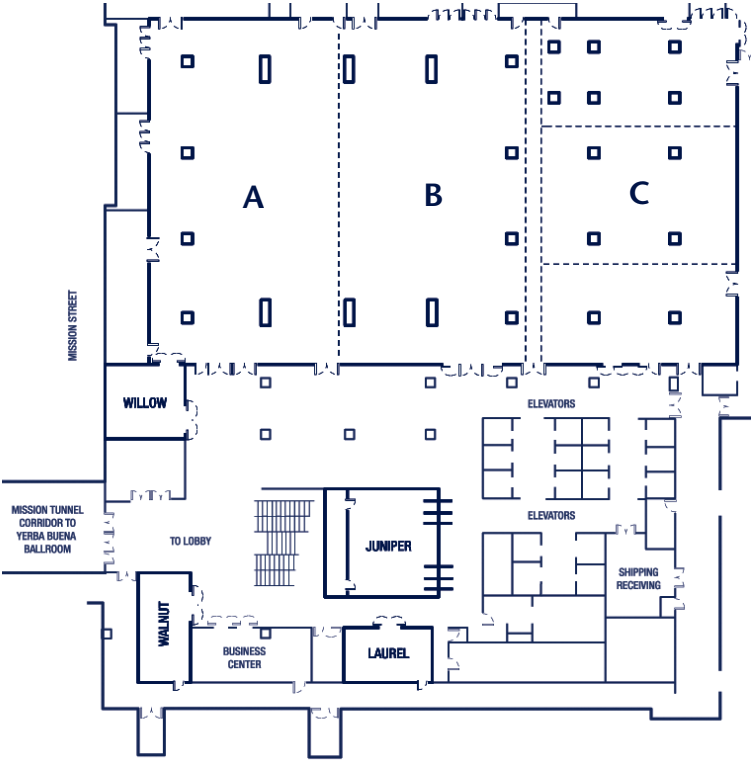
TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Registration questions:	ISSCCinfo@yesevents.com	
Hotel Information:	San Francisco Marriott Marquis 55 Fourth Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com	Phone: 416-418-3034
Registration:	YesEvents 1700 Reisterstown Road #236 Baltimore, MD 21208 Email: issccinfo@yesevents.com	Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

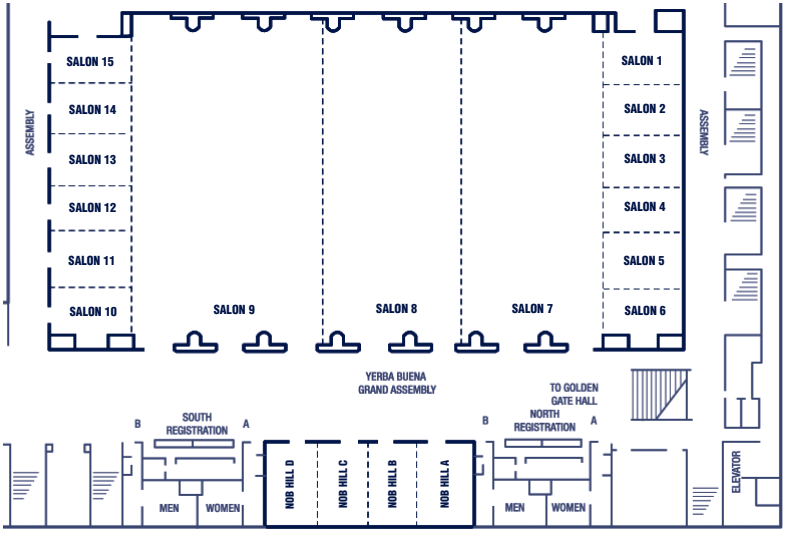
Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2016 will be held on January 31-February 4, 2016 at the San Francisco Marriott Marquis Hotel.

Golden Gate Ballroom



Yerba Buena Ballroom



445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

ISSCC.org

sscs.ieee.org

ISSCC 2015 ADVANCE PROGRAM