INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

ISSCC®

UNIVERSITY OF PENNSYLVANIA

2014

PRESS KIT

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 1, 2013, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

1. PREAMBLE

1.1 FAQ About ISSCC

1. What is ISSCC?
ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. ISSCC is the technical bell weather of the semiconductor circuit industry: According to the Semiconductor Industry Association (SIA), the semiconductor industry had US$290 billion in sales in 2012. ISSCC continues to be the premier technical forum for presenting advances in semiconductor, solid-state and integrated circuits and systems resulting from **Moore's Law**.

2. How Big is ISSCC?
Attendance at ISSCC 2014 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%** of the total.

3. Where is ISSCC?

The **61st year of ISSCC** will be held at the San Francisco Marquee Marriott on February 9-13, 2014. This has been its location since 1993.

4. How Does the Conference Formally Open?

ISSCC 2014 will kick-off with four exciting plenary speakers on Monday, February 10, 2014:

Mark Horowitz, Yahoo! Founder's Chair Stanford University, Stanford, CA, USA
Ming-Kai Tsai, Chairman and CEO MediaTek, Hsinchu, Taiwan
Erik H.M. Heijne, Instrumentation Physicist, CERN, Geneva, Switzerland
Susie Wee, VP and CTO of Networked Experiences, Cisco, Palo Alto, CA, USA

5. What Technical Areas are covered at ISSCC?
The Conference covers a spectrum of design approaches in various technical areas and advancements broadly categorized as: (1) Communication Systems; (2) Analog Systems; (3) Digital Systems; and (4) Innovative Topics, such as micro-machines, imagers, sensors, bio-medical, as well as developments that are three or more years away from commercialization.

6. Who selects papers to be presented at ISSCC?
Typically, over 600 papers are submitted for consideration each year. They are reviewed by an international team of over 150. Experts from Asian, Europe, and North America are organized into ten sub-committees that cover the 4 broad themes described above:

(1) For **Communication Systems** — RF, Wireless, Wireline Sub-Committees
(2) For **Analog Systems** — Analog, Data Converters Sub-Committees
(3) For **Digital Systems** — Energy-Efficient Digital, High-Performance Digital, Memory Sub-Committees
(4) For **Innovative Topics** — Imagers/MEMS/Medical Devices/Displays, Technology-Directions Sub-Committees

7. Is everything covered at ISSCC highly technical?

No, only the regular sessions (2 to 30) are intensely technical; The Plenary Session ranges from moderately technical to relatively non-technical; Evening Sessions are moderately technical; the Educational Sessions are narrowly specialist technical; the Demonstration Session are popularly technical; the Student Session is modestly technical.

8. What Sessions are of general interest?

This year, besides the Plenary, there are two Evening Sessions that are both broad and general, and likely to be of interest to both technical journalists and analysts: on Monday, February 10, 2014, an evening panel discussion on "Next-Generation Networked Systems— Challenges for Silicon" featuring **senior management** from SK Telecom, NVIDIA, Bosch, Qualcomm, ARM, and NTT; on Tuesday, February 11, 2014, an evening panel discussion on "Perspectives on the Semiconductor Industry and the future of semiconductor innovation" featuring **prominent CEOs** (including Broadcom, Cypress, ARM, IMEC, Etron) and **Venture Partners** (Tallwood, Kleiner Perkins, August) that invest in the semiconductor industry.

10. What companies are presenting this year at ISSCC?

Companies presenting technical papers e includes: ADI, AMD, ARM, Broadcom, Cypress, Fujitsu, IBM, Intel, Marvell, Maxim, MediaTek, Micron, Microsoft, NEC, Qualcomm, Renesas, Samsung, Sony, STMicroelectronics, TI, Toshiba, Xilinx, just to name a few. A more complete list can be seen in the Index.

11. Are there educational sessions?

ISSCC 2014 features the following educational sessions:

Ten Tutorials (targeted toward participants that are interested in new topics)
Six forums (targeted toward participants interested in sharing expert knowledge)
Short course (targeted toward participants interested in an in-depth learning experience in an annually-evolving field)

12. Are there any other activities besides technical and educational sessions?

Here is a complete list of activities that will be part of ISSCC 2014:

- A Plenary Session (4 presentations)
- 29 Technical Sessions (206 presentations)
- 5 Evening Sessions including a plenary panel, two regular panels and two special-topic evening sessions (SET)
- 17 Educational Sessions featuring:
  - Ten Tutorials (targeted toward participant broadening)
  - Six forums (targeted toward information sharing amongst experts)
  - Short course (targeted toward in-depth learning)
- Student Research Preview (targeted toward student broadening)
- Demonstration sessions from industry and academia (targeted toward deeper understanding)Networking social events (targeted toward bonding)
- Author interview sessions (targeted toward in-depth understanding)
- Women's networking event (targeted toward young women in engineering)
- Various university alumni events (targeted toward nostalgia)
- Book display (targeted toward attendee broadening)

13. How do I use this Press Kit?

The Press Kit provides a PREAMBLE section that features general information. The kit emphasizes TECHNICAL SESSION OVERVIEWS of 206 papers in 29 technical sessions, featuring pithy paper pitches! A following section expands upon highlighted papers (paper-number order) emphasizing underlying background and future significance. Another major section consists of technology trends (in alphabetical Sub-Committee order) emphasizing past challenges, current solutions, and potential directions. Finally, we have provided an INDEX section with multiple vectors: (a) 206 papers grouped by Subcommittee in paper-number order; (b) 206 papers grouped by technical areas in paper-number order; (c) 206 papers grouped by company/university/institution (in alphabetical order) in paper-number order.

1.2 ABOUT ISSCC 2014 – Silicon Systems Bridging the Cloud

The theme of ISSCC 2014 is "*Silicon Systems Bridging the Cloud*".

The "*cloud*" concept is rapidly revolutionizing the way we do business by enabling highly-scalable software services that can be perceived as intangible assets that leverage traditional hardware. Currently, such intangibilities include services such as *Dropbox*, *Amazon Web Services (AWS)*, *Google Maps*, and *YouTub*e. These services make us not only productive, but keep us entertained, to the extent that their creative intellectual value will likely be included in future rounds of gross-domestic product calculation!

While the trend toward an increasing value of intangible cloud-based services is undeniable, its foundation relies on tangible assets: hardware systems that are becoming faster, more-cost effective, and more computation- communication- and security-efficient — all thanks to silicon.

Correspondingly, the 2014 International Solid-State Circuits Conference (ISSCC) will address various aspects of the role that new silicon systems will play in further enabling the "*cloud*". ISSCC 2014 will be held at the San Francisco Marriott Marquis February 9–13, 2014.

1.3 PLENARY SESSION (Session 1)

- The plenary session, taking place on the morning of Monday, February 10th, will feature four invited speakers, as follows:
- Mark Horowitz, Yahoo! Founder's Chair, Stanford University, CA, will present "Computing's Energy Problem (and What We Can Do About It)"
- Ming-Kai Tsai, Chairman and CEO of MediaTek, Hsinchu, Taiwan, will present "Cloud 2.0 Clients and Connectivity— Technology and Challenges"
- Erik H.M. Heijne, Instrumentation Physicist, CERN, Geneva, Switzerland, will present "How Chips Pave the Road to the Higgs Particle and the Attoworld Beyond"
- Susie Wee, Vice-President and Chief Technology Officer of Networked Experiences, Cisco, Palo Alto, CA, will present "The Next Generation of Networked Experiences"

1.4 PLENARY EVENING PANEL

Next-Generation Networked Systems: Challenges for Silicon

Domain Experts and Circuit Designers — Friends or Foes?

Background:

Connecting diverse semiconductor devices through wireless and wired networks has become the preferred way to design systems that are at the leading edge of technical innovation. Such interconnected semiconductor systems are providing business advantages to the marketplace. However, system design is not yet unified, and in practice these systems are defined differently according to the *application area*, *implementation technology,* and the *individual engineer's background,* whether at the system or circuit level. This cacophonous lack of order presents fundamental challenges to circuit designers and circuit-design educators.

In this Evening Panel Session, several world-renowned experts both on the system side and on the traditional silicon side, will share their experience with, and vision for, the development of innovative systems based on semiconductor technology and circuits. Each expert will be asked to address the following issues:

- Does design primarily belong to the system architect or to the circuit designer?
- Is domain-specific knowledge (e.g., biomedical or automotive) essential for system development?
- Can the domain expert alone, rather than the system architect, design and develop a system as the principal engineer?
- Alternatively, is it possible for the circuit designer to provide a "system platform" to the domain experts for their applications?
- Are there any good examples in which semiconductor technology and circuits are the primary contributors to the creation of an innovative system?
- Are integration of MEMS or of temperature-sensing circuits, on an SoC, good examples?

Panellists:

Alex Jinsung Choi, *SK Telecom, Seoul, Korea*
William Dally, *NVIDIA, Santa Clara, CA*
Stefan Finkbeiner, *Bosch Sensortec, Stuttgart, Germany*
Robert Gilmore, *Qualcomm, San Diego, CA*
Mike Muller, *ARM, Cambridge, UK*
Atsushi Takahara, *NTT, Yokosuka, Japan*

1.5 CEO/VC EVENING PANEL

Perspectives on the Semiconductor Industry, and the Future of Semiconductor Innovation

Background:

ISSCC has organized a long-overdue panel on "Call for Leadership", one which will seek the perspective of industry leaders on the semiconductor industry, and its future need for discontinuous innovation.

While, logically, we are not near the end of semiconductor innovation, only 3 semiconductor start-ups were funded in 2011 (with no exits), compared to 39 in 2004 (with 10 exits) [source: Cohort Analysis — www.seedtable.com/world/semiconductor]. What are the forces behind this trend? Are VCs funding other areas? Is our current funding model for semiconductor innovation broken?

In any case, significant innovation will be needed across a broad spectrum of technologies to fuel the insatiable demand for enhanced user experience in portable systems. Thus, for mobile computing, any slowdown in the improvement in MIPS/W will require a speed up in the increase in energy density (Wh/L) of battery technology. Further, for cloud services, the cost of power delivery and cooling is a significant percentage of its OPEX, and must be reduced to sustain growth. In the solution of such problems, lack of semiconductor innovation will result in anaemic improvement in MIPS/W/$, and will therefore impact the growth rate of mobile and cloud computing.

This panel which includes representatives of service and system providers will be asked if their future needs are likely to be met by following the current silicon roadmap, or if increased investment in semiconductor innovation is required.

Panellists:

An ensemble of Visionaries — Venture Partners and CEOs — will discuss the opportunities and challenges for innovation in the semiconductor industry:

Representing Venture Partners:

- **Dado Banatao,Tallwood,** might be considered as a candidate for "The Last Man Standing" in semiconductor investments. He continues to invest in unique and challenging semiconductor-technology solutions for computing, communication, and consumer platforms. Banatao has led investments in Marvell, Inphi, SiRF, Wilocity and many other semiconductor companies. He is currently Chairman of Ikanos.
- **John Doerr, KPCB,** and his partners have backed some of the world's most successful entrepreneurs at Google, Amazon, Intuit, Zynga. and Twitter. Ventures sponsored by Doerr have created more than 200,000 new jobs.
- **Andy Rappaport, August Capital**, has been involved in the formation and success of several start-ups, including Transmeta, Viewlogic, Actel, and Silicon Architects. At August, he funded Atheros, Escalade, Genoa, Adaptive and Silicon Image. He serves on the Board of SuVolta, Luxtera, and Magnum Semiconductor.

Representing CEOs:

- **Nicky Lu is CEO and President of Etron Technology,** a public Taiwanese fabless IC design and product company specializing in memory and SoCs. He is a vocal proponent of entrepreneurship, and serves on the board of the Taiwan Semiconductor Industry Association (TSIA), and as Chairman of the Global Semiconductor Alliance (GSA).
- **Scott McGregor is CEO and President of Broadcom.** Since he joined Broadcom in 2005, the company has expanded from $2.40 billion in revenue, with 3,250 employees, to $8.01 billion in 2012, with 11,750 employees. Broadcom has acquired over 50 innovative semiconductor start-ups including Netlogic.
- **TJ Rodgers is CEO and President of Cypress Semiconductor.** Business Week's "*Bad Boy of Silicon Valley*" is a perpetual entrepreneur who has launched a series of autonomous businesses that have relied on the parent company for funding in much the same way as startup companies rely on venture capital. Examples include: Cypress Microsystems (creator of PSoCs); and SunPower which was spun out of Cypress in 2008 for $2.6 billion.
- **Simon Segars is CEO of ARM**, Forbes magazine's #1 innovative company in Europe in 2012. He is a long term veteran of ARM with a variety of roles and experiences representing insights in fabless semiconductor modeling and IP models.
- **Luc Van den hove is CEO of imec**, a world leading nano-electronics research organization headquartered in Europe, who leverages global partnerships to deliver industry-relevant solutions utilizing innovations.

An ISSCC audience consisting of experts in the field, inventors, entrepreneurs, researchers, young professionals, and students will challenge the panelists, stimulating their views of the prospects of future innovation in our industry.

Concerns and Questions:

Our primary concern is the reduction in funding available for new semiconductor ventures. Are the escalating NRE costs of ASICs and designs providing a barrier to new entrants? Are there any new entrants in technology?

What advice would you give to entrepreneurs thinking of starting a semiconductor company?

Many of the semiconductor platforms for future systems will be delivered by Multi-National Corporations (MNCs). For the MNC CEOs on the panel, we will ask whether, going forward, they are increasing their investment in innovation, or if a strategy of acquisition is sustainable for growth. It is likely that the VCs will have something to say on this matter.

Are funding sources (and incentives) in offshore markets shifting the focus of semiconductor innovation to regions such as China, The Middle East, Brazil, and Russia? Are there pitfalls in following this trend? Should governments do more to support small companies? If public-funded institutes and universities provide the research, must governments also fund the commercialization of this research into semiconductor products?

Is the fabless semi model being displaced by the IP model?

Is there a future for bright students and young entrepreneurs in the semiconductor industry?

1.6 A PANTHEON-OF-EXPERTS EVENING PANEL

As process scaling slows down, circuit innovation is becoming one of the most important product differentiators. One can point to great circuit inventions of the past that were accidental, or failed attempts to solve other problems (bugs), as well as those that result from logical thinking (features). Which is more effective?

The evening panel, "Anatomy of Innovation: Bug or Feature?, onTuesday, February 11th will focus on this delimena. In this panel, leading analog-circuit experts (listed below) describe the process by which their best innovations were conceived. They will reveal interesting anecdotes from their experiences, such as turning a bug into a feature. Then, they will discuss which is most effective, accidental discovery or logical thinking.

- Ali Hajimiri, Caltech, Pasadena, CA, USA
- Qiuting Huang, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland
- Lawrence Loh, MediaTek Inc., Hsinchu, Taiwan
- Kofi Makinwa, Delft University of Technology, Delft, Netherlands
- Akira Matsuzawa, Tokyo Institute of Technology, Tokyo, Japan
- Dennis Monticelli, Texas Instruments, Santa Clara, CA, USA

ISSCC 2014
SESSION OVERVIEWS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2014 in February in San Francisco

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 61st appearance of ISSCC, on February 9th to the 13th, 2014, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2014, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 9-13, 2014, at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview:
Ultra-High-Speed Transceivers and Techniques
WIRELINE SUBCOMMITTEE

Session Chair: *Ken Chang, Xilinx, San Jose, CA*
Session Co-Chair: *Koichi Yamaguchi, Renesas Electronics, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

The rise of cloud computing and mobile communications has driven an explosion in the need for data communication bandwidth, making efficient wireline transceivers that work at the limits of the process technology increasingly critical. Techniques to reduce the power consumed by the sophisticated equalization and clocking circuits necessary to operate over lossy electrical channels are therefore required. This session includes 9 papers in this area, addressing topics of 28Gb/s transceivers, a 60Gb/s transmitter, sub-250fJ/b equalizers at 16 to 25Gb/s, and robust TX equalization and clock generation/recovery designs.

- In Paper 2.1, LSI presents a multi-standard 28Gb/s transceiver implemented in 28nm CMOS and consuming 560mW per channel. The design's AFE provides 15dB of boost, while the DFE uses a half-rate 1-tap unrolled architecture. Over a 34dB test channel, the horizontal eye margin is 0.49UI and the vertical margin is 99mV.

- In Paper 2.2, Broadcom describes a 4×28Gb/s transceiver supporting 100GbE/40GbE standards realized in 40nm CMOS. The TX incorporates a 3-tap FIR with output-phase adjustment, and the RX uses a half-rate CDR with a dedicated eye-monitor channel. The transceiver dissipates 780mW from a 0.9V supply and achieves a BER $<10^{-15}$ over a 20dB-loss channel at Nyquist.

- In Paper 2.3, National Taiwan University, introduces fully-integrated 60Gb/s NRZ and PAM4 transmitters in 65nm CMOS. The NRZ transmitter consumes 450mW of power and the PAM4 TX consumes 290mW, both from a 1.2V supply.

- In Paper 2.4, UCLA presents a 25Gb/s receiver that includes a one-stage CTLE and a half-rate/quarter-rate two-tap DFE. The design is fabricated in 45nm CMOS and uses charge-steering techniques to equalize for a Nyquist channel loss of 24dB. The circuit delivers an eye opening of 0.4UI for BER $<10^{-12}$ and performs 4× demultiplexing while drawing 5.8mW from a 1V supply.

- In Paper 2.5, Oregon State University describes a 16Gb/s 3-tap DFE implemented in 65nm GP CMOS that uses a charge-based sampling circuit and is capable of operating down to a 0.7V supply. The DFE achieves 0.46UI margin at BER $<10^{-12}$ over 18dB of channel loss with 0.25pJ/b energy efficiency.

- In Paper 2.6, POSTECH presents a DLL-based referenceless CDR for intra-panel interfaces. Using a pattern-dependent clock-embedded signaling scheme, clock information is transmitted with an overhead of only one bit for each data packet. The CDR is implemented in 65nm CMOS and achieves a power efficiency of 0.63mW/Gb/s at 9Gb/s.

- In Paper 2.7, POSTECH introduces a coefficient-error-robust transmitter architecture that uses channel loss to suppress the impact of coefficient errors. An implementation fabricated in 65nm CMOS operates at 8Gb/s over a 17.5dB-loss channel and improves the eye variation by more than 2× compared with a conventional FFE transmitter with only 27% area overhead.

- In Paper 2.8, UC Berkeley/Xilinx describe a 16GHz injection-locked 20nm ring oscillator employing pulse-position modulation that reduces flicker noise through feedback control. Compared to conventional injection-locking, jitter reduces from 434 to $268fs_{rms}$. The circuit consumes 46.2mW with an area of $0.044mm^2$.

- In Paper 2.9, Politecnico di Milano presents a circuit to control the bandwidth and frequency response of a digital PLL. The technique ensures that the loop bandwidth remains independent of analog parameters and does not require injection of extra signals into the loop. When embedded in a 65nm CMOS bang-bang 2.9-to-4.0-GHz PLL, it sets the bandwidth in the 100-to-2MHz range with 4% accuracy independent of input noise level.

Session 3 Overview: *RF Techniques*

RF SUBCOMMITTEE

Session Chair: *Masoud Zargari, Qualcomm-Atheros, Irvine, CA*
Session Co-Chair: *Tae Wook Kim, Yonsei Univ., Seoul, Korea*

Subcommittee Chair*:* *Andreia Cathelin, STMicroelectronics, Crolles, France, RF Subcommittee*

In recent years the use of CMOS technology has enabled the integration of low-cost, low power and multi-standard RF transceivers. While architectural innovation has allowed most of the transceiver blocks to be integrated in a single chip, full compliance to wireless standards still demands that many off-chip components be added to achieve the overall solution. The papers presented in this session focus on increasing the level of integration of several key building blocks of wireless transceivers. The first part of the session is focused on the transmitter side and in particular on several closed-loop techniques to maximize the output power delivered to the antenna. The second part of the session gives an overview of the most recent techniques applied to the receiver path. Three wideband solutions compliant to software-define-radio (SDR) are presented, followed by a state-of-the-art tuner and a novel beamforming receiver.

- In Paper 3.1, Toshiba proposes a new on-chip antenna impedance detection technique, which improves PAE by 1.5x in a 0.13μm 3G/4G CMOS Power Amplifier.

- In Paper 3.2, Fujitsu Laboratories presents a fully integrated EER CMOS PA in 90nm for WCDMA and LTE. Power efficiencies of 34.1% and 32.2% were achieved for LTE10MHz and LTE20MHz respectively.

- In Paper 3.3, KU Leuven presents a novel on-chip true-rms power detector in 40nm CMOS. The power detector allows measuring the power under varying antenna impedances. The measured input range for a linearity error within ±0.5dB is 32.5dB at 5GHz.

- In Paper 3.4, KU Leuven presents a dual-mode transformer-based Doherty LTE PA in 40nm CMOS that is 2x more efficient at power back-off compared to previous CMOS LTE PAs.

- In Paper 3.5, The University of Twente and TNO present a 4-element beamforming receiver with new constant-G_m vector-modulator topology in 65nm CMOS. This enables a low power consumption of 6.5-to-9mW per element in a 1.0-to-2.5GHz RF band with a 73dB spurious-free dynamic range

- In Paper 3.6, Broadcom presents a sub-2dB noise-cancelling receiver in 28nm CMOS that boosts large-signal resilience to blockers located at integer multiples of LO harmonics by more than 20dB.

- In Paper 3.7 KAIST, UT Dallas and PHYCHIPS present a TV tuner front-end in 0.13μm CMOS that shows an exceptional linearity performance over the whole front-end gain range with state-of-the-art harmonic-rejection ratio (>83dB HRR3, >89dB HRR5, and >68dB HRR7).The LNA shows >+27dBm OIP3 at 22dB of voltage gain. Contrary to the previous works the 2-stage harmonic rejection is done in baseband, which makes it more resilient to gain mismatch.

- In Paper 3.8 TU Delft presents the first discrete-time superheterodyne receiver with complex BPF in 65nm CMOS. This highly reconfigurable RX covers the input frequency range of 1.8 to 2.5GHz with 0.2-to-20MHz BW and achieves uncalibrated IIP2 of > +85dBm. The power dissipation of the entire chain (up to the ADC) is 55 to 65mW.

- In Paper 3.9 The University of Macau and Instituto Superior Tecnico present an RF-BB current-re-use receiver with parallel N-path mixers to alleviate the tradeoff between NF and power. The 65nm CMOS receiver achieves 4.6±0.9dB NF, +61/+17.4dBm out-of-band IIP2/IIP3 and >51dB HRR2-6, without external parts or calibration.

Session 4 Overview: *DC-DC Converters*

ANALOG SUBCOMMITTEE

Session Chair: *Wing-Hung Ki, HKUST, Hong Kong, Hong Kong*
Session Co-Chair: *Christoph Sandner, Infineon, Villach, Austria*

Subcommittee Chair: *Axel Thomsen, Silicon Labs, Austin, TX, Analog Subcommittee*

To meet the challenges of dynamic power requirements of diverse electronic applications, both high performance switched-mode and switched-capacitor DC-DC converters are indispensable. In the first part of the session, switched-mode power converters catering to multi-core SoCs (system-on-chips) are presented. They have to switch at frequencies into the 10MHz regime for small form factor, to have multi-phase for ripple reduction, fast control in response to large and fast load current changes, and fast reference tracking for dynamic voltage scaling.

The second part of the session is dedicated to Switched-Capacitor (SC) DC-DC converters. With technical advances allowing power levels of several watts, they find their way into applications where inductor-based DC-DC converters have dominated over the last decades. Several techniques are shown to increase both efficiency and power density. This is achieved by making use of multi-phase and reconfigurable architectures.

- In Paper 4.1, by Toshiba, a 3-phase digitally controlled DC-DC converter with 84%-to-90% efficiency over 0.4A-to-9A load range is presented. A 1-cycle fast phase adding/dropping scheme is proposed, offering less than 10mV ripple, 88% reduction from the optimal PID control.

- In Paper 4.2, by the University of Dallas, Texas, a 40-MHz 4-phase ZDS hysteretic converter achieves 1% settling time of 230ns for 5A/5ns load step with C_{OUT}=940nF and 9.8% droop at 1.2V. The ZDS control enables 6x lower switching frequency without affecting the transient response.

- In Paper 4.3, by Fudan University, a ripple-based adaptive on-time control method is proposed and proven in a DVS-capable single-Inductor 4-output DC-DC buck converter to overcome the cross-regulation problem. The converter achieves ripple below 30mV and 87% peak efficiency.

- In Paper 4.4, by HKUST, a 10/30MHz buck converter that features a high-accuracy delay-compensated ramp generator and an area-efficient Type-III compensator built around a differential difference amplifier (DDA) that also facilitates reference-tracking is presented. The measured maximum output power is 3.6W.

- In Paper 4.5, by Dartmouth College, a chip-scale resonant switched-capacitor (ReSC) converter is presented that can provide up to 4.6W at 0.64 W/mm² with over 82% efficiency. The 2-phase, nominally 2:1 converter uses fully integrated MIM capacitors with die-attached 1.9 nH air-core solenoid inductors.

- In Paper 4.6, by the University of California, San Diego, a recursive switched-capacitor topology is implemented that provides 15 conversion ratios for high efficiency over a wide output voltage range. The topology opportunistically connects individual 2:1 SC cells while maximizing capacitance utilization.

- In Paper 4.7, by ETH Zurich, an on-chip switched-capacitor DC-DC voltage regulator in 32nm SOI CMOS for microprocessor power delivery is presented. A reconfigurable power stage regulates the output voltage between 0.7 to 1.1V from a 1.8V input supply. The power density is up to 3.1 W/mm^2.

- In Paper 4.8, by NXP Semiconductors, a 3-phase switched-capacitor boost converter using only 2 external floating capacitors and providing 16V output from a 3.3V input is presented. It reaches an efficiency of 70.3% at 7mA load current. The volume is 15x smaller compared to competitive inductive converters.

Session 5 Overview: *Processors*

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Atsuki Inoue, Fujitsu, Kawasaki, Japan*
Session Co-Chair: *Christopher Gonzalez, IBM, Yorktown, NY*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

As compute power is increasingly migrated to large data centers and the cloud, microprocessors face progressively more stringent design constraints. This year's processor session introduces 5 new processors providing increased performance and power efficiency. In addition to growing core counts, cache size, and thread count, the historical theme of integration continues as voltage regulators are now being implemented on chip. Other papers in this session demonstrate creative self-monitoring and adaptive techniques to meet power and performance design goals.

- In Paper 5.1, IBM presents the POWER8™ microprocessor featuring 12 cores and 96MB of on-chip L3 cache. The chip is implemented in 22nm SOI eDRAM technology with 15 levels of metal. The processor features 7.6Tb/s off-chip bandwidth, integrated voltage regulation and resonant clocking.

- In Paper 5.2, IBM demonstrates a distributed system of micro-regulators implemented in 22nm eDRAM technology for power management of the POWER8™ microprocessor. With a 12.3A load, the micro-regulators achieve a power efficiency of 90.5% and power density of 36W/mm^2.

- In Paper 5.3, IBM describes the resonant clocking architecture implemented in the POWER8™ microprocessor. The multimode resonant design can oscillate from 2.5GHz to greater than 5GHz, reduce clock grid power by 33% and can dynamically switch between high and low resonant frequency modes without idle cycles.

- In Paper 5.4, Intel introduces the Ivytown Xeon® processor containing 15 cores, and 37.5MB shared L3 cache. The processor has 4.31B transistors in a high-κ metal-gate tri-gate 22nm CMOS technology with 9 metal layers. It features an enhanced ring bus topology, a 1 PLL per column clocking structure and a multimode memory interface.

- In Paper 5.5, AMD presents their latest x86 core, Steamroller. It is implemented in 28nm occupying 29.47mm^2, with more than 236 million transistors. A shared 96KB 3-way instruction cache and 10KB L2 branch target buffer improve single and multi-threaded performance as compared to a previous 32nm design. Power reduction is achieved by resonant clocking, power supply monitors and power gating techniques.

- In Paper 5.6, AMD demonstrates a real-time voltage-droop detector which triggers the clock to adapt to falling voltage, allowing frequency to be maintained at lower voltage and achieving power efficiency improvements of 7 to 15%.

- In Paper 5.7, Intel presents a graphics execution core implemented in 22nm tri-gate CMOS incorporating an adaptive clocking technique for fast voltage-droop mitigation, and an all-digital retention voltage clamp for reduced leakage during state-retentive sleep mode. The core offers 12-27% power savings, wide voltage operation down to 0.38V, and 40% improvement in peak GFLOPS/W.

- In Paper 5.8, Applied Micro reveals the first generation 64b v8 ARM 8-core processor. Featuring a 4-wide out-of-order superscalar micro-architecture, the processor is fabricated in 40nm bulk CMOS technology, and operates at 3GHz with a 0.9V supply, consuming 4.5W.

- In Paper 5.9, Intel describes the 4th Generation Intel® Core™ processor Haswell implemented in a 22nm tri-gate process. It fully integrates voltage regulators improving battery life by ~50%, improves graphics by extending the cache hierarchy with eDRAM providing 102GB/s bandwidth at 1.22pJ/b, adds lower power states reducing standby power by 95%, has optimized I/O interfaces, and doubles floating point operation capability.

Session 6 Overview:
Technologies for High-Speed Data Networks

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Pirooz Parvarandeh, Maxim Integrated, San Jose, CA*
Session Co-Chair: *Chris Nicol, Wave Semiconductor, Sunnyvale, CA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

Increasing data rates require the use of a number of technologies to achieve high data throughput while minimizing power consumption. The papers in this session showcase industry-led innovations that underpin future high-speed data networks. The first paper maximizes inter-chip data rates while lowering power consumption for memory architectures in high-speed switches. The second paper utilizes advanced DSP techniques to enable high-capacity optical networking systems. The third paper demonstrates the integration of high-performance data converters with 28nm FPGAs. The first and third papers also demonstrate the benefits of 3D integration.

- In Paper 6.1, *Cypress Semiconductor*, a 3D IC for 400Gb/s Ethernet improves bandwidth between a packet processor and memory by using an interposer, thus lowering power in router line cards. This paper provides a perspective on the challenges of implementing high-speed data networking systems.

- In Paper 6.2, *NTT Network Innovation Laboratories,* a digital signal processor ASIC for 100Gb/s coherent optical communications is reported. It incorporates Low Density Parity Check (LDPC) Forward Error Correction (FEC) and Multiple Input Multiple Output (MIMO) detection, and enables high-capacity optical transport networks achieving more than 8Tb/s/fiber. This paper additionally discusses the advancements that are required to achieve a 1Pb/s/fiber capacity.

- In Paper 6.3, *Xilinx,* ultra-high integration of two 28nm FPGA dice and two 65nm mixed-signal dice on a 65nm interposer realizing a 3D solution in a BGA package is demonstrated. The digital-to-analog converters achieve SFDR > 63.8dBc to 400MHz at 1.6GS/s. The ADC attains SNDR > 61.6dBFS to Nyquist at 500MS/s with an interface power of 0.3mW/Gb/s and analog isolation > 92dB.

Session 7 Overview: *Image Sensors*

IMMD SUBCOMMITTEE

Session Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*
Session Co-Chair: *David Stoppa, Fondazione Bruno Kessler, Trento, Italy*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

This session presents recent advancements in the field of image sensors such as: process improvements for back-side-illuminated CMOS sensors, low-power sensors for wireless applications, high-speed image processing for feature extraction and recognition, as well as recent advancements in time-of-flight sensors.

- In Paper 7.1, Samsung Electronics presents a 1/4-inch 8Mpixel CMOS image sensor with back-side-illuminated 1.12μm pixels. Each pixel is fully surrounded by front-side deep-trench isolation and includes a vertical transfer gate. This technology leads to a reduction of the optical crosstalk from 19% to 12.5%, and to an increase in linear full-well capacity from 5,000 to 6,200 electrons.

- In Paper 7.2, the University of Michigan reports a bio-inspired analog/digital mixed-mode 2D optical flow sensor for artificial compound eyes. The sensor estimates 2D optical flows from the integrated mixed-mode algorithm core, providing 2D 16b optical flows or compressed frames up to 120fps. The 2D flow estimation core consumes 243.3pJ/pixel.

- In Paper 7.3, the Chinese Academy of Sciences (with Tsinghua University) presents a vision chip in a 0.18μm process, which integrates an image sensor consisting of 256×256 pixels together with three von Neumann-type parallel processors and a self-organizing map (SOM) neural network. The SOM network can be reconfigured into an array processor in 3 clock cycles. The SOM network enables face recognition at 1340fps with a recognition accuracy of 86%.

- In Paper 7.4, Shizuoka University (with Brookman Technology) presents a 413×240-pixel CMOS Time-of-Flight (ToF) range imager with pinned photodiode high-speed lock-in pixels. The lock-in pixel structure uses lateral electric field control to implement a multiple-tap charge modulator. A range resolution of 4-to-6.4mm, with a light pulsewidth of 13ns, is measured for the range of 0.8 to 1.8m. Range data can be calculated for every frame.

- In Paper 7.5, Shizuoka University presents a 132×120-pixel CMOS ToF range imager with 0.3mm resolution at 32mm range. The ToF imager employs an indirect ToF measurement technique using pulse photocurrent response and draining-only modulation pixels. Furthermore, a column gating-clock skew calibration scheme allows a timing skew of 8ps rms.

- In Paper 7.6, Microsoft describes pixel and signal path of a 512×424-pixel ToF image sensor. Consecutive frames with different modulation frequencies are combined, which enables a range error of less than 1% over ranges from 0.8 to 4.2m. Modulation frequencies up to 130MHz are supported, and the modulation contrast at 50MHz is 67%.

Session 8 Overview: *Optical Links and Copper PHYs*

WIRELINE SUBCOMMITTEE

Session Chair: *Ichiro Fujimori, Broadcom, Irvine CA*
Session Co-Chair: *Hideyuki Nosaka, NTT, Kanagawa Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, Wireline Subcommittee*

Cloud computing requires interconnect solutions for distances ranging from tens of kilometers to less than one meter, driving the demand for advances in both optical links and copper-based Ethernet PHYs. The power consumption, cost, data-rate, and density of these designs must all be improved simultaneously, driving innovation in both the circuit and system architectures. This session includes 9 papers, including demonstrations of a highly parallel short-reach 60×10Gb/s optical interconnect, linear as well as non-linear techniques for electronic dispersion compensation of optical-component non-idealities at 6 to 25Gb/s, and a driver enabling a VCSEL rated for 25Gb/s to operate at 40Gb/s. Similarly, a new 10GBASE-T analog front-end and a GPHY driver architecture with rail-to-rail full-duplex operation demonstrate power savings for Ethernet PHY applications. Finally, two new CDR architectures enable robust frequency acquisition and low-jitter clock recovery in reference-less systems.

- In Paper 8.1, KAIST presents an electronic-dispersion-compensation circuit (EDC) for directly modulated distributed feedback lasers in 90nm CMOS. At 6Gb/s, the EDC consumes 68mW and achieves OSNR gains of 11.7dB and 14.7dB for 50km and 75km length optical cables, respectively.

- In Paper 8.2, Sony demonstrates a 600Gb/s optical interface using a 12×5 two-dimensional arrays of VCSELs, photodiodes, and opto-electronic drive/receive circuits. Using 60 links operating at 10Gb/s fabricated in 65nm CMOS, the input sensitivity is $13.3\mu A_{pp}$ at a BER of 10^{-12}.

- In Paper 8.3, the University of Pavia describes a power-scalable continuous delay-based equalizer for electronic dispersion compensation in multi-mode fibers that operates over a wide range of data-rates. Fabricated in 28nm LP CMOS, the equalizer power scales from 55 to 90mW as the data-rate scales from 10 to 25Gb/s.

- In Paper 8.4, TSMC presents an area- and power-efficient optical receiver. Using a shared inductor, the 28nm CMOS prototype achieves a power efficiency of 1pJ/b and an area reduction of 56% compared to an implementation without inductor sharing. At a BER of 10^{-12}, the vertical eye opening is >0.25UI at 25Gb/s.

- In Paper 8.5, Broadcom describes an analog front-end (AFE) for a 4-port 10GBASE-T transceiver chip in 40nm CMOS including transmitter, receiver, and hybrid. For a cable length of 100m supporting full 10Gb/s traffic, the AFE dissipates <1.75W, the lowest power for a 10GBASE-T AFE reported to date.

- In Paper 8.6, Broadcom presents a driver architecture that enables rail-to-rail full-duplex operation to improve driver efficiency. The architecture is demonstrated in a 2.5V GPHY driver in 28nm CMOS, with the reduced supply resulting in a 24% power reduction as compared to the mainstream 3.3V drivers.

- In Paper 8.7, University of Illinois at Urbana-Champaign demonstrates a BBPD-based automatic frequency acquisition scheme that has unlimited acquisition range and is immune to transition-density variation. The digital CDR, implemented in 65nm CMOS, has a range of 4 to 10.5Gb/s, consumes 22.5mW, and achieves 0.2MHz jitter-transfer bandwidth and 9MHz jitter tolerance.

- In Paper 8.8, the UC Irvine describes an 8.2-to-10.3Gb/s full-rate reference-less CDR in 0.18µm CMOS that uses an asymmetric phase-detector transfer curve for frequency detection. The 10.3Gb/s CDR achieves an out-of-band jitter tolerance of $0.58UI_{pp}$ with 2^{31}-1 PRBS.

- In Paper 8.9, Fujitsu presents a 40Gb/s driver IC over-driving a 25Gb/s VCSEL using a group- delay-compensation circuit for the pre-emphasis. The VCSEL driver achieves 40Gb/s operation with optical modulation amplitude of 2.3dBm and power consumption of 312mW.

Session 9 Overview: *Low Power Wireless*

WIRELESS SUBCOMMITTEE

Session Chair: *Jan Crols, AnSem, Heverlee, Belgium*
Session Co-Chair: *Alyosha Molnar, Cornell University, Ithaca NY*

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Helsinki, Finland, Wireless Subcommittee*

Low power transceivers for short-range wireless communication are emerging in a wide range of frequencies and bandwidths. This session starts with a full SOC for near-field communication (NFC). It then covers two low-power ultrawideband radios. After that, five radios for ISM band operation at 433MHz, 900MHz and 2.4GHz are presented, each demonstrating different architecture and circuit choices to achieve the lowest possible power consumption without compromising bit rate and output power (TX) or sensitivity level (RX).

- In Paper 9.1, Mediatek presents a near-field communication (NFC) transceiver SOC supporting card emulation mode, reader mode and peer-to-peer mode. The radio supports cm-range communication at 13.6MHz and fills 1.1mm^2 in 0.11µm CMOS.

- In Paper 9.2, Tsinghua University presents an ultra-wideband transceiver in 65nm CMOS that supports 500Mb/s at 1m range while consuming only 13.3mW. The system meets FCC spectral mask requirements through a combination of high-bit-rate OOK modulation and frequency hopping.

- In Paper 9.3, Tsinghua University and Samsung present an ultra-wideband transceiver in 65nm CMOS that provides 1Mb/s communication while consuming only 1mW. The system enables low-power synchronization through a low duty cycle, pulsed-chirp spread-spectrum approach.

- In Paper 9.4, The University of Macau and Instituto Superior Technico present a ZigBee receiver in 65nm CMOS for the 433-to-960MHz bands, achieving an 8.1dB Noise Figure while consuming 1.15mW. The receiver demonstrates new techniques for current reuse, and employs N-path feedback and downconversion to reuse the input LNA for both RF and baseband signals.

- In Paper 9.5, imec presents a 2.4GHz receiver in 65nm CMOS employing a digital phase-tracking loop to perform direct phase-to-digital conversion. The receiver achieves -92dBm sensitivity for 2Mb/s signals in the IEEE 802.15.4 standard while consuming 2.4mW.

- In Paper 9.6, Oregon State University and Fudan University present a 2.4-to-2.7GHz WBAN receiver in 65nm CMOS, able to demodulate 971kb/s signals with -90dBm sensitivity while consuming 1.05mW. The receiver combines a Q-enhanced LNA with sub-sampling to provide low power downconversion with minimal noise folding.

- In Paper 9.7, imec, Eindhoven University of Technology and Fujitsu present a 400-to-450MHz IEEE 802.15.6 transceiver in 40nm CMOS for medical applications, employing digitally reconfigurable circuits to support modulation schemes and data rates from 11.7kb/s to 4.5Mb/s. The receiver achieves a sensitivity as low as -112dBm while consuming 2.2mW.

- In Paper 9.8, imec and Delft University of Technology present a 2.1-to-2.7GHz Frequency Modulator in 40nm CMOS for ZigBee and Bluetooth Smart, employing an all-digital fractional-N PLL with two-point modulation. The PLL employs a snapshot TDC to provide <1.7ps jitter while consuming 0.86mW.

Session 10 Overview: *Mobile Systems-on-Chip (SoCs)*

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: *Vasantha Erraguntla, Intel, Bangalore, India*
Session Co-Chair: *Takashi Hashimoto, Panasonic, Fukuoka, Japan*

Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO, Energy-Efficient Digital Subcommittee*

Mobile SoCs are becoming extremely complex to meet the relentless demand for more compute power and a richer user experience in mobile applications. Qualcomm's Hexagon DSP in 28nm CMOS consumes 58μW/MHz at 0.6V, while Renesas and MediaTek present multicore heterogeneous processors with low power to achieve long battery life and boost performance by exploiting thermal headroom. A multicore processor from KAIST delivers a rich user experience with a 30fps 720p augmented reality chip for wearable electronics. To minimize standby-power, NEC introduces a 16b MTJ-based non-volatile microcontroller with low wakeup time among NV SoCs. Additionally, power-efficient digital baseband SoCs from imec, the Technical University of Dresden and Ericsson are presented, which support multi-standard communication at low power using fine-grain power management techniques.

- In Paper 10.1, Qualcomm presents their 28nm Hexagon™ DSP optimized for mobile heterogeneous computing with an on-chip LDO. The DSP operates from 255MHz at 0.6V, up to 1.20GHz (5640 DMIPS) at 1.05V. With the LDO, the DSP consumes 58μW/MHz at 0.60V. The leakage is 4.08mW at 0.90V.

- In Paper 10.2, Renesas describes a 28nm heterogeneous quad/octa-core mobile application processor. The high-performance cores and the low-power cores operate at 2GHz and 1GHz, respectively, to achieve a maximum performance of 35600 DMIPS. A 24% reduction in SRAM leakage is achieved using a long-length transistor in the word driver and the timing generator. 20% and 29% reductions in dynamic and leakage power, respectively, are accomplished by employing adaptive-voltage-scaling techniques.

- In Paper 10.3, MediaTek presents a 28nm heterogeneous multi-processor in a mobile SoC, consisting of a dual-core ARM Cortex™-A15 and a dual-core Cortex-A7. Various power, thermal and performance optimizations techniques deliver 23% higher clock speed, or up to 41% power savings. A new adaptive thermal management algorithm is also introduced. The chip operates between 0.85-1.25V, with the A15 cores reaching 1.8GHz and the A7 cores reaching 1.4GHz.

- In Paper 10.4, KAIST describes a real-time markerless 1.22TOPS augmented reality multicore processor with a neural network NoC for wearable applications. This 4×8mm^2 65nm processor consumes 1.52mW/MHz for a 30fps 720p augmented-reality operation. The operating range with DVFS is 65MHz at 0.7V to 250MHz at 1.2V.

- In Paper 10.5, NEC and Tohoku University presents a 4.79×4.79mm^2 fully non-volatile 16b microcontroller in 90nm MTJ technology that achieves zero standby power and full performance. The three-terminal magnetic spin SRAM MCU achieves 145μW/MHz with a 1V power supply, and 4.5μW when operating intermittently exhibiting 0.1% duty cycle with 120ns wakeup time.

- In Paper 10.6, Holst Centre/imec describes a multi-standard digital baseband transceiver supporting Bluetooth Smart / ZigBee / IEEE 802.15.6 for 2.5GHz personal networks, with a single RF front-end and consuming 200μW (RX) / 80μW (TX), with adaptive voltage scaling down to 0.74V. The complete digital baseband architecture, including the physical and lower data-link layer processing occupies a silicon footprint of 0.2mm^2 in 40nm.

- In Paper 10.7, the Technical University of Dresden presents a 105GOPS 36mm^2 heterogeneous software-defined radio (SDR) multi-processor SoC for 4G in 65nm CMOS. This SoC achieves a maximum frequency of 446MHz at 1.2V and 69.2mW, using fine-grained power management with ultra-fast DVFS combined with AVS.

- In Paper 10.8, Ericsson presents a 28nm multi-standard 2G/3G/4G cellular modem based on a unified baseband architecture supporting carrier aggregation. Operating at 1.03V, the modem features an LTE Cat4 downlink of 150Mb/s (10MHz+10MHz aggregated) together with an uplink of 25Mb/s.

Session 11 Overview: *Data Converter Techniques*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Jan Mulder, Broadcom, Bunnik, The Netherlands*
Session Co-Chair: *Stéphane Le Tual, STMicroelectronics, Crolles, France*

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA, Data Converters Subcommittee*

Power efficiency and high dynamic range are of crucial importance for contemporary data converters, which are essential in a wide range of demanding applications, such as medical, sensor, and advanced wireless mobile systems. Circuits and architectures tailored to low-voltage deep-submicron CMOS technologies, data-driven conversion and optimized calibration algorithms are presented in this session. These innovative data converter techniques and algorithms are advancing the state of the art in dynamic range and power efficiency.

- In Paper 11.1, Eindhoven University of Technology uses chopping, dithering, oversampling and data-driven noise reduction to obtain a power-efficient SAR ADC that can be configured for 12b or 14b operation. Implemented in 65nm CMOS, the converter achieves an SNDR up to 79.1dB in a 4kHz bandwidth.

- In Paper 11.2, National Taiwan University reaches a record efficiency of 0.85fJ/conversion-step for a 200kS/s 10b ADC in 40nm CMOS. Combining subranging and SAR architectures, the DAC switching energy and comparator power consumption can be reduced significantly, while achieving 55.6dB SNDR.

- In Paper 11.3, Massachusetts Institute of Technology presents a 10b 0.5V SAR ADC in 0.18um CMOS exploiting the characteristics of ECG input signals to save energy. Using an LSB-first algorithm, a power efficiency down to 2.9fJ/conversion-step is achieved for a low-activity input signal.

- In Paper 11.4, Broadcom (with Wolfson Microelectronics) describes a 28nm CMOS pipelined SAR ADC, which features a dynamic residue amplifier with noise-filtering properties. At 80MS/s, the converter achieves an SNDR of 68dB, while consuming only 1.5mW.

- In Paper 11.5, the University of Michigan (with Samsung Electronics) introduces a comparator-less pipeline ADC using a self-biased ring amplifier in 65nm CMOS. It presents 56.3dB SNDR at 100MS/s for 2.46mW power consumption.

- In Paper 11.6, Maxim Integrated (with MIT) uses a dual-ramp zero-crossing-based circuit in a 0.13μm CMOS pipelined ADC to reach 74dB SNDR and 95dB linearity at 48MS/s.

- In Paper 11.7, Integrated Device Technology uses a 3D calibration algorithm to minimize amplitude, delay and duty-cycle mismatches in a 16b 3.2GS/s DAC fabricated in 65nm CMOS. Consuming 240mW, the converter achieves a linearity better than -80dB up to 600MHz.

Session 12 Overview: *Sensors; MEMS, and Displays*

IMMD SUBCOMMITTEE

Session Chair: *Ralf Brederlow, Texas Instruments, Freising, Germany*
Session Co-Chair: *Yoshiharu Nakajima, Japan Display, Ebina, Japan*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

This session presents recent achievements in the area of gesture sensing, capacitive touch displays, time, pressure and temperature sensors. Two advanced gesture-recognition systems are extending the touch experience into the 3rd dimension. These presentations are followed by three papers showing resolution- and size-related improvements in touch-screen display interfaces. An innovative, ultra-low-power capacitive interface circuit for pressure sensors is followed by two presentations on novel temperature-sensing principles pushing barriers of low-voltage operation and energy efficiency. Last but not least, an extremely accurate MEMS-based real-time clock is presented.

- In Paper 12.1, the University of California at Berkeley (with UC Davis) presents an ultrasound-time-of-flight-based 3D gesture-recognition system. The system enables object localization with up to 0.4mm resolution to a distance of up to 0.5m.

- In Paper 12.2, Princeton University demonstrates 30cm out-of-plane sensing for a 40x40cm² gesture-sensing system that relies on the minimization of the effects of stray capacitance.

- In Paper 12.3, Sharp talks about a record-size 70-inch display capacitive touch-sensing system with 224 channels.

- In Paper 12.4 Kobe University (with Panasonic) combines self and mutual capacitance sensing principles to achieve 1mm touch resolution at 322Hz frame rate, thus getting rid of ghosting artifacts.

- In Paper 12.5 KAIST (with Zinitix) shows an extremely small, capacitive touch sensor chip consuming only 2.6mW of power with a total area of 46mm².

- In Paper 12.6 Pohang University (with the University of Michigan) presents a capacitive-to-digital converter using successive-approximation principles using a predictive baseline cancelation scheme to achieve a record figure-of-merit of 63.9fJ per conversion-step.

- In Paper 12.7 TU Delft (with Yonsei University) demonstrates a sub-1V temperature sensor based on dynamic threshold MOSFETs as reference with an accuracy of 0.4°C from a single-temperature trim.

- In Paper 12.8 Smartec BV (with TU Delft, Guilan University, and SenseArt) presents a new temperature sensor principle resulting in 3× better energy efficiency compared to the state of the art.

- In Paper 12.9 SiTime (with Oregon State University, UCLA, and TU Delft) describes a temperature-compensated MEMS oscillator system with a frequency stability of 3ppm for time-keeping applications.

Session 13 Overview: *Advanced Embedded Memory*

MEMORY SUBCOMMITTEE

Session Chair: *Jonathan Chang, TSMC, Taiwan*
Session Co-Chair: *Hugh Mair, MediaTek, Austin, TX*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee*

Embedded memory continues to be a critical technology enabler for a wide range of applications from high-performance computing to mobile applications. This year's conference highlights significant increases in on-chip capacity and bandwidth along with a continued drive towards advanced technology nodes while maintaining a strong focus on low-power operation. A 1Gb embedded DRAM using 22nm tri-gate CMOS logic technology is presented to meet the demands of bandwidth-intense applications. Papers in 14nm FinFET, 16nm FinFET, and 20nm planar technologies demonstrate state-of-the-art read/write assist techniques in order to challenge V_{MIN} limitations. Various aspects of power and performance optimizations are highlighted in the session, including leakage power, dynamic power, latency, and throughput.

- In Paper 13.1, Intel demonstrates a 1Gb 2GHz embedded DRAM using a 22nm tri-gate logic process. A 128Mb macro achieves a density of 17.5Mb/mm^2 using a cell size of 0.029µm^2. 2GHz operation at 1.05V and 1GHz operation at 0.7V are demonstrated.

- In Paper 13.2, Samsung describes the first 14nm FinFET SRAM with the smallest bit-cell size reported to date (0.064µm^2). By using innovative read/write assist schemes, up to a 200mV V_{MIN} improvement for the 0.064µm^2 cell is shown.

- In Paper 13.3, Renesas describes a 20nm high-density single-port/dual-port SRAM with a wordline-voltage-adjustment system for read/write assist. This scheme achieves 100mV V_{MIN} improvement for 64Kb single-port and dual-port SRAMs. A bit density of 8.74Mb/mm^2 is achieved for the SP-SRAM while 3.08Mb/mm^2 is achieved for the DP-SRAM.

- In Paper 13.4, Toshiba has developed a new SRAM bitcell in 65nm CMOS that achieves 27fA/b standby leakage for low power MCU products. Using SRAM over conventional nonvolatile approaches enables fast wake-up from deep sleep. Operating power is reduced though quarter-array activation and hierarchical bitlines.

- In Paper 13.5, TSMC describes the write-assist techniques used for their 0.073µm^2 16nm FinFET SRAM bit cell. Silicon results demonstrating over 300mV improvement in V_{MIN} are shown.

- In Paper 13.6, Renesas describes a large, 80Mb/1Mentry, 1.6Gsearch/s TCAM implemented using four parallel 400MHz units in 28nm. The key design features include flexible search mode, row and column shift redundancy, and search omission with valid-bit.

- In Paper 13.7, University of Michigan describes a variation-tolerant sensing scheme to improve sense margin in advanced technologies. Silicon results in 28nm are presented to show both margin and performance improvement.

- In Paper 13.8, National University of Singapore presents an alternative approach to balancing power and precision. Compared to a conventional approach of reducing bit width, the design uses lower-order bits for ECC-based correction of high-order bits, enabling lower-voltage operation and lower total power.

Session 14 Overview:
Millimeter-Wave and Terahertz Techniques

RF SUBCOMMITTEE

Session Chair: *Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany*
Session Co-Chair: *Brian Floyd, North Carolina State University, Raleigh, NC*

Subcommittee Chair:
Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee

Efficient generation of mm-Wave and THz signals is a critical need for the enablement of radar, communications, and imaging applications. The first four papers in this session present state-of-the-art solutions for mm-Wave power amplifiers and transmitters at 60, 79, and 28GHz. The final four papers in the session present harmonically-generated 0.25-to-0.5THz sources and arrays in advanced silicon.

- In Paper 14.1, KU Leuven presents a 40nm CMOS power amplifier for licensed E-band that employs series-parallel power combining to achieve 17.5dBm output compression point, 20dBm saturated output power, and 20% peak PAE over 71 to 86GHz.

- In Paper 14.2, imec demonstrates a 79GHz phase-modulated CW radar transmitter in 28nm CMOS. The circuit architecture uses digital pseudo-random noise modulation at a 4GHz RF bandwidth for a low-power implementation with 10.4% power efficiency.

- In Paper 14.3, KU Leuven presents a 60GHz push-pull power amplifier in 40nm CMOS suitable for 64-QAM modulation. An inverter-based architecture is used to cancel AM-to-PM conversion and achieve 16.4dBm saturated output power with 23% peak PAE.

- In Paper 14.4, Virginia Tech describes a 28GHz class-F/F^{-1} power amplifier in 0.13µm SiGe BiCMOS that achieves 15dBm output compression point, 17dBm saturated output power, and 40% peak PAE.

- In Paper 14.5, The University of Wuppertal and IHP present a programmable 0.53THz 16-pixel source array with up to 1mW radiated power in 0.13µm SiGe BiCMOS for active-THz imaging applications. Each asynchronously operated triple-push oscillator delivers up to -12dBm with a 25dBm EIRP.

- In Paper 14.6, Cornell University presents a lensless scalable 16-element phased array at 338GHz with 17.1dBm EIRP and 0.8mW radiated power in a 65nm CMOS process.

- In Paper 14.7, The University of California, Irvine and The University of California, Davis describe a 300GHz phase-locked loop with 7.9% locking range using a triple-push VCO with an active varactor in a 90nm SiGe BiCMOS process.

- In Paper 14.8, Cornell University shows a 247-to-263GHz VCO with 1.14% DC-to-RF efficiency and 2.6mW peak output power using coupled Colpitts oscillators in a 65nm CMOS process.

Session 15 Overview: *Digital PLLs*

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Anthony Hill, Texas Instruments, Dallas, TX*
Session Co-Chair: *Hiroo Hayashi, Toshiba, Kawasaki, Japan*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

The four papers presented in this session highlight developments in clock generation and distribution. These papers demonstrate the growing trend toward fully-synthesizable digital PLLs. Solutions presented relate to digital PLL integration, including power-supply noise rejection, temperature compensation, and fast frequency switching required in modern SoCs.

- In Paper 15.1, the Tokyo Institute of Technology presents a 780μW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using an edge-injection technique. This design introduces a current digital-to-analog converter composed of standard CMOS NAND gates, where the PLL is completely assembled using standard-cell components. The PLL consumes 0.0066mm^2 in 65nm CMOS operating at 380MHz to 1.41GHz.

- In Paper 15.2, Samsung Electronics presents a 0.012mm^2 3.1mW bang-bang digital fractional-N PLL with power-supply-noise cancellation and a walking-one-phase-selection fractional frequency divider in 20nm CMOS. This digital PLL offers a solution to power-supply noise and the high energy consumption of a time-to-digital converter (TDC). The noise-cancellation technique shown in this paper suppresses jitter degradation to <10% across a supply-noise frequency of 5kHz to 50MHz and supports a frequency range of 25MHz to 1.6GHz.

- In Paper 15.3, MediaTek presents a 2.4GHz all-digital PLL with a digitally regulated supply-noise-insensitive temperature-self-compensated ring DCO. This 40nm PLL consumes just 6.4mW of power, with an integrated jitter of 3.29ps at 2.418GHz. The supply sensitivity after calibration is 0.0087, with a frequency drift of 2% across temperatures from 20°C to 100°C. This PLL area is 0.013mm^2.

- In Paper 15.4, the University of Illinois at Urbana-Champaign and Intel present a 20MHz-to-1GHz, 14ps peak-to-peak jitter reconfigurable multi-output all-digital clock generator using open-loop fractional dividers in 65nm CMOS. This clock-generation unit occupies an area of 0.12mm^2.

Session 16 Overview: *SoC Building Blocks*

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Kathy Wilcox, AMD, Boxborough, MA*
Session Co-Chair: *Yasuhisa Shimazaki, Renesas Electronics, Tokyo, Japan*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

The four papers in this session highlight developments in system-on-chip (SoC) blocks essential to continue scaling trends. These include fabrics required for high throughput, as well as blocks needed for secure systems and temperature sensors to achieve target power requirements. These designs are demonstrated in recent technologies with low area and low power overhead that enables ease of use in SoC design.

- In Paper 16.1, Intel presents a 256-node network-on-chip (NoC) with 20.2Tb/s throughput. Industry leading energy efficiency of 18.3Tb/s/W at 430mV is achieved through the use of source-synchronous hybrid packet/circuit-switched operation. The 23mm^2 design is implemented in a 22nm tri-gate CMOS process.

- In Paper 16.2, Intel introduces a variation-tolerant physically unclonable function (PUF) circuit that occupies 4.66μm^2/b in 22nm CMOS. The hybrid cross-coupled/delay PUF has a low energy consumption of 0.19pJ/b at 0.9V, and a high operating frequency of 2GHz, while maintaining immunity to probing attacks.

- In Paper 16.3, the University of Michigan presents true-random-number generators (TRNGs) implemented in 28nm and 65nm CMOS, which utilize a 3-edge ring oscillator synthesized entirely with standard cells. The proposed TRNG utilizes the thermal noise in a 3-edge ring oscillator as a source of randomness. It passes all NIST randomness tests, provides 23.16Mb/s throughput at 0.9V and occupies 375μm^2 in 28nm.

- In Paper 16.4, Columbia University presents a temperature sensor, which utilizes 2-transistor voltage reference circuits and achieves an accuracy of +3.2/-3.4°C after 1-point calibration. The proposed differential reading achieves a DC-PSRR better than -67dB by eliminating sensitivity to V_{DD}. The temperature sensor occupies 279μm^2 in 65nm CMOS and consumes 0.92μW at V_{DD}=0.6V.

Session 17 Overview: *Analog Techniques*

ANALOG SUBCOMMITTEE

Session Chair: *Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands*
Session Co-Chair: *Edgar Sanchez-Sinencio, Texas A&M University, College Station, TX*

Subcommittee Chair: *Axel Thomsen, Silicon Labs, Austin, TX, Analog Subcommittee*

Analog technology continues to push the state of the art. This session illustrates the diversity and vitality of modern analog circuitry. Papers in this session span the range of filters, amplifiers, audio, voltage regulators, and oscillators. New frontiers of accuracy, power, and performance are established.

- In Paper 17.1, by University of Twente presents an 80V class-D power amplifier implemented in a 0.14µm SOI BCD process. The amplifier adaptively regulates its switching frequency for optimal power efficiency and achieves best-in-class 93% efficiency at 45W output power, >80% power efficiency down to 4.5W output power and >49% efficiency down to 0.45W output power.

- In Paper 17.2, by University of Macau, a single-stage amplifier with rail-to-rail output swing for LCD column driver ICs in 0.18µm CMOS is presented, that uses a Nested-Current-Mirror technique. The amplifier has 84dB DC gain, and 0.013-to-1.24MHz GBW over 0.15-to-15nF capacitive load with >62° phase margin.

- In Paper 17.3, by KAIST, a 0.9V 6.3µW three-stage amplifier capable of driving 500pF capacitive load is presented. This amplifier, fabricated in a 0.18µm CMOS process, achieves 1.34MHz gain-bandwidth product, 52.7° phase margin and 0.62V/µs average slew rate.

- In Paper 17.4, by Politecnico di Milano, an architecture in 0.35µm CMOS is presented that performs impedance spectroscopy in the frequency range from 1kHz to 150MHz with 180dB loop gain at all frequencies. Two DC outputs directly related to the real and imaginary parts of the input admittance achieve a resolution better than 1pS and 1aF, respectively.

- In Paper 17.5, by NXP Semiconductors, a 2-channel instrumentation amplifier in 0.16µm CMOS is presented with 0.1% gain matching and a 13.3x area improvement with respect to state-of-the-art designs with similar gain accuracy. Dynamic element matching (DEM) and a high chopping frequency yields 18.7nV/√Hz noise, 17µV offset, and 12.9 NEF.

- In Paper 17.6, by ST Microelectronics, a buck-boost Envelope Modulator based on AC-coupled multilevel switching regulators is presented. Power added efficiency when loaded by an RF power amplifier reaches 39% for an output power of 26.3dBm and ACLR <-40dBc. The circuit is manufactured in a 0.13µm, 4.8V CMOS process.

- In Paper 17.7, by MediaTek, an ultra-low power self-charged XO is proposed for 32.768kHz real-time clock generation. A direct-charging scheme with logic-intensive design is proposed to reduce the power and supply voltage. It consumes 1.89nW under 0.15V supply and occupies 0.03mm^2 active area in a 28nm CMOS process.

- In Paper 17.8, by Texas Instruments, a fully integrated 33kHz RC oscillator in 65nm CMOS for sleep timers in wireless sensor networks is presented. The oscillator uses an inverter as comparator and a supply that tracks the inverter parameters. It achieves ±0.21% frequency stability over −20°C to +90°C and better than 4ppm long term frequency stability over intervals above 2s while consuming only 190nW.

- In Paper 17.9, by Columbia University, a 0.6V 70MHz 4th Order Continuous-Time Butterworth filter in 65nm CMOS is presented where the output stages of OTAs are replaced with power-efficient rail-to-rail Class-D stages. The filter achieves 58dB dynamic range, 55.8dB SNR and 60dB THD at +2.8dBm output signal power, while dissipating 26.2mW from a 0.6V supply.

- In Paper 17.10, by National Chiao Tung University, a 0.6V output voltage low-drop regulator with embedded voltage reference in a 28nm CMOS process is proposed for low-power biomedical systems. A 30ppm/°C temperature coefficient and 10mA driving capability is achieved at 0.65V input voltage.

- In Paper 17.11, by HKUST, a fully-integrated tri-loop LDO architecture is proposed and verified in 65nm CMOS for wideband communication systems. It achieves a transient response time of 0.65ns with 50µA quiescent current and 140pF load capacitor. Measured PSR is -15.5dB at 1GHz.

Session 18 Overview:
Biomedical Systems for Improved Quality of Life
TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Yogesh Ramadass, Texas Instruments, Dallas, TX*
Session Co-Chair: *David Ruffieux, CSEM, Neufchatel, Switzerland*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, The Netherlands*
Technology Directions Subcommittee

Advanced biomedical systems-on-chip combined with miniaturized sensors and actuators offer new developments in the field of mobile, low-cost healthcare applications. Implants and lightweight systems that bring a high level of comfort to the patient truly enable early diagnosis, personal point-of-care and therapy outside of a traditional clinical setting. Overall, this brings a higher quality-of-life to the patient while reducing costs.

This session presents recent advances in biomedical devices for point-of-care diagnosis and therapy. It includes SoCs for assisted hearing, SoCs for connected personal health applications and analysis of physiological signals such as mental health monitoring and early breast cancer detection.

- In Paper 18.1 from Phonak Communications, a 1V 2.4GHz wireless digital audio communication SoC for hearing-aid applications is described. With the help of an embedded DC-DC converter using delta-sigma control, the SoC is able to reject noise in the audible frequency band. The SoC consumes 3mA while receiving a 7kHz audio signal in good link situations.

- Paper 18.2 from the Massachusetts Institute of Technology presents a fully-implantable cochlear implant in a 0.18um HVCMOS process that uses a piezoelectric middle ear sensor interface. The SoC consumes 572uW including the stimulator, exploiting a 0.6V reconfigurable sound processor with adaptive channels and a neural stimulator providing energy-optimal waveforms.

- In Paper 18. 3 from imec, a multi-parameter biomedical SoC with integrated AFE and DSP is presented. The AFE has 3 biopotential readout channels consuming 31uW each and 1 bioimpedance readout consuming 58uW. The DSP includes real-time motion artifact reduction with a general-purpose microcontroller and a dedicated hardware accelerator for improved energy efficiency.

- In Paper 18.4 from KAIST, a mobile electrical impedance tomography IC consuming 53.4mW for a personal early breast cancer detection system is presented. The system incorporates 92 electrodes for current stimulation and voltage sensing. The differential sinusoidal current stimulator injects up to 400μA of current, and voltage-sensing amplifier can measure breast tissue impedance with a maximum gain of 60dB thereby achieving a sensitivity of 4.9mΩ.

- In paper 18.5 from KAIST, a mental health management system relying on EEG signal acquisition, data processing and classification is presented. The system implements closed-loop operation via neuro-feedback stimulation. The IC, integrated in a 0.13μm CMOS process, measures 5mm x 2.35mm and consumes 2mW.

- In paper 18.6 from National Chiao Tung University, a 670μW, 2.5D, 10mm x 5mm 16-channel hybrid microsystem is designed for neural sensing applications. It consists of a high-density micro-probe array that is connected via a silicon interposer with TSVs to a signal acquisition and processing/classification chain. The signal processing chain consists of several 180nm and 65nm dies and an MCU.

- In Paper 18.7 from National Taiwan University, a batteryless remotely controlled locomotive IC that uses electrolytic bubbles as the propulsion mechanism is presented. The IC is wirelessly powered and controlled by a 10MHz ASK signal allowing movement in four orthogonal directions with two speed controls. The IC reaches a speed of 0.3mm/s. The circuit and electrolysis actuator consume 125.4uW and 82uW, respectively.

Session 19 Overview: Nonvolatile Memory Solutions

MEMORY SUBCOMMITTEE

Session Chair: *Jin-Man Han, Samsung, Korea*
Session Co-Chair:*Tadaaki Yamauchi, Renesas Electronics, Japan*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee*

Strong market demands of diverse non-volatile memory technologies show continuing increase in density, reliability, and performance. This year the leading edge process node for NAND Flash is scaled down to the minimum feature size of 16nm, and three-dimensional vertical NAND has been demonstrated. In addition, Flash controllers contribute to the higher reliability and performance on such advanced node. Emerging memories such as Resistive RAM (ReRAM) are continuing to show significant performance progress.

- In Paper 19.1, Micron reports 128Gb MLC NAND Flash memory using 16nm planar cell with high-k dielectric/metal gate cell architecture. 400MT/s/pin using a 1.8V DDR interface is enabled by an advanced data path design. New design features are employed to compensate memory cell degradation due to scaling.

- In Paper 19.2, SK Hynix describes a 64Gb MLC NAND Flash memory implemented in 16nm process. It supports 400Mb/s NV-DDR2 interface for high-speed data transaction. The delayed P1 program pulse scheme makes the cell distribution tighter without additional overhead, and the cell current screen scheme both reduces the operation power and enhances the read accuracy.

- In Paper 19.3, Toshiba reports an embedded NAND-storage device controller with unified memory which contributes to 2× and 10× faster random read and write performance, respectively. Low-power dual-lane 5.8Gb/s M-PHY with random read command processor attains performance of 66.3KIOPS random read and 690MB/s.

- In Paper 19.4, National TsingHua U describes an embedded 1Mb ReRAM in 28nm process with 0.27-to-1V read. A swing-sample-and-couple sense amplifier improves read margins/speeds by over 1.8×. A self-boost-write-termination scheme contributes to a reduction of 99% SET energy with below 0.5% area penalty.

- In Paper 19.5, Samsung reports three dimensional 128Gb MLC vertical NAND Flash Memory with 24 WL stacked layers. The chip accomplishes 50MB/s write throughput with 3K endurance for typical embedded applications and extended endurance of 35K with 33MB/s write throughput for data center and enterprise SSD applications.

- In Paper 19.6, Chuo U describes a hybrid storage of ReRAM/TLC NAND Flash with RAID-5/6 for cloud data centers. The bit-error rate of 50nm ReRAM and the failure rate of 2xnm TLC NAND are improved by 69% and 98%, respectively. It is achieved by applying 5 techniques involving adaptive asymmetric coding for ReRAM and bits/cell optimization for TLC NAND.

- In Paper 19.7, Micron reports 16Gb ReRAM with 200MB/s write and 1GB/s read in 27nm process. A 1GB/s DDR interface and an 8-bank concurrent core architecture are employed with high parallelism and pipelined data path architecture.

Session 20 Overview: *Wireless Systems*

WIRELESS SUBCOMMITTEE

Session Chair: *Iason Vassiliou, Broadcom, Greece*
Session Co-Chair: *Myung-Woon Hwang, FCI, Korea*

Subcommittee Chair: *Aarno Pärssinen, Helsinki, Finland, Wireless Subcommittee*

State-of-the-art wireless systems implemented in low-cost, deep-sub-micron CMOS processes support a wide range of applications including mm-Wave ranging, Gb/s communications in 60GHz/5GHz bands and cost-sensitive cellular communications. This session includes one radar receiver paper, three state-of-the-art 60GHz transceivers supporting 2 to 28Gb/s, the first reported fully integrated 802.11a/b/g/n/ac SoC supporting over 1Gb/s and three cellular receivers implementing blocker-tolerant techniques intended to eliminate the need for external filters.

- In Paper 20.1, KU Leuven presents a 40nm CMOS receiver for 60GHz mm-precise localization that uses a combination of multi-tone signals and sub-sampling to reduce the required bandwidth in baseband, thus enabling fast and power-efficient ranging measurements. Multi-burst averaging leads to 4mm precision across 5-meter distances at 50kHz update rate.

- In Paper 20.2, Broadcom presents a highly integrated 60GHz 802.11ad, 16x16 phased-antenna-array transceiver chipset with polarization diversity in 40nm CMOS, including RF/PHY and MAC. It supports up to 64-QAM modulation and throughput of over 3.5Gb/s at 10m. Radio power consumption is 960/1190mW (RX/TX), while a single coaxial cable is used to interface between chips to ease integration to PC platforms.

- In Paper 20.3, Tokyo Institute of Technology presents the first 64-QAM 60GHz CMOS RF transceiver that achieves a TX-to-RX EVM of -26.3dB, enabling 10.56Gb/s in regular 802.11ad mode and 28.16Gb/s 4-channel bonding mode using 16QAM. The transceiver is implemented in 65nm CMOS and consumes 251mW and 220mW from a 1.2V supply in transmit and receive mode respectively.

- In Paper 20.4, Toshiba presents the first fully-integrated single-chip 60GHz CMOS transceiver for proximity systems including RF, PHY and MAC, achieving MAC throughput of 2.0Gb/s at 4cm distance. Digital noise-suppression techniques and broadband noise-tolerant RF/analog blocks reduce noise from digital blocks to less than -35dBc. Total power consumption of the TX/RX chip, implemented in 65nm CMOS, is 1268mW, which is scaled to 36% when operating at 0.2Gb/s.

- In Paper 20.5, Marvell presents the first reported dual-band 3-stream 802.11a/b/g/n/ac MIMO WLAN SoC in 40nm CMOS. By employing an all-digital fractional-N PLL with an FoM of -244dB, and a wideband low-impedance bias circuit that minimizes pre-PA driver memory effect, it achieves an EVM floor of -37dB and an over-the-air TCP/IP throughput of 1Gb/s at 5775MHz in 802.11ac MCS9 80MHz mode.

- In Paper 20.6, Columbia University presents a blocker-resilient software-defined receiver in 65nm CMOS with a low-noise active TX leakage cancellation scheme that can cancel up to +2dBm peak TX leakage at the RX input, enabling an effective IIP3 of +30dBm (enhancement of 18dB) with an associated increase in NF of <0.5dB.

- In Paper 20.7, MediaTek presents the most compact inductor-less, SAW-less TDD cellular six-band receiver for GSM/EDGE/TDSCDMA. It is implemented in 40nm CMOS, occupies 0.57mm^2 and achieves a 1.7dB NF while consuming 26mA.

- In Paper 20.8 UCLA presents a wideband receiver by employing N-path filters around the LNA in 65nm CMOS. The receiver provides an attenuation of 15dB in the middle of the alternate adjacent channel and a noise figure of 5.4dB with a 0dBm blocker at 23MHz offset.

Session 21 Overview: *Frequency Generation Techniques*

RF SUBCOMMITTEE

Session Chair: *Piet Wambacq, imec, Belgium*
Session Co-Chair: *Chih-Ming Hung, MStar Semiconductor, Taiwan*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, France, RF Subcommittee*

VCOs and PLLs are at the heart of communication systems. They are critical for almost all RF applications such as receivers, transmitters, imagers, and radars. This session starts with three highly digitized frequency synthesizers, including multiplying DLL/PLLs with fractional-N operation and a direct-digital frequency synthesizer. The fourth paper shows a mm-Wave PLL based on a subsampling technique. Interference-tolerant VCOs and PLLs are presented next, followed by a multichannel receiver whose LO frequencies are generated from a single stable FBAR oscillator without a PLL.

- In Paper 21.1, Politecnico di Milano presents the first MDLL-based frequency synthesizer in 65nm CMOS with fine fractional-N resolution of 190Hz, low power consumption of 3mW and low integrated rms jitter of 1.4ps.

- In Paper 21.2, National Taiwan University presents an analog "divider-less" fractional-N PLL in 0.18μm CMOS, which modulates the edge of the reference clock. The design achieves a low in-band noise of -112dBc/Hz at 2.3GHz and 266fs rms jitter.

- In Paper 21.3, the Chung-Ang University, Analog Devices and KAIST present the first CMOS-based direct-digital frequency synthesizer that operates at 2GHz with a high spectral purity up to 70.3dBc SFDR. Power consumption is only 130mW and the chip area is 0.1mm^2 in 55nm CMOS.

- In Paper 21.4, imec and Vrije Universiteit Brussel present the first mm-Wave PLL utilizing a subsampling phase detector instead of a classical divider chain. Implemented in 40nm CMOS, the PLL has a jitter as low as 230fs for a power consumption of 42mW.

- In Paper 21.5, Stanford University presents a 3.24GHz-to-8.45GHz VCO in 40nm CMOS. The large tuning range is obtained via mode switching while preserving excellent phase noise, meeting the requirements for cellular applications.

- In Paper 21.6 Lund University and Ericsson describe a dual-core VCO in 65nm CMOS. It uses two figure-8-shaped concentric coils to save area and simultaneously achieve an extremely large tuning range of 75% with a supply voltage of only 0.4V.

- In Paper 21.7, the University of Washington and Avago Technologies present a 2.4GHz ZigBee receiver that uses an oscillator based on a temperature-compensated thin-film bulk acoustic-wave resonator, thereby eliminating the need of a PLL. Using a 65nm CMOS technology, power consumption of the sliding-IF receiver architecture with careful LO frequency planning is only 1.8mW.

- In Paper 21.8 Broadcom presents a calibration technique that mitigates unwanted pulling effects in a direct-conversion transmitter. When the TX VCO is heavily pulled, the technique lowers the EVM from 11% to 2.4%. It also suppresses the unwanted sidebands caused by pulling from another nearby oscillator by more than 20dB.

Session 22 Overview: *High-Speed Data Converters*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Jieh-Tsorng Wu, National Chiao-Tung University, Hsinchu, Taiwan*
Session Co-Chair: *Seung-Tak Ryu, KAIST, Daejeon, South Korea*

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA, Data Converters Subcommittee*

This session demonstrates design techniques to realize data converters with unprecedented combinations of speed, resolution, and power efficiency in advanced CMOS technologies. Papers in this session include a time-interleaved ADC with a sampling rate up to 90GS/s, a time-interleaved DAC at 4.6GS/s conversion rate, and a time-based 2.2GS/s ADC. These converters are essential for systems enhanced by digital signal processing, such as optical communications, wireline communications, broadband satellite receivers, and cable systems.

- In Paper 22.1, IBM (with EPFL) presents a 90GS/s 8b time-interleaved ADC in 32nm SOI CMOS. It contains 64 SAR ADC channels. It achieves above 33dB SNDR up to 19.9GHz input frequency and consumes 667mW from a 1.2V supply.

- In Paper 22.2, Carnegie Mellon University presents a 20GS/s 6b time-interleaved ADC in 32nm SOI CMOS. It contains 8 flash ADC channels and features on-chip calibration to reduce inter-channel mismatches in the background. It achieves 30.7dB SNDR up to Nyquist and consumes 69.5mW from a 0.9V supply.

- In Paper 22.3, STMicroelectronics presents a 10GS/s 6b time-interleaved ADC in 28nm fully depleted SOI CMOS. It contains 8 SAR ADC channels. It uses a master T/H that enables 20GHz input sampling without the need for timing skew calibration. It achieves 4.6 ENOB at 20GHz input and consumes 32mW from a 1V supply.

- In Paper 22.4, MIT presents a 1GS/s 10b time-interleaved ADC in 65 nm CMOS. It contains 8 SAR ADC channels. It features a full-rate 4b flash ADC for sub-ranging and timing skew calibration. It achieves 51.4dB SNDR at Nyquist and consumes 18.9mW from a 1V supply.

- In Paper 22.5, STMicroelectronics (with Supélec) presents a 1.62GS/s 9b time-Interleaved ADC in 40nm CMOS. It contains 12 SAR ADC channels. It uses a digital calibration unit to estimate and correct inter-channel mismatches in the converter backend. It achieves 48dB SNDR and demonstrates interleaving spurs below -70dBFS up to 750MHz input frequency, while consuming a total power of 93mW.

- In Paper 22.6, the Tokyo Institute of Technology presents a 2.2GS/s 7b time-based folding ADC in 40nm CMOS. With no need for calibration, it achieves 37.4dB SNDR at Nyquist. It consumes 27.4mW from a 1.1V supply.

- In Paper 22.7, Maxim Integrated presents a 4.6GS/s 14b time-interleaved DAC in 0.18μm CMOS. It contains two current-steering DAC channels. It provides 80mA of output current and achieves -79dBc IMD with a 500MHz output without trimming or calibration. It consumes a total power of 2.3W.

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Session 23 Overview: *Energy Harvesting*

ANALOG SUBCOMMITTEE

Session Chair: *Makoto Nagata, Kobe University, Kobe, Japan*
Session Co-Chair: *Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX, Analog Subcommittee*

For powering devices from ambient energy sources, innovative CMOS circuit techniques are devised to facilitate highly efficient energy harvesting. Depending on the applications, the loads can range widely from nW to mW and the required output voltages vary from sub-1V to tens of volts. The energy sources can be electrochemical gradient inside an ear, thermoelectric generators, piezoelectric transducers, fuel cells, solar cells, and others. This session starts with three papers presenting novel ultra low power circuits for charge pumping, DC-to-DC conversion and power management, followed by five papers on enabling techniques for dual source power management, energy pile-up resonance, maximum power point tracking and high-voltage charge pumps.

- In Paper 23.1, Korea University and HKUST present an energy harvesting charge pump with switching body biasing and adaptive dead-time schemes for efficiency improvement. The charge pump achieves 240% improvement of maximum output current over conventional architecture and enables the operation at input voltage down to 0.15 V.

- In Paper 23.2, MIT introduces a power management circuit that harvests energy from the endocochlear potential. The entire harvesting circuit consumes only 544pW with an efficiency of 56%.

- In Paper 23.3, University of Michigan presents a fully-integrated energy harvester, which consumes only 3nW and operates in an adaptive manner to loads ranging from 5nW to 5μW.

- In Paper 23.4, Georgia Institute of Technology reports a dual-source single-inductor CMOS charger-supply. It achieves 62 to 83% power conversion efficiency over 0.1 to8mA load current. This converter requires 65% less volume than the prior smallest design.

- In Paper 23.5, KAIST presents an energy extracting scheme based on an energy pile-up technique which builds the internal voltage swing of the piezoelectric transducer up to 5.3 times of the original swing. The piezoelectric harvesting circuit achieves a peak efficiency of 74.9%.

- In Paper 23.6, University of Texas at Dallas presents a 43V 400mW-to-21W photovoltaic energy harvester with 94% power efficiency. With a global-search-based maximum-power-point tracking technique, the harvester tracks global maximum-power-point under partial shading conditions in 350μs transient time.

- In Paper 23.7, Korea University demonstrates a self-powered 30μW-to-10mW piezoelectric energy harvesting system with a maximum power conversion efficiency of 80%. This system realizes the fastest maximum-power-point tracking time of 9.09ms/V, over 9 times faster than the state-of-the-art.

- In Paper 23.8, UCLA introduces a high-voltage charge pump producing 34V with 2.5V tolerant transistors in a 65nm bulk CMOS technology.

Session 24 Overview: *Integrated Biomedical Systems*

IMMD SUBCOMMITTEE

Session Chair: *Maysam Ghovanloo, Georgia Institute of Technology, Atlanta, GA*
Session Co-Chair: *Wentai Liu, University of California, Los Angeles, CA*

Subcommittee Chair: *Roland Thewes, TU Berlin, Germany, IMMD Subcommittee*

This session presents state-of-the-art integrated biomedical systems for high-density neural recording, efficient neuromodulation, ultra-low-power cardiac monitoring, artificial noses, cell type detection, and 3D ultrasound imaging. The first paper focuses on a miniaturized, wirelessly powered, neural interface for acquisition of ECoG signals. The second paper presents a switched-capacitor-based wireless deep-brain stimulator that also supports optogenetic stimulation. The next two papers focus on ECG monitoring using ultra-low-power circuit-design techniques. The fifth paper describes an artificial nose-on-a-chip that can detect early-stage pneumonia. The next paper is about a flow cytometer-on-a-chip using magnetic bead labels. The seventh paper describes an interface chip for EEG recording with active dry electrodes. Finally, a 64-channel interface chip is presented for beamforming in 2D capacitive micromachined ultrasound transducers (CMUT).

- In Paper 24.1, the University of Melbourne (with UC Berkeley) presents a 225 μW 64-channel implantable microsystem for recording of ECoG signals with wireless power delivery. It includes a microfabricated unit comprised of a planar electrode array, an antenna, and a 65nm CMOS IC.

- In Paper 24.2, Georgia Institute of Technology (with Michigan State University) presents a power-efficient wireless switched-capacitor stimulating (SCS) system for electrical/optical deep-brain stimulation. The SCS system improves the stimulator efficiency, reaching a peak of 80.4%, by generating charge-controlled decaying-exponential stimulus pulses.

- In Paper 24.3, the University of Michigan presents an ECG-monitoring SoC suitable for arrhythmia diagnosis that can be injected using a syringe. The 65nm test chip consumes 64nW while continuously capturing abnormal cardiac events, achieving 100× lower power than prior work.

- In Paper 24.4, imec (with TU Eindhoven, Olympus, and KU Leuven) presents a fully integrated implantable ECG-acquisition IC. It integrates a low-power wide-dynamic-range analog signal processor that extracts QRS features in the analog domain, while consuming 680nA.

- In Paper 24.5, National Tsing Hua University (with Taipei Medical University and National Chiao Tung University) presents a nose-on-a-chip for ventilators to monitor and detect pneumonia in early stage. The chip is fabricated in 90nm CMOS, consumes 1.27mW at 0.5V, and provides a promising solution for rapid diagnostics of ventilator-associated pneumonia.

- In Paper 24.6, UC Berkeley presents a flow cytometer on a chip embedded into a single-use microfluidic cartridge. The chip is implemented in 0.18μm CMOS, operates at 1.2GHz, and detects cell types using superparamagnetic micro-bead labels.

- In Paper 24.7, Holst Center/imec (with TU Delft and KU Leuven) presents a digital active electrode for biopotential signal acquisition with dry electrodes. The 0.18μm CMOS ASIC achieves 60nV/√Hz input-referred noise, and ±350mV electrode offset rejection.

- In Paper 24.8, POSTECH (with Samsung Advanced Institute of Technology) presents an analog-digital-hybrid architecture for a single-chip 64-channel ultrasound beamformer to be used with a 2D CMUT array. The 0.13μm CMOS chip achieves a delay resolution of 6.25ns and maximum delay range of 8μs.

Session 25 Overview:
High-Bandwidth Low-Power DRAM and I/O

MEMORY SUBCOMMITTEE

Session Chair: *Uksong Kang, Samsung Electronics, Hwasung, Korea*
Session Co-Chair: *James Sung, Etron, Hsinchu, Taiwan*

Subcommittee Chair: *Kevin Zhang, Intel, OR, Memory Subcommittee*

Requirements for high bandwidth and low power continue to increase in servers and consumer electronics. There are significant challenges in DRAMs to meet all such needs in various applications. In ISSCC 2014, the first LPDDR4 DRAM for mobile applications is demonstrated which has an integrated ECC engine for low-power operation. Next, the first High-Bandwidth Memory (HBM) with 4 TSV stacked layers achieving 128GB/s bandwidth is disclosed. Also, new circuits to reduce standby and I/O power in GDDR5M are shown. The papers in this session present the latest technologies and circuit techniques to improve the performance and power in DRAMs.

- In Paper 25.1, Samsung demonstrates LPDDR4 SDRAM for the first time. It has 8Gb density and is implemented in 25nm DRAM process technology. It achieves a data rate of 3.2Gb/s/pin at 1.0V supply voltage and has an integrated ECC engine for sub-1V operation.

- In Paper 25.2, SK Hynix discloses High-Bandwidth Memory (HBM) for the first time. It is implemented in 29nm DRAM process technology. It consists of 4 TSV stacked layers with total density of 8Gb. It shows high bandwidth of 128GB/s at 1.2V supply voltage with 8 channels and total number 1024 I/Os.

- In Paper 25.3, SK Hynix presents a 1.35V 5Gb/s/pin GDDR5M using 29nm DRAM process technology. It achieves low standby power of only 5.4mW using WCK auto-sync mode. Additional circuit techniques including clock timing skewing and error-adaptive duty-cycle corrector are applied to improve signal integrity.

Session 26 Overview:
Energy Efficient Dense Interconnects

WIRELINE SUBCOMMITTEE

Session Chair: *SeongHwan Cho, KAIST, Korea*
Session Co-Chair: *Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, Wireline Subcommittee*

With the need for increased I/O bandwidth to support ever-increasing communication demands, the development of energy-efficient links that enable high-density interfaces is essential. This session presents 6 papers that introduce new high-speed aggregated serial-link techniques in advanced CMOS technologies. These designs address the demands of a range of key applications, from dense chip-to-chip communications to high-bandwidth memory access.

- In Paper 26.1, nVidia describes a 320Gb/s parallel transceiver in 28nm CMOS using a single-tap reconfigurable FFE transmitter and a receiver with a single-stage continuous-time linear equalizer and a 2-tap DFE. Achieved link power efficiency is 6.5pJ/b.

- In Paper 26.2, Intel introduces a scalable bi-directional serial transceiver at 32Gb/s/lane, with 3-tap FFE transmitter, a CTLE equalizer, and 6-tap DFE. The transceiver, implemented in a 22nm CMOS technology, has per-lane efficiency of 6.3pJ/b at 32Gb/s, while equalizing 17dB of channel loss at Nyquist.

- In Paper 26.3, Kandou Bus presents a new coded signaling scheme that doubles pin efficiency, and is demonstrated in a design supporting 96Gb/s data transmission over an 8-wire bus at 4.3pJ/b/wire over 15dB loss channels. The circuit is implemented in 40nm CMOS.

- In Paper 26.4, Intel shows a 25Gb/s DDR4-to-GDDR5 differential transmitter in a 22nm CMOS process. The configurable transmitter features pre-emphasis control, a high-frequency current-controlled SST driver with equalization, and an all-active DDR driver that minimizes power cost and area overhead of reconfiguration. Over a 24dB-loss channel, the bidirectional transceiver dissipates 4.8pJ/b.

- In Paper 26.5 from Texas A&M, Oregon State University, and Fudan University, a scalable quarter-rate transmitter is presented. This transmitter uses an analog-controlled impedance-modulated 2-tap equalizer and achieves 8-to-16Gb/s operation at 1pJ/b, supporting up to 12dB of equalization. The low-swing global clock distribution enables improved energy efficiency through aggressive voltage scaling, operating with V_{DD} from 0.75 to 1V. The circuit is implemented in a 65nm CMOS process.

- In Paper 26.6, MediaTek introduces a new DDR3 memory interface with asymmetric ODT to save I/O power dissipation on the controller side. It operates at data-rates to 2.667Gb/s/pin on a wire-bond BGA package and single-side mounted PCB.

Session 27 Overview: *Energy-Efficient Digital Circuits*

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: *Bing Sheu, TSMC, Hsinchu, Taiwan*
Session Co-Chair: *Marian Verhelst, KU Leuven, Belgium*

Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO, Energy-Efficient Digital Subcommittee*

Next-generation computing devices for mobile applications require energy efficiency, while achieving increased system performance and programmability. This is enabled through ultra-low-voltage operation, application kernel hardware acceleration, and embedded reconfigurable logic. The papers in this session present several advanced implementation techniques to take these trends to the next level and bring them to the market. Examples include back-biasing techniques, variation-resilient near-threshold operation, charge-recovery schemes, and multi-granularity reconfigurable logic. These techniques are demonstrated in real-world applications such as a DSP processor, low-density parity check (LDPC) decoders, a speech-recognition processor, an FFT core, and a JPEG encoder.

- In Paper 27.1, STMicroelectronics and CEA-LETI - MINATEC describe a 32b VLIW DSP fabricated in 28nm UTBB FDSOI technology capable of dynamically tracking the maximum frequency within 3.5% accuracy. The 1mm^2 chip achieves scalable performance and high energy efficiency in the 397mV-to-1.3V supply range, showing an operating frequency of 460MHz at the minimum 0.4V supply, and a minimum energy per operation of 62pJ at 0.46V.

- In Paper 27.2, MIT presents a speech-recognition chip targeted at real-time decoding for medium vocabulary (5,000 word) continuous speech tasks. The 6.25mm^2 chip excels in memory usage efficiency, is implemented in 65nm CMOS, and consumes 6mW of core power during real-time decoding with a 13.0% word error rate.

- In Paper 27.3, KU Leuven describes the design of a near-threshold full JPEG encoder in a 40nm CMOS technology. The variation-resilient chip is functional down to a supply voltage of 210mV at a 5MHz clock frequency, and consumes 29pJ/pixel at the minimum-energy point, which occurs at 41MHz.

- In Paper 27.4, MIT presents a 0.6mm^2 VLSI implementation of a 746,496-point FFT for up to 0.1% frequency-sparse signals in a 45nm SOI process, consuming 298-1206nJ of energy at a throughput of 36-109GS/s, utilizing scaled supply voltage of 0.66-1.18V, achieving an 88× reduction in run-time compared to a C++ implementation on an i7 CPU.

- In Paper 27.5, UCLA and Qualcomm describe a multi-granularity FPGA capable of efficiently mapping mobile-computing algorithms. The 20mm^2 core in 40nm CMOS, incorporates traditional configurable logic blocks, 2 coarse-grain kernels and an efficient, mixed-radix hierarchical interconnect, achieving a 4× interconnect area reduction and 10-50% lower active power over commercial FPGAs. Using the coarse-grain kernels, the chip's energy efficiency is within 4-5× of ASIC designs.

- In Paper 27.6, the University of Michigan presents a 65nm 576b LDPC decoder, using charge-recovery logic demonstrating a 1.7× gain in energy efficiency, drastically increasing the scale at which charge recovery logic has been applied, with a die area of 1.5mm^2. The lowest energy of 7.3pJ/b/iteration is achieved at a 7.9Gb/s throughput, when self-oscillating at 821MHz, recovering 51.4% of the supplied energy.

- In Paper 27.7, UC Berkeley, STMicroelectronics and EPFL describe a 4mm^2 LDPC decoder chip that supports all codes and throughputs of the IEEE 802.11ad standard for Gb/s wireless LANs. The use of 28nm UTBB FDSOI with back bias allows for aggressive frequency and voltage scaling. Algorithmic-architectural co-optimization enables throughputs of 1.5, 3 and 6Gb/s, consuming 6, 14 and 38mW, respectively.

- In Paper 27.8, the University of Michigan presents a static single-phase contention-free flip-flop (S2CFF) in 45nm SOI, targeting wide-range voltage scalable designs (0.4-1V). The static contention-free flip-flop offers single-phase clock operation with the same device count as a conventional transmission-gate flip-flop (TGFF). Measured active energy, clock power and leakage power are reduced by 32%, 41%, and 35%, respectively, compared to the TGFF.

Session 28 Overview:
Mixed-Signal Techniques for Wireless

WIRELESS SUBCOMMITTEE

Session Chair: *Shouhei Kousai, Toshiba, Kawasaki, Japan*
Session Co-Chair: *Jan van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands*

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Helsinki, Finland, Wireless Subcommittee*

Mixed-signal circuit techniques are essential for high-performance and energy-efficient wireless systems. This session covers circuit techniques of $\Delta\Sigma$-modulators and digital-to-time converters, as well as their application to software-defined radios, frequency synthesizers, and radar systems.

- In Paper 28.1, Aalto University and Ericsson present a software-defined radio receiver that investigates the possibility of using $\Delta\Sigma$-modulators for direct RF-to-digital conversion. The wideband $\Delta\Sigma$-modulator-based receiver using 40nm CMOS is capable of handling up to 20MHz signal bandwidth with a narrowband NF of 4.2dB.

- In Paper 28.2, MediaTek describes a fractional-N frequency synthesizer for 802.11ac applications using 40nm CMOS. The presented circuit has an area of only 0.29mm^2 while fulfilling the stringent noise requirement of 802.11ac at a power consumption not exceeding 17.5mW. The fractional spurs are suppressed by minimizing charge-pump switching noise.

- In Paper 28.3, National Tsing Hua University presents a digital-to-time converter for an impulse radar system using 65nm CMOS. The proposed converter is robust to process, temperature and voltage variations, and can measure time-of-arrival ranges up to 10nsec with a 6ps resolution, which corresponds to 15m distance with 0.9mm accuracy.

Session 29 Overview:
Data Converters for Wireless Systems

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Gerhard Mitteregger, Intel Mobile Communication Group, Munich, Germany*
Session Co-Chair: *Brian Brandt, Maxim Integrated, MA*

Subcommittee Chair: *Boris Murmann, Stanford University, CA, Data Converters Subcommittee*

Analog-to-digital converters for wireless systems continue to improve in noise and distortion performance, sample rate, and integration. This steady advance allows them to move closer to the antenna and digitize an increasing number of communication channels. Two of the ADCs in this session employ continuous-time delta-sigma modulators while one uses a pipelined architecture. The first paper addresses the challenges posed by large out-of-band blocker signals. The second paper tackles the high dynamic range and low noise floor requirements inherent to modern communication channels. The final paper employs new background calibration techniques, including one that compensates for nonlinear kickback resulting from the input sampler. The impressive performance advancements in these works confirm the effectiveness of the design techniques.

- In paper 29.1, IIT Madras presents a 5mW CT $\Delta\Sigma$ ADC with an embedded 2nd-order active filter and VGA achieving 82dB DR over a 2MHz bandwidth. With the embedded Butterworth filter, the out-of-band IIP3 and IIP2 improve by 10dB and 15dB, respectively, compared to a system with the filter placed in front of the ADC. The combined system, VGA, Filter and CT $\Delta\Sigma$ ADC, achieves a DR of 92dB in 130nm CMOS.

- In paper 29.2, Analog Devices (with the University of Toronto) describes a $\Delta\Sigma$ 0-3 MASH ADC achieving -167dBFS/Hz noise spectral density with 53MHz bandwidth. The converter samples at 3.2GHz and achieves a DR of 88-90dB in a bandwidth of 53.3 to 45.7MHz. A novel 0-3 MASH ADC is used, which contains a 16-step flash ADC front-end, and a 3rd-order feed-forward continuous-time $\Delta\Sigma$ modulator back-end. The ADC is designed in 28nm CMOS and draws a total power of 235mW from 0.9/1.8/-1V supplies.

- In paper 29.3, Analog Devices shows a 14b 1GS/s RF sampling pipelined ADC that relies on background calibration to correct for inter-stage gain, settling and memory errors. To improve the sampling linearity, it employs input distortion cancellation and digital calibration to compensate for the nonlinear charge injection from the sampling capacitors. The ADC is fabricated in 65nm CMOS and has an integrated input buffer. With a 140MHz and 2V_{pp} input signal, the converter maintains SNDR and SFDR of 69dB and 86dB, respectively while dissipating 1.2W.

Session 30 Overview:
Technologies for Next-Generation Systems
TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Fu Lung Hsueh, TSMC, Hsinchu, Taiwan*
Session Co-Chair: *Jan Genoe, imec, Leuven, Belgium*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

New materials and technologies are enabling next generation systems and applications. The first four papers in this session combine different semiconductor materials (organic and/or oxide) on flexible foils to realize a variety of applications such as a microprocessor, a display, a sensor and an RFID tag. Papers 5, 8 and 9 combine in a hybrid manner crystalline high-bandgap semiconductors on top of the back-end-of-line (BEOL) of silicon. In papers 6 and 7 dedicated communication systems are implemented in automobiles and over the human body. Finally, paper 10 implements a learning machine mimicking the activity in the human brain.

- In Paper 30.1, imec, KULeuven, TNO, Panasonic and Evonik show a flexible 8b microprocessor on foil comprising solution-processed n-type oxide transistors and organic p-type transistors combined in a CMOS technology. The microprocessor instruction sequence is implemented by inkjet printing silver paste drops on the foil. The processor operates from 6.5V supply and has a maximum clock speed of 2.1kHz.

- In Paper 30.2, imec, TNO and Panasonic show new AMOLED scan drivers integrated with an a-IGZO backplane on flexible foil. The system enables PWM driving of the OLED pixels with a duty cycle of almost 100%. This PWM driving method enables up to 40% static power reduction of AMOLED displays.

- In Paper 30.3, University of Tokyo discloses a wireless and flexible wet sensor sheet with organic transistors for urination detection in diapers. An ESD protection circuit with organic Schottky diodes using CuPc achieves 2kV ESD tolerance, which is indispensable for biomedical applications.

- In Paper 30.4, the University of Catania, STMicroelectronics, University of Eindhoven and CEA-Liten show a 13.56 MHz RFID tag on foil using a complementary organic CMOS process. The tag can recognize ASK PWM signals up to 75bps with 25% modulation depth.

- In Paper 30.5, Panasonic presents a three-phase AC-AC matrix converter realized by GaN/Si integrated chips. The extremely compact solution (19mm by 14 mm) can switch up to 10A under 600V.

- In Paper 30.6, Keio University shows an electromagnetic clip connector that enables an in-vehicle LAN to reduce wire harness weight by 30%. Signaling schemes are implemented to improve noise immunity and satisfy EMC standards at 1.4GHz.

- In Paper 30.7, the Institute of Microelectronics Singapore discloses a wideband Body Channel Communication (BCC) transceiver achieving 60 Mb/s data rate. The transceiver operates with high energy efficiency (31pJ/b Tx and 150 pJ/b Rx).

- In Paper 30.8, University of California, Qualcomm and HRL Laboratories demonstrate a compensated track-and hold (THA) in InP BiCMOS technology providing low non-linear distortion at 30 GS/s sampling rate.

- In Paper 30.9, the Semiconductor Energy Laboratory elaborates a normally-off computing FPGA by implementing a 1um c-axis aligned crystal (CAAC) IGZO FET technology on top of a 0.5um CMOS wafer. Load and store times in the nonvolatile registers in the BEOL are 8ns and 40ns, respectively.

- In Paper 30.10, the University of Tennessee presents an analog feature extraction engine with a deep machine learning algorithm. It is implemented in a 0.13um CMOS technology and achieves 1 TOPS/s peak efficiency at 3V supply.

ISSCC 2014
SESSION HIGHLIGHTS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2014 in February in San Francisco

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- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 61st appearance of ISSCC, on February 9th to the 13th, 2014, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2014, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 9-13, 2014, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 1, 2013, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

Session 2 Highlights: Wireline

[2.1] 28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28nm CMOS

[2.3] 60Gb/s NRZ and PAM4 Transmitters for 400GbE in 65nm CMOS

Paper 2.1 Authors: *Hiroshi Kimura, Pervez Aziz, Tai Jing, Ashutosh Sinha, Ram Narayan, Hairong Gao, Ping Jing, Shiva Kotagiri, Amaresh Malipatil, Gary Hom, Anshi Liang, Aniket Kadkol, Eric Zhang, Gordon Chan, Ruchi Kothari, Kathy Ling, Yehui Sun, Benjamin Ge, Jason Zeng, Michael Wang, Chris Abel, Freeman Zhong*
Paper 2.1 Affiliation: *LSI, San Jose, CA*

Paper 2.3 Authors: *Ping-Chuan Chiang[1,2], Hao-Wei Hung[1], Hsiang-Yun Chu[1], Guan-Sing Chen[1], Jri Lee[1,2]*
Paper 2.3 Affiliation: *[1]National Taiwan University, Taipei, Taiwan, [2]Atilia Technology, Taipei, Taiwan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- In a previous ISSCC, a 28Gb/s transceiver over 29dB channel consuming 700mW in 32nm CMOS was reported. This year, a longer reach and lower power 28Gb/s transceiver in 28nm CMOS is reported.

- Last year, ISSCC reported a 60+Gb/s RX DFE in 65nm CMOS. This year, a transmitter has reached 60Gb/s, also in 65nm CMOS.

TECHNICAL HIGHLIGHTS

- **Lowest-power CMOS 28Gb/s transceivers over high-loss channels**
- In Paper 2.1, LSI Logic describes a multi-standard 28Gb/s transceiver implemented in 28nm CMOS and consuming 560mW per channel for CEI-25G, CEI-28G, IEEE802.3bj, and 32G-FC applications over long-reach channels. The design's AFE provides 15dB of boost, while the DFE uses a half-rate 1-tap unrolled architecture. Over a 34dB test channel, the horizontal eye margin is 0.49UI and the vertical margin is 99mV.

- **First fully integrated 60Gb/s transmitter in CMOS**
- In Paper 2.3, National Taiwan University introduces fully-integrated 60Gb/s NRZ and PAM4 transmitters in 65nm CMOS for 400GbE applications. The NRZ transmitter consumes 450mW of power and the PAM4 TX consumes 290mW, both from a 1.2V supply.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of complete transceivers and energy-efficient equalizers operating at 28+Gb/s over long-reach channels highlights the potential for the continued viability of high-speed electrical interconnects.
- A next generation 60Gb/s CMOS transmitter enables 400GbE and beyond applications

Session 3 Highlights: RF Techniques

[3.2] A 1.95GHz Fully Integrated Envelope Elimination and Restoration CMOS Power Amplifier with Envelope / Phase Generator and Timing Aligner for WCDMA and LTE

Paper 3.2 Authors: *K. Oishi, E. Yoshida, Y. Sakai, H. Takauchi, Y. Kawano, N. Shirai, H. Kano, M. Kudo, T. Murakami, T. Tamura, S. Kawai, S. Yamaura, K. Suto, H. Yamazaki, T. Mori*
Paper 3.2 Affiliation: *Fujitsu Laboratories, Kawasaki, Japan*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Corelles, France, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- In recent years, the demand for low-cost and low-power system-on-a-chip (SoC) solutions for mobile terminals has led to the development of highly integrated, low-distortion, and power-efficient CMOS power amplifiers (PAs).

- PAs incorporating envelope tracking (ET) or envelope elimination and restoration (EER) techniques published in the past in general require additional off-chip components in order to satisfy power efficiency, gain and output power requirements of LTE systems.

TECHNICAL HIGHLIGHTS

- **World's first fully integrated envelope elimination and restoration (EER) CMOS PA for WCDMA and LTE terminals.**

- Paper 3.2 by Fujitsu Laboratories presents a fully integrated EER CMOS PA for WCDMA and LTE. Power efficiencies of 34.1% and 32.2% were achieved for LTE10MHz and LTE20MHz respectively.

APPLICATIONS AND ECONOMIC IMPACT

- This fully integrated CMOS PA will enable system-on-a-chip (SoC) integration of a complete LTE transceiver, which will further reduce the size, cost, and complexity of mobile devices.

- More efficient PAs will reduce overall system power dissipation, which will in turn extend battery life.

Session 4 Highlights: DC-DC Converters

[4.6] An 85%-Efficiency Fully Integrated 15-Ratio Recursive Switched-Capacitor DC-DC Converter With 0.1-to-2.2V Output Voltage Range

Paper Authors: *Loai G. Salem and Patrick P. Mercier*
Paper Affiliation: *University of California San Diego, La Jolla, CA*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- The growing demand for both performance and battery life in portable consumer electronics requires SoCs and power management circuits to be small, efficient, and dynamically powerful. Dynamic voltage scaling can help achieve these goals in load circuits, though generally at the expense of increased DC-DC converter size or loss.

- While switched-capacitor DC-DC converters can offer conversion in small, fully-integrated form-factors, their efficiencies are only high at discrete ratios between the input and output voltages.

TECHNICAL HIGHLIGHTS

- **Novel switched capacitor DC-DC converter topology with high efficiency across a wide output voltage range:**

- Paper 4.6 describes the design of a SC DC-DC converter, fabricated in 0.25µm CMOS. The fully-integrated converter achieves greater than 70% efficiency over an output range from 0.9-2.2V at a 2mA load current, with a peak efficiency of 85%. The architecture is a novel inductor-less recursive topology. The topology opportunistically connects individual 2:1 SC cells either in series or parallel to provide multiple ratios while maximizing capacitance utilization.

APPLICATIONS AND ECONOMIC IMPACT

- This solution can be utilized in a standard CMOS process for a wide range of voltage-regulation applications. The highly integrated solution reduces the number of external components and the system cost.

- The switched-capacitor solution alleviates the need for a high-cost external inductor in the system. The resulting reduction in size provides a more attractive solution for portable systems with small form factors.

Session 5 Highlights: Processors

[5.1] POWER8™: A 12-Core Server-Class Processor in 22nm SOI with 7.6Tb/s Off-Chip Bandwidth

[5.8] A 3GHz 64b ARM v8 Processor in 40nm Bulk CMOS Technology

Paper [5.1] Authors: *E. Fluhr[1], J. Friedrich[1], D. Dreps[1], V. Zyuban[2], G. Still[3], C. Gonzales[4], A. Hall[1], D. Hogenmiller[1], F. Malgioglio[4], R. Nett[1], J. Paredes[1], J. Pille[3], D. Plass[4], R. Puri[2], P. Restle[2], D. Shan[1], K. Stawiasz[2], Z. Deniz[2], D. Wendel[5], M. Ziegler[2]*
Paper [5.1] Affiliation: *[1]IBM STG, Austin, TX; [2]IBM T. J. Watson, Yorktown Heights, NY; [3]IBM STG, Raleigh, NC; [4]IBM STG, Poughkeepsie, NY; [5]IBM STG, Boeblingen, Germany*

Paper [5.8] Authors: *A. Yeung[1], H. Partovi[1], Q. Harvard[1], R. Homer[1], J. Ngai[2], L. Ravezzi[1], M. Ashcraft[1], G. Favor[1]*
Paper [5.8] Affiliation: *[1]Applied Micro, Sunnyvale, CA; [2]Applied Micro, Boxborough, MA*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

CONTEXT AND STATE OF THE ART

- Exploding data growth and analytics requirements continue to demand higher-level thread/core/memory integration to handle “Big Data” in datacenters.
- Solutions to deliver cost-effective servers drive fine-grain, fast-response power management features to minimize energy consumption and a higher level of off-chip component integration for today’s power-constrained datacenters.
- Increased pervasiveness of “Cloud Computing” raises the demand for low-power architectures that can scale out to many cores in dense form factors.

TECHNICAL HIGHLIGHTS

- **IBM Power8™ features 12 8-threaded cores with 96MB of eDRAM L3 and achieves a 2.5× performance improvement over Power7+™.**
- IBM presents the POWER8™ microprocessor featuring 12 cores and 96MB of on-chip L3 cache. The chip is implemented in 22nm SOI eDRAM technology with 15 levels of metal. The processor features 7.6Tb/s of off-chip bandwidth, integrated voltage regulation and resonant clocking.
- **Applied Micro introduces the first server class ARM processor integrating four 4.5W dual-core processors modules running at 3.0 GHz.**
- Applied Micro reveals the first generation 64b v8 ARM 8-core processor. Featuring a 4-wide out-of-order superscalar micro-architecture, the processor is fabricated in 40nm bulk CMOS technology, and operates at 3GHz with a 0.9V supply, consuming 4.5W

APPLICATIONS AND ECONOMIC IMPACT

- The IBM and Applied Micro processors represent two major aspects of processor development: extreme performance for Big Data handling and power efficiency for cloud computing. These greater levels of performance and energy-efficiency in ever more dense form factors will extend our abilities from increasing multimedia social computing to scientific and medical applications, such as understanding human genomes. Businesses will be able to consolidate workloads, increasing their data processing capabilities and enabling lower cost to consumers.

- These processors represent a new level of performance, integration, and innovative circuit techniques to deliver significantly increasing performance and capabilities. These efficient engines will enable servers to handle the most challenging technical applications and help meet the needs for the world's growing cloud computing ecosystem.

Session 6 Highlights: Technologies for High-Speed Data Networks

[6.3] A Heterogeneous 3D-IC Consisting of Two 28nm FPGA Die and 32 Reconfigurable High-Performance Data Converters

Paper Authors: *Christophe Erdmann, Donnacha Lowney, Adrian Lynam, Aidan Keady, John McGrath, Edward Cullen, Daire Breathnach, Denis Keane, Patrick Lynch, Marites De La Torre, Ronnie De La Torre, Peng Lim, A. Collins, Brendan Farley and Liam Madden*

Paper Affiliation: *Xilinx, Dublin, Ireland*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- Historically FPGAs have been single chip systems.
- Exponential growth in bandwidth in FPGA systems is becoming a limiting factor in the system budget with respect to interconnect complexity and associated power.

TECHNICAL HIGHLIHTS

- **Ultra-high performance FPGA 3D-IC system.**
- This work demonstrates a reconfigurable heterogeneous 3D-IC assembled from two 28nm FPGAs and two 65nm mixed signal die on a 65nm interposer in a BGA package.
- An aggregate bandwidth in excess of 400Gb/s using sixteen 16b DAC instances running at 1.6GS/s achieving an FPGA-to-data-converters interface power of 0.3mW/Gb/s..

APPLICATIONS AND ECONOMIC IMPACT

- The integration of flexible data converters with FPGA eliminates the IO cost and also offers a dynamically scalable, power efficient platform solution that addresses diverse applications including high-speed data networking.

Session 7 Highlights: Image Sensors

[7.1] A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12μm Pixel with Front-Side Deep-Trench Isolation and Vertical Transfer Gate

[7.6] A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC

Paper [7.1] Authors: *J. Ahn, K. Lee, Y. Kim, H. Jeong, B. Kim, H. Kim, J. Park, T. Jung, W. Park, T. Lee, E. Park, S. Choi, G. Choi, H. Park, Y. Choi, S. Lee, Y. Kim, Y. Jay Jung, D. Park, S. Nah, Y. Oh, M. Kim, Y. Lee, Y. Chung, I. Hisanori, J. Im, D.-KJ Lee, B. Yim, G. Lee, H. Goto, C. Choi, D. Lee, and G. Han*
Paper [7.1] Affiliation: *Samsung Electronics, Yongin, Korea*

Paper [7.6] Authors: *C. Bamji, A. Payne, A. Daniel, A. Mehta, B. Thompson, D. Snow, H. Oshima, L. Prather, L. Kordus, M. Fenton, P. O'Connor, R. McCauley, S. Nayak, S. Acharya, S. Mehta, T. Elkhatib, T. Meyer, T. O'Dwyer, T. Perry, V.-H. Chan, V. Won, V. Mogallapu, W. Qian, Z. Xu*
Paper [7.6] Affiliation: *Microsoft, Mountain View, CA*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- The race toward high-resolution CMOS image sensors requires pixel shrink below 1.0μm. To improve sensitivity, image sensor technology has migrated from front-side (FSI) to back-side (BSI) illumination. One way to improve signal-to-noise is to reduce crosstalk, requiring isolation between pixels. This is achieved by adopting deep-trench isolation (DTI). However, to further shrink the pixel pitch, a vertical transfer gate is also needed.
- In recent years, 3D Time-of-Flight (ToF) imaging has become a mature technology in gesture control. However, there are still open challenges in combining long-distance range with high-precision depth measurements.

TECHNICAL HIGHLIGHTS

- **First combination of Deep-Trench Isolation combined with Vertical Transfer Gate in BSI technology**
- In Paper 7.1, Samsung Electronics reports the industry's first combined Deep-Trench Isolation and Vertical Transfer Gate in BSI technology, implemented in an 8Mpixel 1.12μm pixel.
- **A 3D image sensor that combines multi-frequency photo-demodulation and adjustable column-level gain**
- In Paper 7.6, Microsoft presents a high-speed multi-frequency photo-demodulation combined with adjustable column-level gain setting that is implemented in a 512×424 pixel array with 10μm pitch.

APPLICATIONS AND ECONOMIC IMPACT

- Paper 7.1 describes a technology innovation that will be exploited in next-generation mobile-device cameras, improving image quality to a level where these will continue to displace compact standalone cameras.
- The technology innovation described in Paper 7.6 replaces the prior triangulation-based generation used by Kinect gesture-recognition gaming consoles.

Session 8 Highlights: *Optical Links and Copper PHYs*

[8.2] A 12×5 Two Dimensional Optical I/O Array for 600Gb/s Chip-to-Chip Interconnect in 65nm CMOS

[8.9] A 40Gb/s VCSEL Over-Driving IC with Group-Delay-Tunable Pre-Emphasis for Optical Interconnection

Paper 8.2 Authors*: H. Morita, K. Uchino, E. Otani, H. Ohtorii, T. Ogura, K. Oniki, Shuichi Oka, S. Yanagawa, H. Suzuki*
Paper 8.2 Affiliation: *Sony, Tokyo, Japan*

Paper 8.9 Authors: *Yukito Tsunoda, Mariko Sugawara, Hideki Oku, Satoshi Ide, Kazuhiro Tanaka*
Paper 8.9 Affiliation: *Fujitsu Laboratories, Kanagawa, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- Traditional optical packaging limits the achievable density of parallel optical interconnects. New dense packaging approaches and associated circuit techniques will enable the penetration of parallel optics into near-processor and related application domains.

- Still further bandwidth growth can be supported by pairing massively parallel optical interconnects with techniques that push VCSELs to operate beyond their nominal data-rates.

TECHNICAL HIGHLIGHTS

- **Ingenious packaging approach enables massively parallel 0.6Tb/s waveguide-coupled optical I/O**
  - Through use of an interposer with a via array, Sony demonstrates the dense connection of drivers and amplifiers to two-dimensional arrays of VCSELs and photodetectors, respectively. The resulting assembly features an ultra-short link between optical elements and electronics, and enables the demonstration of 600Gb/s aggregate data transfer over a 60-channel optical waveguide.
  - The chip is implemented in a 65nm process and achieves input sensitivity of $13.3\mu A_{pp}$ at a BER of 10^{-12}

- **Group delay compensating driver enables VCSEL data-rate extension by 60% to 40Gb/s**
  - A group-delay-compensation pre-emphasis circuit developed by Fujitsu allows use of a 25Gb/s VCSEL at data-rates to 40Gb/s. Use of the group-delay-compensator results in dramatic enhancement in output eye quality.

APPLICATIONS AND ECONOMIC IMPACT

- Aggregate bandwidth requirements for communication between compute nodes separated by a range of distances is extending into the range of Tb/s. Massively parallel, ultra-high speed optical chip-to-chip interconnect solutions have the potential not only to enable continued bandwidth scaling, but also to enable dramatically increased flexibility in system interconnect topologies.

Session 9 Highlights: Low Power Wireless

[9.1] A Self-Calibrating NFC SoC with a Triple-Mode Reconfigurable PLL and a Single-Path PICC-PCD Receiver in 0.11µm CMOS

[9.4] A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components

Paper 9.1 Authors: *W. L. Lien[1], T.Y. Choke[1], Y.C. Tan[1], M. Kong[1], E.C. Low[1], D.P. Li[1], L. Jin[1], H. Zhang[1], C.H. Leow[1], S. L. Chew[1], U. Dasgupta[1], C. H. Yong[1], T. B. Gao[1], G. T. Ong[1], W. G. Tan[1], W. Shu[1], C. L. Heng[1], Osama Shana'A[1,2]*
Paper 9.1 Affiliation: *[1]MediaTek, Singapore, Singapore, [2]MediaTek, San Jose CA*

Paper 9.4 Authors: *Z. Lin[1], P.-I. Mak[1] and R. P. Martins[1,2]*
Paper 9.4 Affiliation: *[1]University of Macau, Macao, China, [2]University of Lisbon, Portugal*

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Helsinki, Finland; Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- Low-power transceivers for short-range wireless communication are emerging in a wide range of frequencies and bandwidths. Novel architecture solutions and circuit techniques are essential in such systems for low-cost and high-energy-efficiency design.

TECHNICAL HIGHLIGHTS

- **First multi-mode multi-standard NFC SoC based on a single receiver**

- In Paper 9.1, Mediatek presents a near-field communication transceiver SOC supporting card-emulation mode, reader mode and peer-to-peer mode. The radio supports cm-range communication at 13.6MHz and fills 1.1mm^2 in 0.11µm CMOS.

- **First ZigBee receiver covering the 433/860/915/960MHz ISM bands with zero external components**

- In paper 9.4, The University of Macau presents a ZigBee receiver in 65nm CMOS for the 433-to-960MHz bands, providing an 8.1dB Noise Figure while consuming 1.15mW. The receiver demonstrates new techniques for current reuse, and employs N-path feedback and downconversion to reuse the input LNA for both RF and baseband signals.

APPLICATIONS AND ECONOMIC IMPACT

- The low-power, multi-mode, fully integrated NFC SOC enables low-cost proximity communications in mobile and other handheld platforms.

- The low-voltage and low-cost wireless radios offer rapid proliferation of Internet-of-Things, Wireless Sensor Networks (WSN), and Body Area Networks (BAN).

Session 10 Highlights:
Mobile Systems-On-Chips (SoCs)

[10.2] A 28nm HPM Heterogeneous Multi-Core Mobile Application Processor with 2GHz Cores and Low-Power 1GHz Cores

[10.4] A 1.22TOPS and 1.52mW/MHz Augmented Reality Multi-Core Processor with Neural Network NoC for HMD Applications

[10.8] A Multi-Standard 2G/3G/4G Cellular Modem Supporting Carrier Aggregation in 28nm CMOS

Paper 10.2 Authors: *M. Igarashi, T.Uemura, R. Mori, N. Maeda, H. Kishibe, M. Nagayama, M. Taniguchi, K. Wakahara, T. Saito, M. Fujigaya, K. Fukuoka, K. Nii, T. Kataoka, T. Hattori*
Paper 10.2 Affiliation: *Renesas Electronics, Tokyo, Japan*

Paper 10.4 Authors: *G. Kim*, *Y. Kim*, *K. Lee*, *S. Park*, *I. Hong*, *K. Bong*, *J. Oh*, *D. Shin*, *S. Choi*, *H-J. Yoo*
Paper 10.4 Affiliation: *KAIST, Daejeon, Korea*

Paper 10.8 Authors: *M. Breschel[1], P. Almers[1], F. Angsmark[1], A. Arvidsson[1], H. Bauer[2], K. van Berkel[3], J. Canovas[1], M. Do[1], A. Ekelund[1], T. Larsson[1], B. Lincoln[1], M. Malmberg[1], M. Naruse[4], M. Onishi[4], C. Östberg[1], J. Smeets[3], M. Escobar[1], J. Voelkl[2], E. Wittenmark[1]*
Paper 10.8 Affiliation: *[1]Ericsson, Lund, Sweden; [2]Ericsson, Nuremberg, Germany; [3]Ericsson, Eindhoven, The Netherlands; [4]Ericsson, Yokohama, Japan*

Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO,*
Energy-Efficient Digital Subcommittee

CONTEXT AND STATE OF THE ART

- Do you want higher performance and better battery life from your mobile devices?
- Augmented reality is the next killer app for your smartphone!
- Do you desire continuous “always-on” connectivity on any network?

TECHNICAL HIGHLIGHTS

- **Renesas unveils their fastest mobile application processor that pushes performance and battery-life limits.**

- This application processor achieves a maximum performance of 35600 DMIPS in an octa-core configuration. Power reduction techniques are employed to achieve 20% reduction of overall dynamic power and 29% leakage power reduction, combined with 20mV suppression of excessive AC-IR drop.

- **Real-time augmented reality for wearable devices – KAIST shows the way.**

- KAIST proposes a real-time markerless augmented-reality processor for wearable electronics. The multicore 65nm chip achieves 1.22TOPS and 1.52mW/MHz for 30fps 720p augmented-reality operation

- **Multi-standard digital baseband SoC supporting carrier aggregation from Ericsson.**

- Ericsson shares details of its first unified SoC architecture for 2G/3G/4G baseband. Highlights include carrier aggregation and a unified baseband architecture. Operating at 1.03V, the modem features an LTE Cat4 downlink of 150Mb/s (10MHz+10MHz aggregated) together with an uplink of 25Mb/s.

APPLICATIONS AND ECONOMIC IMPACT

- The next generation of smart phone and wearable devices demands higher resolution and a richer user experience, while being always connected wherever you are! These compelling usage models are causing consumers worldwide to open their wallets.

- As the number of standards are growing and evolving, mobile devices need to support a wide range of legacy and future standards, while being economically viable. Multi-standard digital basebands are the way forward.

Session 11 Highlights: Data Converter Techniques

[11.2] A 0.85fJ/conversion-step 10b 200kS/s Subranging SAR ADC in 40nm CMOS

[11.4] A 1.5mW 68dB SNDR 80Ms/s 2× Interleaved SAR-Assisted Pipelined ADC in 28nm CMOS

Paper 11.2 Authors: *H-Y Tai, Y-S Hu, H-W Chen, and H-S Chen*
Paper 11.2 Affiliation: *National Taiwan University, Taipei, Taiwan*

Paper 11.4 Authors: *F. van der Goes[1], C. Ward[1], S. Astgimath[2], Han Yan[1], J. Riley[1], J. Mulder[1], S. Wang[1] and K. Bult[1]*
Paper 11.4 Affiliation: *[1]Broadcom, Bunnik, The Netherlands, [2]now at Wolfson Microelectronics PLC, Edinburgh, United Kingdom*

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA, Data Converter Subcommittee*

CONTEXT AND STATE OF THE ART

- Low-power Analog-to-Digital Converters (ADCs) are key building blocks in modern electronics. The power efficiency of an ADC can be measured as the energy consumed per conversion step (the so-called Walden figure of merit).
- SAR ADC resolution and sampling speed continue to improve, but the power efficiency has been limited to over 30fJ/conversion-step for 11+ effective bits and for 50 to 100MS/s designs.
- In general, the figure of merit for all ADCs ever reported had been limited to values greater than 2fJ/conversion-step.

TECHNICAL HIGHLIGHTS

- **Press Headline for Paper 11.2 – Record efficiency of 0.85fJ/conversion-step**
- Combining subranging and successive approximation, this 10b 200kS/s A/D converter is realized using only 84nW of power.
- **Press Headline for Paper 11.4 – A 1.5mW ADC featuring 68dB SNDR at 80MS/s and 9.1fJ/conversion-step**
- A dynamic residue amplifier with optimized noise-filtering properties dramatically reduces the power consumption in the critical portions of this pipelined successive-approximation converter.

APPLICATIONS AND ECONOMIC IMPACT

- These converters, targeting sensor networks and mobile systems, enable great progress in extending battery life and widening the communication bandwidth among humans, and in man-machine interfaces at the edge of the cloud.

Session 12 Highlights: Sensors, MEMS, and Displays

[12.3] A 240Hz-Reporting-Rate 143×81 Mutual-Capacitance Touch-Sensing Analog Front-End IC with 37dB SNR for 1mm-Diameter Stylus

Paper Authors: *Mutsumi Hamaguchi, Akira Nagao, Masayuki Miyamoto*
Paper Affiliation: *Sharp, Fukuyama, Japan*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Touch-screen displays today are typically <10 inches in size.
- State-of-the-art touch-screen displays have a report rate of 120Hz and a 2.5mm size resolution.

TECHNICAL HIGHLIGHTS

- **Biggest ever capacitive touch-screen display!**
- This paper demonstrates a 70-inch display touch-screen controller.
- The report rate is 2× higher (240Hz) than the state of the art at a 1mm size resolution.

APPLICATIONS AND ECONOMIC IMPACT

- This will open up new application areas for touch-screen controllers. These include large displays for interactive television or interactive advertisement screens.
- Due to the higher resolution and reporting rate, better pattern recognition and error detection are enabling a more natural user experience.

Session 12 Highlights: Sensors, MEMS, and Displays

[12.9] A 1.55×0.85mm² 3ppm 1.0µA 32.768kHz MEMS-Based Oscillator

Paper Authors: *Samira Zaliasl[1], Shouvik Mukherjee[1], Will Chen[1], Kimo Joo[1], Raj Palwi[1], Niveditha Arumugam[1], Preston Galle[1], Meghan Phadke[1], Jim Salvia[2], Haechang Lee[1], Charles Grosjean[1], Sudhakara Pamarti[3], Teri Fiez[4], Kofi Makinwa[5], Aaron Partridge[1], Vinod Menon[1]*
Paper Affiliation: *SiTime, Sunnyvale CA[1], InvenSense, Sunnyvale, CA[2], University of California, Los Angeles, CA[3], Oregon State University, Corvallis, OR[4], Delft University of Technology, Delft, Netherlands[5]*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Today's real-time clocks operate from quartz-based crystals.
- These are rather bulky (~2×2 to 5×10mm²) and therefore need a lot of PCB board space.
- To achieve sub-10ppm resolution, complex trimming at multiple temperatures is needed, making these products rather expensive.

TECHNICAL HIGHLIGHTS

- **Smallest and most accurate ultra-low-power 32kHz MEMS clock replaces quartz**
- Much smaller required board space (1.55×0.85mm²) enables smaller applications, or more features in applications like smart watches or phones.

APPLICATIONS AND ECONOMIC IMPACT

- Real-time clock sources are part of almost every consumer product.
- Smaller size enables more features for similar-sized consumer products.

Session 13 Highlights: Advanced Embedded Memory

[13.1] A 1Gb 2GHz Embedded DRAM in 22nm Tri-Gate CMOS Technology

Paper 13.1 Authors: *F. Hamzaoglu, U. Arslan, N. Bisnik, S. Ghosh, M. Lal, N. Lindert, M. Meterelliyoz, R. Osborne, J. Park, S. Tomishima, Y. Wang, K. Zhang*
Paper 13.1 Affiliation: *Intel, Hillsboro, OR*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee*

CONTEXT AND STATE OF THE ART

- High-speed eDRAM is an increasingly important alternative to SRAM in certain applications to improve bandwidth and capacity.

- As the need for increased on-chip, high-bandwidth memory has continued to grow unabated, driven by high-bandwidth computing, technologists have looked to alternatives to traditional SRAM. In this year's paper in advanced embedded memory, Intel demonstrates an embedded DRAM in their leading edge 22nm FinFET technology to bridge the capacity and bandwidth gap.

TECHNICAL HIGHLIGHTS

- **Intel introduces first 22nm eDRAM to improve graphics performance in high-end CPUs**

- In Paper 13.1, Intel demonstrates a 1Gb 2GHz embedded DRAM using a 22nm tri-gate logic process. A 128Mb macro achieves a density of 17.5Mb/mm^2 using a cell size of 0.029μm^2. The paper demonstrates 2GHz operation at 1.05V and 1GHz operation at 0.7V.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrates eDRAM on 22nm tri-gate technology

- With more than 50% of the transistors used for on-chip memory in current high-performance systems, eDRAM represents a key enabler of future high- bandwidth computing systems.

Session 13 Highlights: Advanced Embedded Memory

[13.2] A 14nm FinFET 128Mb 6T SRAM with V_{MIN}-Enhancement Techniques for Low-Power Applications

[13.5] A 16nm 128Mb SRAM in High-κ Metal-Gate FinFET Technology with Write-Assist Circuitry for Low V_{MIN} Applications

Paper 13.2 Authors: *T. Song, W. Rim, J. Jung, G. Yang, J. Park, S. Park, K.-H. Baek, S. Baek, S. Oh, J. Jung, S. Kim, G. Kim, J. Kim, Y. Lee, K. S. Kim, S.-P. Sim, J. S. Yoon, K.-M. Choi*
Paper 13.2 Affiliation: *Samsung Electronics, Yongin, Korea*

Paper 13.5 Authors: *Y.-H. Chen, W.-M. Chan, W.-C. Wu, H.-J. Liao, S. Natarajan, J. Chang, J.-J. Liaw*
Paper 13.5 Affiliation: *TSMC, Hsinchu, Taiwan*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee*

CONTEXT AND STATE OF THE ART

- SRAM is the main barrier to logic scaling.
- Since the demonstration of 22nm FinFET products at the ISSCC in 2012, competition in the industry has accelerated as major players are transitioning to FinFET technology.
- This year's papers on advanced embedded memory demonstrate SRAM designs in leading edge FinFET technologies from major industry players to continue density scaling into the 14/16nm nodes.

TECHNICAL HIGHLIGHTS

- **Samsung demonstrates a 14nm SRAM with highest density reported to date**
- In Paper 13.2, Samsung describes the first 14nm FinFET SRAM with the smallest bit cell size reported to date (0.064μm^2). By using innovative read/write assist schemes, up to a 200mV V_{MIN} improvement for the 0.064μm^2 cell is shown.
- **TSMC introduces a 16nm SRAM with assist circuit techniques to improve V_{MIN} by 300mV to extend battery life in mobile applications.**
- In Paper 13.5, TSMC describes the write-assist techniques used for their 0.073μm^2 16nm FinFET SRAM bit cell. Silicon results demonstrating over 300mV improvement in V_{MIN} are shown.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrates FinFET transistor scaling to 14/16nm node.
- This technology and the innovative circuit techniques enable low-voltage operation to lower power and extend battery life in a wide range of mobile applications.

Session 14 Highlights: RF Subcommittee

[14.5] A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13µm SiGe BiCMOS

Paper Authors: *Ullrich Pfeiffer[1], Yan Zhao[1], Janusz Gryzb[1], Richard Al Hadi[1], Neelanjan Sarmah[1], Wolfgang Förster[1], Holger Rücker[2], Bernd Heinemann[2]*
Paper Affiliation: *[1]University of Wuppertal, Wuppertal, Germany; [2]IHP, Frankfurt (Oder), Germany*

Subcommittee Chair: *Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- The THz frequency range (300GHz to 3THz) has many applications in imaging, sensing, and high-data-rate communications.
- Low-cost implementation of THz systems is challenging due to the limited cut-off frequency of devices.

TECHNICAL HIGHLIGHTS

- **First ever milliwatt-level signal source operated at a half-THz in silicon.**
- In Paper 14.5, The University of Wuppertal and IHP present a reconfigurable 16-element radiator array at 0.53THz in a 0.13µm SiGe BiCMOS process.
- Similar to visual light, the radiation from each element within the array is diffuse or non-coherent which improves the illumination of a scene by eliminating specular reflection. Operating at 0.5THz provides enhanced resolution over existing lower-frequency systems.
- The radiated power from the 16 pixel array is 1mW, which is enough for many imaging applications. Higher power can be achieved through simply scaling the array size.

APPLICATIONS AND ECONOMIC IMPACT

- Portable THz sources can revolutionize imaging and sensing applications. There are many applications in the areas of security, bio-sensing, and imaging that will benefit from this work.
- Low cost solutions to existing THz systems allow rapid uptake of the technology.

Session 15 Highlights: Digital PLLs

[15.1] A 0.066mm² 780µW Fully Synthesizable PLL with a Current-Output DAC and an Interpolative Phase-Coupled Oscillator Using Edge-Injection Technique

Paper Authors: *W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, A. Matsuzawa*
Paper Affiliation: *Tokyo Institute of Technology, Tokyo, Japan*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

CONTEXT AND STATE OF THE ART

- Digital SoCs, from mobile applications to large compute data centers, depend on a solid, steady heartbeat provided by a phase-locked loop (PLL) circuit.

- PLLs were traditionally built with analog logic components, which required custom fabrication steps and lengthy silicon debug cycles. The emergence of digital PLLs is driving cost reduction in modern processors as they eliminate custom steps and components. Digital implementations enable rapid exploitation of cutting-edge process technologies.

TECHNICAL HIGHLIGHTS

- **A phase-locked loop synthesized from standard-cell library components enables low-cost and rapid adoption of new processes, accelerating time-to-market for complex SoCs.**

- The Tokyo Institute of Technology presents a 780µW fully synthesizable PLL with a current-output DAC and an interpolative phase-coupled oscillator using an edge-injection technique. This design introduces a current digital-to-analog converter composed of standard CMOS NAND gates. The PLL is completely assembled using standard-cell components and automatic place-and-route. The PLL occupies 0.0066mm² in 65nm CMOS operating from 390MHz to 1.41GHz.

APPLICATIONS AND ECONOMIC IMPACT

- Eliminating laborious custom work required for digital PLLs reduces time-to-market and development cost for SoCs.

- A fully synthesizable PLL from standard-cell components can now be rapidly designed and targeted to specific applications with better power and performance attributes.

Session 16 Highlights: SoC Building Blocks

Paper 16.2: A 0.19pJ/b PVT-Variation-Tolerant Hybrid Physically Unclonable Function Circuit for 100% Stable Secure Key Generation in 22nm CMOS

Paper 16.3: A 23Mb/s 23pJ/b Fully Synthesized True-Random-Number Generator in 28nm and 65nm CMOS

Paper 16.2 Authors: *S. K. Mathew*, *S. K. Satpathy*, *M. A. Anders*, *H. Kaul*, *S. K. Hsu*, *A. Agarwal*, *G. K. Chen*, *R. J. Parker*, *R. K. Krishnamurthy*, *V. De*
Paper 16.2 Affiliation: *Intel, Intel, Hillsboro, OR*

Paper 16.3 Authors: *K. Yang*, *D. Fick*, *M. B. Henry*, *Y. Lee*, *D. Blaauw*, *D. Sylvester*
Paper 16.3 Affiliation: *University of Michigan, Ann Arbor, MI*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

CONTEXT AND STATE OF THE ART

- Secure systems are becoming increasingly more important as electronics become embedded in our daily lives. Building blocks for secure systems include true-random-number generators and physically unclonable function circuits.

- For these building blocks to be included in designs, they need to be small, power efficient and portable to the latest technology nodes. These components have to be robust to process, voltage and temperature variations, as well as inadvertent interactions with other system-on-chip components, and intentional outside attacks.

TECHNICAL HIGHLIGHTS

- **Intel introduces a variation-tolerant on-chip security key generator.**
  The 22nm design has the lowest reported energy consumption of 0.19pJ/b and the highest reported operating frequency, while maintaining high immunity to probing attacks. A number of techniques are used to ensure the randomness and consistency of key generation under a variety of process, environmental, aging and attack conditions.

- **The University of Michigan presents the first fully synthesized true random number generator that passes all NIST randomness tests.**
  The design is demonstrated in both 65nm and 28nm processes to illustrate its ease of technology portability. Phase-noise accumulation in on-chip ring-oscillators is leveraged in a way that guarantees unbiased randomness, while being robust to intentional attacks and inadvertent on-chip interactions.

APPLICATIONS AND ECONOMIC IMPACT

- Integrated and robust security blocks will enable new privacy and security capabilities of consumer devices and open the door to a range of new applications in the mobile domain, such as secure online transactions, data storage and exchange.

- Increased security of consumer devices and application development will stimulate strong economic growth in the mobile and consumer market.

Session 17 Highlights: Analog Techniques

[17.7] A 1.89nW/0.15V Self-Charged XO for Real-Time Clock Generation

Paper Authors: *Keng-Jan Hsiao*
Paper Affiliation: *Mediatek, Hsin-chu, Taiwan*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- XO circuits typically use a Pierce oscillator that uses amplitude control to achieve sub-μW power consumption. Also differential topologies have been introduced to achieve superior power efficiency.

- Prior art utilizes amplifiers that operate in the linear region and consume static power. Alternatively, the amplifier is replaced with a complex DLL-based design, which requires multiple power domains with high supply voltages.

TECHNICAL HIGHLIGHTS

- **The smallest area (0.03 mm^2) and record power consumption (1.89nW) reported for a 32.768 kHz XO to date:** Paper 17.7 describes the design of a single-supply self-charged XO, fabricated in 28nm CMOS. The circuit drives the crystal with pulses utilizing a direct-charging scheme to reduce the power and supply voltage. This makes the design more logic oriented. The frequency drift is less than 48.8 ppm from -20C to 80C. The circuit operates from a single supply with a voltage as low as 0.15 V.

APPLICATIONS AND ECONOMIC IMPACT

- The design can be widely used in major consumer electronic and wireless products utilizing an ultra-low power system clock. It is demonstrated in a mainstream CMOS process and is implemented in a small area, making it an attractive solution for integration in SoCs.

- The low power consumption of this system allows for significant saving of battery power when the oscillator is used for system clock in stand-by mode or for low-power applications. The new benchmark in power efficiency allows for much longer battery life and reduces the system cost.

Session 18 Highlights:
Biomedical Systems for Improved Quality of Life

[18.1] A 1V 3mA 2.4GHz Wireless Digital Audio Communication SoC for Hearing-Aid Applications in 0.18um CMOS

[18.2] A Fully Implantable Cochlear Implant SoC with Piezoelectric Middle-Ear Sensor and Energy-Efficient Stimulation in 0.18um HVCMOS

Paper 18.1 Authors: *A. El-Hoiydi[1], F. Callias[1], Y. Oesch[1], C. Kuratli[2], R. Kvacek[3]*
Paper 18.1 Affiliation: *[1]Phonak Communications, Murten, Switzerland, [2]EM Microelectronic-Marin, Marin, Switzerland, [3]ASICentrum, Prague, Czech Republic*

Paper 18.2 Authors: *M.Yip[1], R. Jin[1], H. Nakajima[2,3], K. Stankovic[2,3], A. Chandrakasan[1]*
Paper 18.2 Affiliation: *[1]Massachusetts Institute of Technology, Cambridge, MA, [2]Harvard Medical School, Boston, MA, [3]Massachusetts Eye and Ear Infirmary, Boston, MA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- Assistive listening devices treat a variety of auditory conditions, and range from hearing aids for treating mild or moderate hearing loss to cochlear implants for patients suffering from profound deafness. The requirement for these devices to be unobtrusive and comfortable for the user places severe size and power constraints on the entire system design.
- Adding wireless connectivity to hearing aids enables features such as background noise reduction and connection to remote microphones. Current wireless hearing aids are based on narrowband FM systems, which offer simple, low power implementation but suffer from limited data rate and susceptibility to interference.
- Conventional cochlear implants require an external behind-the-ear unit comprising a microphone and sound processor, since size and power constraints preclude systems from being completely implantable. This external unit is aesthetically undesirable for the user as well as restricting use in the shower or while swimming.

TECHNICAL HIGHLIGHTS

- **The world's lowest power 2.4 GHz wireless digital audio SoC suitable for miniature hearing aid applications:**
  The SoC consumes 3mA at 1V while receiving a 7kHz BW audio signal in good link situations, and with the help of an embedded DC-DC converter using delta-sigma control, the SoC is able to reject noise in the audible frequency band.
- **The first cochlear implant system suitable for complete implantation including a piezoelectric microphone mounted within the inner ear:**
  The SoC consumes a total of 572uW, and contains a 0.6V reconfigurable sound processor with adaptive channels and a programmable neural stimulator providing energy-optimal waveforms.

APPLICATIONS AND ECONOMIC IMPACT

- Miniaturized hearing aids can now be enhanced with reliable, robust and low latency wireless connectivity without sacrificing battery lifetime or significantly increasing form factor. Applications include wireless audio connection to mobile phones or microphones, and binaural audio beam-forming for background noise reduction.

- Cochlear implants can become fully implantable, giving significantly improved quality of life to profoundly deaf patients worldwide.

Session 18 Highlights:
Biomedical Systems for improved quality of life

[18.3] A Multi-Parameter Signal Acquisition SoC for Connected Personal Health Applications

Paper Authors: *Nick Van Helleputte[1], Mario Konijnenburg[2], Hyejung Kim[1], Julia Pettine[2], Dong-Woo Jee[1], Arjan Breeschoten[2], Alonso Morgado[1],Tom Torfs[1], Harmke de Groot[2], Chris Van Hoof[1],2, Refet Firat Yazicioglu[1]*
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Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- Connected personal healthcare, or medical consultation at a distance, requires smart, miniature wearable devices that can collect and analyze physiological and environmental parameters without the intervention of medical practitioners.

- Ensuring medical-grade signal quality, multi-sensor support, generic signal processing and low-power specifications is a challenge.

TECHNICAL HIGHLIGHTS

- A general-purpose platform to address numerous medical applications is realized with a SoC containing versatile analog front-ends (AFE), a power-efficient signal processor (DSP) and hardware accelerators.

- The AFE has 3 channels for biopotential readout consuming 31uW per channel and one bioimpedance readout consuming 58uW.

- The DSP includes real-time motion artifact reduction with a general-purpose microcontroller, and a dedicated hardware accelerator achieving more than10x energy-savings in vector multiply-accumulate executions.

APPLICATIONS AND ECONOMIC IMPACT

- This paper enables low-cost implementation of a variety of personal health applications that require high flexibility, multi-sensors front-ends, and execution of various signal processing algorithms with a single low power SoC.

Session 19 Highlights: Nonvolatile Memory Solutions

[19.1] A 128Gb MLC NAND Flash Device Using 16nm Planar Cell

[19.5] Three-Dimensional 128Gb MLC Vertical NAND Flash Memory with 24-WL Stacked Layers and 50MB/s High-Speed Programming

Paper 19.1 Authors: *M. Helm, J.K. Park, A. Ghalam, J. Guo, C. Ha, C. Hu, H. Kim, K. Kavalipurapu, E. Lee, A. Mohammadzadeh, V. Moschiano, D. Nguyen, V. Patel, T. Pekny, B. Saiki, D. Song, J. Tsai, V. Viajedor, L. Vu, T. Wong, J.H. Yun, R. Ghodsi, A. D'Alessandro, D. Di Cicco, V. Moschiano*
Paper 19.1 Affiliation: *Micron, San Jose, CA*

Paper 19.5 Authors: *K.T. Park, J.M. Han, D. Kim, S. Nam, K. Choi, M. Kim, P. Kwak, D. Lee, Y.H. Choi, K.M. Kang, M.H. Choi, D.H. Kwak, H.W Park, S.W. Shim, H.J. Yoon, D. Kim, S.W. Park, K. Lee, K. Ko, D.K. Shim, Y.L. Ahn, J. Park, J. Ryu, D. Kim, K. Yun, J. Kwon, S. Shin, S.J. Kim, C. Kim, D. Youn, W.T. Kim, T. Kim, H.C. Lee, S. Seo, H.G. Kim, D.S. Byeon, H.J. Yang, M. Kim, B.H. Kim, M.S. Kim, J. Yeon, S. Shim, C. Yeo, J. Jang, J. Song, H.S. Kim, W. Lee, D. Song, S. Lee, K.H. Kyung, J.H. Choi*
Paper 19.5 Affiliation: *Samsung Electronics, Hwasung, Korea*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee*

CONTEXT AND STATE OF THE ART

- **Flash Clash at ISSCC for higher density, 2D vs. 3D**
  - Faced with on-going difficulties to further scale down planar cell technology, Paper 19.1 shows yet another aggressive scaling of 2D NAND Flash technology transitioning from the previously published 20nm technology down to 16nm.
  - To address the ever-growing scaling challenges such as manufacturing cost increase and reliability degradation in the conventional 2D NAND Flash memories, Paper 19.5 shows a new 3D MLC NAND memory device with the promise of lower manufacturing cost and superior device scalability.
  - The highest density MLC NAND Flash published at ISSCC so far is 64Gb with 19nm 2D technology.

TECHNICAL HIGHLIGHTS

- **First ever 16nm 2D MLC 128Gb NAND Flash**
  - [19.1] The highest density with high-κ dielectric/metal-gate planar cell MLC NAND Flash developments of 128Gb with 173.3mm^2.
  - [19.1] A center-page buffer architecture achieving fast read and write performance of 48µs and 1260µs, respectively.

- **First ever 3D MLC 128Gb NAND Flash**
  - [19.5] Industry-first 128Gb three dimensional (3D) NAND Flash memory
  - [19.5] 2-plane architecture with 50MB/s programming throughput and power-reduction techniques

APPLICATIONS AND ECONOMIC IMPACT

- With the introduction of monolithic 128Gb MLC NAND Flash, NAND Flash is ready to storm the data centers in addition to everyday storage in laptops.

- NAND Flash memory-based SSD market is expected to reach up to $15 billion USD in 2014.

Session 20 Highlights: Wireless Systems

[20.2] A 16TX/16RX 60GHz 802.11ad Chipset with Single Coaxial Interface and Polarization Diversity

[20.6] A Blocker-Resilient Wideband Receiver with Low-Noise Active Two-Point Cancellation of >0dBm TX Leakage and TX Noise in RX Band for FDD/Co-Existence

Paper 20.2 Authors: *M. Boers[1], I. Vassiliou[2], S. Sarkar[1], S. Nicolson[1], E. Adabi[1], B. Afshar[1], B. Perumana[1], T. Chalvatzis[2], S. Kavadias[2], P. Sen[1], W. L. Chan[1], A. Yu[1], A. Parsa[3], S. Yoon[1], A. G. Besoli[1], C. Kyriazidou[2], G. Zochios[2], N. Kocaman[1], A. Garg[1], H. Eberhart[1], P. Yang[1], H. Xie[1], H. J. Kim[1], A. T. Mehrabani[1], M. K. Wong[4], D. P. Thirupathi[1], S. Mak[3], R. Srinivasan[1], A. Ibrahim[1], E. Sengul[1], V. Roussel[1], P-C. Huang[1], T. Yeh[3], M. Mese[1], J. Castaneda[1], B. Ibrahim[1], T. Sowlati[1], M. Rofougaran[1], A. Rofougaran[1]*
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Paper 20.6 Authors: *J. Zhou, P. R. Kinget, and H. Krishnaswamy*
Paper 20.6 Affiliation: *Columbia University, New York, NY*

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Helsinki, Finland; Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- Progress in 60GHz wireless communications continues. System- and circuit-level innovations continue to increase the data-rate, reduce the power consumption and cost, and enhance the link reliability of 60GHz wireless devices.
- New wireless standards need to support full-duplex wireless communication across multiple frequency bands. New solutions are needed to satisfy the wireless standard requirements in a small-form-factor, low-cost platform.

TECHNICAL HIGHLIGHTS

- **Full-featured 802.11ad chipset with an integrated beamforming and polarization diversity [20.2]**
- In Paper [20.2], the chipset supports up to 64-QAM modulation and throughput of over 3.5Gb/s at 10m while consuming 960mW and 1190mW in the receive and transmit modes, respectively.
- **Sophisticated low-noise active TX leakage cancellation technique that enables FDD/co-existence in software-defined radios[20.6]**
- In Paper [20.6], the 65nm CMOS chip can cancel up to +2dBm peak transmit leakage at the receiver input, enabling an effective IIP3 of +30dBm (enhancement of 18dB) with an associated increase in NF of < 0.5dB.

APPLICATIONS AND ECONOMIC IMPACT

- IEEE 802.11ad supports data rates up to 6.7Gb/s, enabling demanding applications such as wireless docking, ultra-fast file transfer and low-latency video streaming in handsets, laptops and consumer electronic devices.
- The software-defined radio CMOS chip, with transmit-leakage canceller, enables multi-band, low-cost, low-power, compact mobile devices that can support time- and frequency-division duplexing.

Session 21 Highlights:
Frequency Generation Techniques

[21.1] A 1.7GHz MDLL-Based Fractional-N Frequency Synthesizer with 1.4ps RMS Integrated Jitter and 3mW Power Using a 1b TDC

Paper Authors: *Giovanni Marucci, Andrea Fenaroli, Giovanni Marzin, Salvatore Levantino, Carlo Samori, Andrea L. Lacaita*
Paper Affiliation: *Politecnico di Milano, Milano, Italy*

Subcommittee Chair: *Andreia Cathelin, ST Microelectronics, France, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Multiplying Delay-Locked Loops (MDLL) that achieve low power and low jitter have been the heart of countless systems. However, the integer-only multiplication ratio has been limiting its applications.

- With the advancement of having fine fractional resolution, MDLL can now be expanded into a variety of applications.

TECHNICAL HIGHLIGHTS

- **The first MDLL-based frequency synthesizer with fine fractional-N resolution**.

- In Paper 21.1, researchers from Politecnico di Milano demonstrate fractional-N operation that is achieved by adding a digitally controllable delay on the reference path. The power consumption of 3mW is more than three times lower than state-of-the-art ring-oscillator-based approaches.

APPLICATIONS AND ECONOMIC IMPACT

- As frequency generation is responsible for a significant portion of the power consumption in transceivers, reducing power consumption in frequency synthesizers by more than a factor of three accounts for a considerable energy reduction in present-day communication systems.

- Techniques used for jitter reduction in integer MDLLs can now be applied more widely in fractional-N frequency synthesizers, leading to better system performance such as higher data-rates and increased interference robustness.

Session 22 Highlights:
High-Speed Data Converters

[22.1] A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS

[22.2] A 69.5mW 20GS/s 6b Time-Interleaved ADC with Embedded Time-to-Digital Calibration in 32nm CMOS SOI

Paper 22.1 Authors: *L Kull[1,2], T. Toifl[1], M. Schmatz[1], P. Francese[1], C. Menolfi[1], M. Braendli[1], M. Kossel[1], T. Morf[1], T. Andersen[1], Y. Leblebici[2]*
Paper 22.1 Affiliation: *[1]IBM Research, Zurich, Rueschlikon, Switzerland; [2]EPFL, Lausanne, Switzerland*

Paper 22.2 Authors: *V. Chen and L. Pileggi*
Paper 22.2 Affiliation: *Carnegie Mellon University, Pittsburgh, PA*

Subcommittee Chair: *Boris Murmann, Stanford University, CA, Data Converters Subcommittee*

CONTEXT AND STATE OF THE ART

- Future optical communication standards such as ITU OTU-4 and 400Gb/s Ethernet require ADCs with sampling rates exceeding several 10's of GS/s and at least 5 effective bits to enable equalization in the digital domain.

- Recently, interleaved successive-approximation register (SAR) ADCs have proven to be a superior choice for achieving medium resolution at very high sampling rates.

TECHNICAL HIGHLIGHTS

- **Fastest CMOS ADC at 90GS/s in 32nm SOI CMOS**

- In Paper 22.1, IBM presents a 90GS/s 8b time-interleaved ADC in a 32nm SOI CMOS. It contains 64 SAR ADC channels. The converter maintains greater than 33dB SNDR up to 19.9GHz input frequency. It consumes 667mW from a 1.2V supply.

- **20GS/s 6b time-interleaved SAR ADC with record FoM for >10GS/s ADCs**

- In Paper 22.2, Carnegie Mellon University presents a 20GS/s 6b time-interleaved ADC in 32nm SOI CMOS. It contains 8 flash ADC channels and uses on-chip calibration to reduce gain, offset, and delay mismatches. It achieves 30.7 dB SNDR up to Nyquist input frequencies. It consumes 69.5mW from a 0.9V supply.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced 32nm SOI CMOS technology and highly interleaved SAR architectures enable next-generation >20Gb/s ADC-based wireline communication systems.

- Low-power consumption and small area realize low-cost and highly integrated systems

Session 23 Highlights: Energy Harvesting

[23.3] A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor DC-DC Converter

Paper Authors: *Wanyeong Jung, Sechang Oh, Suyoung Bang, Dennis Sylvester, David Blaauw*
Paper Affiliation: *University of Michigan, Ann Arbor, MI*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Recent advances in low-power circuits have enabled mm-scale wireless sensor networks and implantable devices. Energy harvesting is an attractive way to power such systems due to limited energy capacity of batteries at small form factors.

- Size limitation restricts the amount of harvested power, which can be as low as 10s of nW for millimeter-scale photovoltaic cells in indoor conditions. Efficient DC-DC up-conversion at such low power levels is extremely challenging and has not yet been demonstrated.

TECHNICAL HIGHLIGHTS

- **nW energy harvester maintains >35% end-to-end efficiency with lowest published power consumption:**
  Paper 23.3 presents a 3nW fully integrated energy harvester based on a self-oscillating switched-capacitor (SC) DC-DC converter. Two coupled ring oscillators in the SC voltage-doubler naturally synchronize, removing power overhead from clock generation and level shifters. The circuit converts 7nW input power from 250mV to 4V, and self-starts at 140mV.

APPLICATIONS AND ECONOMIC IMPACT

- The wide range of operation for this circuit allows for its utilization in many wireless sensor networks and implantable systems that have previously utilized a battery.

- Replacing the battery in the system decreases the overall cost and improves the quality of usage for implantable devices.

Session 24 Highlights: Integrated Biomedical Systems

[24.2] A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep-Brain Stimulation

[24.7] A 60nV/√Hz 15-Channel Digital Active Electrode System for Portable Biopotential Signal Acquisition

Paper [24.2] Authors: *Hyung-Min Lee[1], Ki-Yong Kwon[2], Wen Li[2], and Maysam Ghovanloo[1]*
Paper [24.2] Affiliation: *[1]Georgia Institute of Technology, Atlanta, GA, [2]Michigan State University, East Lansing, MI*

Paper [24.7] Authors: *Jiawei Xu[1,2], Benjamin Büsze[1], Hyejung Kim[4], Kofi Makinwa[2], Chris Van Hoof[3,4], Refet Firat Yazicioglu[1,4]*
Paper [24.7] Affiliation: *[1]Holst Center/imec, Eindhoven, The Netherlands, [2]Delft University of Technology, Delft, The Netherlands, [3]KU Leuven, Leuven, Belgium, [4]imec, Leuven, Belgium*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Brain disorders affect up to one billion people worldwide and are one of the greatest health burdens to our society. Yet only limited treatments exist for most people suffering from these devastating disorders. Neurologists and neurosurgeons need new tools to improve diagnostics and therapy for such disorders. Wearable EEG monitoring and neuromodulation are emerging to address these needs.

TECHNICAL HIGHLIGHTS

- **Switched-capacitor-based neuro-stimulation enables highest efficiency yet**

- The integrated switched-capacitor stimulation (SCS) system combines stimulator efficiency (battery to electrode) with stimulus efficiency (electrode to neural tissue). SCS achieves stimulation efficiency as high as 80.4%.

- **The first active dry electrode interface for wearable EEG monitoring**

- The extremely high input impedance (1GΩ) and low-noise (0.65μV_{rms}) of the architecture ensure high signal quality from dry electrodes. The 4-wire digital output minimizes the cabling, also improving the EMI robustness. The contact impedance measurement and DC coupling ensure reliable acquisition in remote patient monitoring applications.

APPLICATIONS AND ECONOMIC IMPACT

- Neuromodulation has strong potential to treat brain disorders, particularly in drug-resistant cases, as evidenced by deep brain stimulation (DBS) to treat Parkinson's disease tremor and dystonia. Today's DBS devices are powered by batteries implanted in the chest that must be replaced every few years. A wireless power-efficient stimulator is reported without size, lifetime, and discomfort issues of traditional DBS, leading to less-invasive head-mounted DBS.

Session 25 Highlights:
High-Bandwidth Low-Power DRAM and I/O

[25.1] A 3.2Gb/s/pin 8Gb 1.0V LPDDR4 SDRAM with Integrated ECC Engine for Sub-1V DRAM Core Operation

Paper 25.1 Authors: *T. Oh, H. Chung, Y. Cho, J. Ryu, K. Lee, C. Lee, J. Lee, H. Kim, M. Jang, G. Han, K. Kim, D. Moon, S. Bae, J. Park, K. Ha, J. Lee, S. Doo, J. Shin, C. Shin, K. Oh, D. Hwang, T. Jang, C. Park, K. Park, J. Lee, J. Choi*
Paper 25.1 Affiliation: *Samsung Electronics, Hwasung, Korea*

Subcommittee Chair: *Kevin Zhang, Intel, OR, Memory Subcommittee*

CONTEXT AND STATE OF THE ART

- LPDDR3 has been established as the leading DRAM device in the past in mobile applications and has entered the mass-production phase. However, new mobile systems are demanding higher bandwidth, lower power along with higher capacity.

TECHNICAL HIGHLIGHTS

- **First-ever reported LPDDR4 with highest data-rate, lowest supply voltage, and highest density**

- In Paper 25.1, Samsung demonstrates LPDDR4 SDRAM for the first time. It has 8Gb density and is implemented in 25nm DRAM process technology. It achieves a data rate of 3.2Gb/s/pin at 1.0V supply voltage and has an integrated ECC engine for sub-1V operation.

APPLICATIONS AND ECONOMIC IMPACT

- This device is going to be used for high-performance low-power next generation handheld devices including smart phones.

- All the LPDDR3 DRAMs currently being used are expected to be replaced by LPDDR4 DRAMs by 2014/2015.

Session 25 Highlights:
High-Bandwidth Low-Power DRAM and I/O

[25.2] A 1.2V 8Gb ×8 Channel 128GB/s High Bandwidth Memory (HBM) DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV Technology

Paper 25.2 Authors: *D. Lee, K. Kim, K. Kim, H. Kim, J. Kim, Y. Park, J. Kim, D. Kim, H. Park, J. Shin, J. Cho, K. Kwon, M. Kim, J. Lee, K. Park, B. Chung, S. Hong*
Paper 25.2 Affiliation: *SK Hynix, Icheon, Korea*

Subcommittee Chair: *Kevin Zhang, Intel, OR, Memory Subcommittee*

CONTEXT AND STATE OF THE ART

- GDDR5 has been established as the leading DRAM device in the past in graphics applications and has entered the mass-production phase. However, new high-performance systems are demanding much higher bandwidth with higher density.

TECHNICAL HIGHLIGHTS

- **First-ever reported High-Bandwidth Memory (HBM) with highest bandwidth and highest density**

- In Paper 25.2, SK Hynix discloses High-Bandwidth Memory (HBM) for the first time. It is implemented in 29nm DRAM process technology. It consists of 4 TSV stacked layers with total density of 8Gb. It shows high bandwidth of 128GB/s at 1.2V supply voltage with 8 channels and total number 1024 I/Os.

APPLICATIONS AND ECONOMIC IMPACT

- This device is going to be used for high-performance next-generation high-end devices including graphics and network applications.

- HBMs are expected to create many new applications requiring higher bandwidth in future memory sub-systems.

Session 26 Highlights

[26.1] A 130mW 20Gb/s Half-Duplex Serial Link in 28nm CMOS

[26.2] A 202mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS

Paper 26.1 Authors: *V. Balan, O. Oluwole, G. Kodani, C. Zhong, S. Maheswari, R. Dadi, A. Amin, G. Bhatia, Peter Mills, Ahmed Ragab, Ming-Ju Lee,*
Paper 26.1 Affiliation: *nVidia, Santa Clara, CA*

Paper 26.2 Authors: *J. Jaussi, G. Balamurugan, S. Hyvonen, T.-C. Hsueh, T. Musah, G. Keskin, S. Shekhar, J. Kennedy, S. Sen, M. Mansuri, M. Leddige, B. Horine, C. Roberts, R. Mooney, B. Casper*
Paper 26.2 Affiliation: *Intel, Hillsboro, OR*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- At ISSCC 2013, researchers from Intel reported a low-power 16Gb/s/lane parallel link consuming 2.6pJ/b. This forwarded-clock link used a TX FIR and CTLE to equalize up to 18dB channel loss. Signaling reach and power were improved by co-designing the transceiver circuitry with a low-loss cable and top-side interconnect launch

- At ISSCC 2012, engineers from Rambus reported a 16Gb/s bi-directional link consuming 4.1pJ/b. They used coded differential signaling to achieve the effect of a 1-tap DFE, along with linear RX equalization, to mitigate ISI across a 15dB channel with a forwarded clock.

TECHNICAL HIGHLIGHTS

- **nVidia reports a 320Gb/s link, one of the fastest aggregate data-rates to date**
- In Paper 26.1, nVidia shows a 20Gb/s/lane × 16-lane parallel transceiver in 28nm CMOS using a single-tap reconfigurable FFE transmitter and a receiver with a single-stage continuous-time linear equalizer and a 2-tap DFE. The design, which can equalize channels with up to 20dB of loss at Nyquist, and which does not require a forwarded clock, achieves a power efficiency of 6.5pJ/b while supporting an aggregate 320Gb/s transfer rate.

- **Intel describes a 32Gb/s/lane energy-efficient scalable bi-directional serial transceiver**
- In Paper 26.2, Intel demonstrates a scalable bi-directional serial transceiver at 32Gb/s/lane with a 3-tap FFE transmitter, a CTLE equalizer, and a 6-tap DFE, in 22nm CMOS process. The transceiver has per-lane efficiency of 6.3pJ/b at 32Gb/s while equalizing 17dB of channel loss.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of complete transceivers and energy efficient equalizers at 20+Gb/s is a critical step toward enabling next-generation compute and memory solutions. Increasing achievable bandwidth density opens up new possibilities for densely interconnected systems, especially for chip-to-chip and chip-to-memory applications.

- A parallel bus of next-generation 20+Gb/s links with pJ/b efficiencies would enable terabyte per second throughputs at low power.

Session 27 Highlights:
Energy-Efficient Digital Circuits

[27.1] A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, Embedding F_{MAX} Tracking

[27.3] A 210mV 5MHz Variation-Resilient Near-Threshold JPEG Encoder in 40nm CMOS

Paper 27.1 Authors: *R. Wilson[1], E. Beigne[2], P. Flatresse[1], A. Valentian[2], F. Abouzeid[1], T. Benoist[2], C. Bernard[2], S. Bernard[2], O. Billoint[2], S. Clerc[1], B. Giraud[2], A. Grover[1], J. Le Coz[1], I. Miro-Panades[2], J.P. Noel[1], B. Pelloux-Prayer[1], P. Roche[1], O. Thomas[2], Y. Thonnart[2], D. Turgis[1], F. Clermidy[2], P. Magarshack[1]*
Paper 27.1 Affiliation: *[1]STMicroelectronics, Crolles, France; [2]CEA-LETI - MINATEC, Grenoble, France*

Paper 27.3 Authors: *N. Reynders, W. Dehaene*
Paper 27.3 Affiliation: *KU Leuven, Leuven, Belgium*

Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO,*
Energy-Efficient Digital Subcommittee

CONTEXT AND STATE OF THE ART

- Wide voltage range operation brings more versatility to achieve high energy efficiency in next-generation portable computing devices, enabling increased and scalable signal processing capabilities. However, very-low voltage operation suffers from high sensitivity to process variations, constraining application performance.

TECHNICAL HIGHLIGHTS

- **Order of magnitude speed increase in DSP processing below 0.4V.**

- In Paper 27.1, STMicroelectronics and CEA-LETI - MINATEC describe a 32b VLIW DSP fabricated in 28nm UTBB FDSOI capable of dynamically tracking the maximum frequency within 3.5% accuracy. The 1mm^2 chip achieves scalable performance and high energy efficiency in the 397mV-to-1.3V supply range, showing an operating frequency of 460MHz at the minimum 0.4V supply, and a minimum energy per operation of 62pJ at 0.46V.

- In Paper 27.3, KU Leuven describes the design of a near-threshold full JPEG encoder in a 40nm CMOS technology. The variation-resilient chip is functional down to a supply voltage of 210mV at a 5MHz clock frequency, and consumes 29pJ/pixel at the minimum-energy point at a frequency of 41MHz.

APPLICATIONS AND ECONOMIC IMPACT

- This technology is essential to enable increased signal processing capabilities in next-generation mobile devices with limited energy resources and cooling, implemented in variation-prone sub-100nm silicon technologies.

- DSPs with such remarkable energy efficiency at high operating frequencies are key to enable always-on sensing and data processing in small form factor devices, empowering tomorrow's handsets with user and context awareness.

Session 28 Highlights: Mixed-Signal Techniques for Wireless

[28.1] A Programmable 0.7-to-2.7GHz Direct ΔΣ Receiver in 40nm CMOS

Paper Authors: M. Englund[1], K. B. Östman[1], O. Viitala[1], M. Kaltiokallio[1], K. Stadius[1], K. Koli[2], J. Ryynänen[1]
Paper Affiliation: [1]Aalto University, Espoo, Finland, [2]Ericsson, Turku, Finland

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Helsinki, Finland; Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- Software-defined radios enable low-cost, flexible realization of multi-standard wireless devices.
- Advancements of semiconductor technology and mixed-signal techniques can be used to realize highly reconfigurable wireless chips.

TECHNICAL HIGHLIGHTS

- **A software-defined radio receiver illustrates the possibility of using a ΔΣ modulator for direct RF-to-digital conversion.**
- In Paper [28.1], the wideband ΔΣ-modulator-based receiver is capable of handling up to 20MHz signal bandwidth with a narrowband NF of 4.2dB.

APPLICATIONS AND ECONOMIC IMPACT

- Software-defined-radio CMOS chips reduce the time that is needed to introduce wireless devices capable of supporting new and evolving standards to the market.

Session 29 Highlight:
Data Converters for Wireline Systems

[29.3] A 14b 1GS/s RF Sampling Pipelined ADC with Background Calibration

Paper 29.3 Authors: *A. Ali, H. Dinc, P. Bhoraskar, C. Dillon, S. Puckett, B. Gray, C. Speir, J. Lanford, D. Jarman, J. Brunsilius, P. Derounian, B. Jeffries, U. Mehta, M. McShea, Ho-Young Lee*
Paper 29.3 Affiliation: *Analog Devices, Greensboro, NC*

Subcommittee Chair: *Boris Murmann, Stanford University, CA, Data Converters Subcommittee*

CONTEXT AND STATE OF THE ART

- Wireless infrastructure components, such as basestation transceivers, rely on A/D converters with very high resolution and speed. ADCs used in current basestations provide 14-to-16b of resolution and operate at 250MS/s. Future systems, such as LTE advanced are calling for faster conversion rates to improve the overall system bandwidth.

TECHNICAL HIGHLIGHTS

- **Highest speed-resolution product ADC for wireless infrastructure applications**

- In paper 29.3, Analog Devices describes a 14b 1GS/s RF sampling pipelined ADC that derives its performance from a variety of design techniques. For example, to improve the sampling linearity, it employs input distortion cancellation and digital calibration to compensate for the nonlinear charge injection from the sampling capacitors. The circuit achieves a near record-breaking combination of speed-resolution product and only 50fs sampling jitter.

APPLICATIONS AND ECONOMIC IMPACT

- This ADC will help enable the next generation of wireless basestations and related wireless infrastructure components.

Session 30 Highlights: Technologies for Next-Generation Systems

[30.1] 8b Thin-Film Microprocessor Using a Hybrid Oxide-Organic Complementary Technology with Inkjet-Printed P²ROM Memory

[30.2] Digital PWM-Driven AMOLED Display on Flex Reducing Static Power Consumption

Paper 30.1 Authors: *Kris Myny[1], Steve Smout[1], Maarten Rockelé[1,2], Ajay Bhoolokam[1,2], Tung Huei Ke[1], Soeren Steudel[1], Koji Obata[3], Marko Marinkovic[4], Duy-Vu Pham[4], Arne Hoppe[4], Aashini Gulati[5], Francisco Gonzalez Rodriguez[5], Brian Cobb[5], Gerwin H. Gelinck[5], Jan Genoe[1,2], Wim Dehaene[1,2], and Paul Heremans[1,2]*
Paper 30.1 Affiliation: *[1]imec, Leuven, Belgium [2]KULeuven, Leuven, Belgium [3]Panasonic, Osaka, Japan [4]Evonik Industries, Marl, Germany [5]Holst Centre/TNO, Eindhoven, The Netherlands*

Paper 30.2 Authors: *Jan Genoe[1,2], Koji Obata[3], Marc Ameys[1], Kris Myny[1], Tung Huei Ke[1], Manoj Nag[1], Soeren Steudel[1], Sarah Schols[1], Joris Maas[4], Ashutosh Tripathi[4], Jan-Laurens van der Steen[4], Tim Ellis[4], Gerwin H. Gelinck[4] and Paul Heremans[1,2,4]*
Paper 30.2 Affiliation: *[1]imec, Leuven, Belgium [2]KULeuven, Leuven, Belgium [3]Panasonic, Osaka, Japan [4]Holst Centre\TNO, Eindhoven, The Netherlands*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- An 8b microprocessor has previously been demonstrated in organic technology but used unipolar logic gates and a lithographically-written memory.

- Previously-reported AMOLED displays on foil consume as much power in the driver circuits as in the backplane due to the use of analog drive circuitry

TECHNICAL HIGHLIGHTS

- **The first hybrid complementary organic/oxide thin film microprocessor on foil with a print-programmable ROM:**
  A flexible 8b microprocessor on foil comprising solution-processed n-type oxide transistors and organic p-type transistors combined in a CMOS technology. The microprocessor instruction sequence is programmed by inkjet printing silver paste drops on the foil. The processor operates from a 6.5V supply and can achieve a clock speed of 2.1kHz

- **The highest reported efficiency for AMOLED displays on foil:**
  New AMOLED scan drivers are integrated with an a-IGZO backplane on flexible foil. The system enables PWM driving of the OLED pixels with a duty cycle of almost 100%. This PWM driving method enables up to 40% static power reduction of AMOLED displays.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of a microprocessor on foil with a printable instruction set illustrates the potential of organic technology to be customized for low-cost consumer applications.

- Increased efficiency for AMOLED displays will lead to longer battery life for mobile applications, while manufacture on foil leads to the possibility of unbreakable displays.

Session 30 Highlights: Technologies for Next-Generation Systems

[30.5] A GaN 3x3 Matrix Converter Chipset with Drive-by-Microwave Technologies
[30.6] An Electromagnetic Clip Connector for In-Vehicle LAN to Reduce Wire Harness Weight by 30%

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Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- A conventional matrix converter for motor drive applications requires multiple high-voltage components including photo-couplers, isolated power supplies, gate drivers, power switches and flywheel diodes. The resulting system is bulky, typically the size of a large laptop.

- In-vehicle communication between electronic control units is conventionally implemented by a wired LAN. The weight of the wire harness increases significantly as the number of control units increases, resulting in decreased fuel efficiency.

TECHNICAL HIGHLIGHTS

- **The world's smallest matrix converter motor drive system implemented using 'Drive by Microwave' GaN switches:**
  The extremely compact (19mm x 14mm) and low power (1.5W) three phase AC-AC matrix converter for motor drive incorporates GaN/Si integrated chips and isolated dividing couplers.

- **In-vehicle LAN with 30% harness weight reduction through the use of electromagnetic clips:**
  Electromagnetic couplers form contactless connections. High noise immunity is achieved by using Manchester encoding, majority-voting error correction and digital clock recovery.

APPLICATIONS AND ECONOMIC IMPACT

- Matrix converters are highly efficient but are not used in many applications due to their large size and cost. This highly-integrated converter will enable a new range of products which will benefit from a high efficiency motor drive.

- Fuel efficiency is improved by the 30% reduction in weight of the in-vehicle wired LAN. This weight reduction is comparable to that achieved by replacement of the copper core with aluminum, but at a much lower cost.

Session 30 Highlights: Technologies for Next-Generation Systems

[30.8] A 30GS/s Double-Switching Track-and-Hold Amplifier with 19dBm IIP3 in an InP BiCMOS Technology

Paper Authors: *Timothy D. Gathman[1], Kristian N. Madsen[2], James C. Li[3], Thomas C. Oh[3] and James F. Buckwalter[4]*
Paper Affiliation: *[1]Qualcomm, Technologies, Inc., San Diego, CA, USA, [2]Peregrine Semiconductor, San Diego, CA, USA, [3]HRL Laboratories, Malibu, CA, USA, [4]University of California, San Diego, CA, USA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions Subcommittee*

CONTEXT AND STATE OF THE ART

- Track-and-hold amplifiers (THA) for very high speed data converters have been implemented in III-V technologies which are not compatible with standard silicon processes, requiring two-chip solutions.

TECHNICAL HIGHLIGHTS

- The world first implementation of a track-and-hold amplifier in an InP BiCMOS process bonded to a standard CMOS wafer and clocked in excess of 10GS/s.
- A worst-case OIP3 and IIP3 of 15.6dBm and 19dBm are measured, respectively.

APPLICATIONS AND ECONOMIC IMPACT

- High-speed track-and-hold amplifier (THA) circuits are critical for high-speed, high-resolution data converters, particularly in emerging 100Gb/s optical communication systems.

ISSCC 2014
TRENDS

CONDITIONS OF PUBLICATION

PREAMBLE

The Trends document serves to capture the trends within each technology track covered by the scope of ISSCC 2014 in February in San Francisco

High resolution figures are available along with the press kit. For access please contact the press coordinator.

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- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 61st appearance of ISSCC, on February 9th to the 13th, 2014, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2014, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 9-13, 2014, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 1, 2013, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

HISTORICAL TRENDS IN TECHNICAL THEMES

Analog Systems

(Analog Subcommittee, Data Converters Subcommittee)

Analog – 2014 Trends

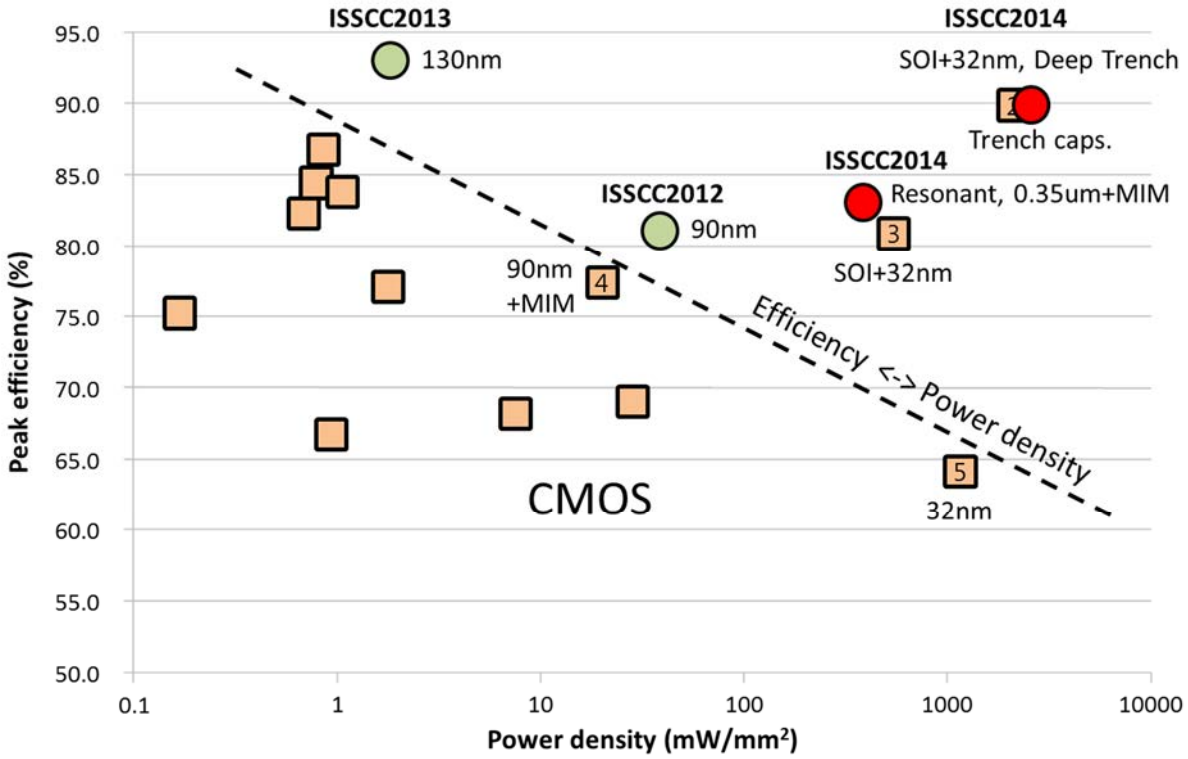
SC Power Converters

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy must fundamentally be performed with analog systems. As a result, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: Increased efficiency in wireless power transmission is enabling faster charging over longer distances. There is also an explosion of technologies that permit energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from energy sources at tens of millivolts, to provide autonomy for remote sensors or to supplement conventional battery supplies in mobile devices. To achieve this, extremely low power must be consumed by the attendant analog circuits so that some energy is left over to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will permit devices to be powered indefinitely from sustainable sources, opening the door to ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like the bridges in our roads, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, digital circuits such as microprocessors drive the market; thus, semiconductor technology has been optimized relentlessly over the past 40 years to reduce the size, cost, and power consumption of digital circuits. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle has decreased, and the variation observed in their analog performance has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in our most modern digital semiconductor technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are captured by movement towards the top-right in the plot below.



Comparison of Integrated Switched-Capacitor Power Converters showing Peak Efficiency vs Power Density. Recent advances achieve much higher power density without sacrificing efficiency (see the top right quadrant).

Data Converters – 2014 Trends

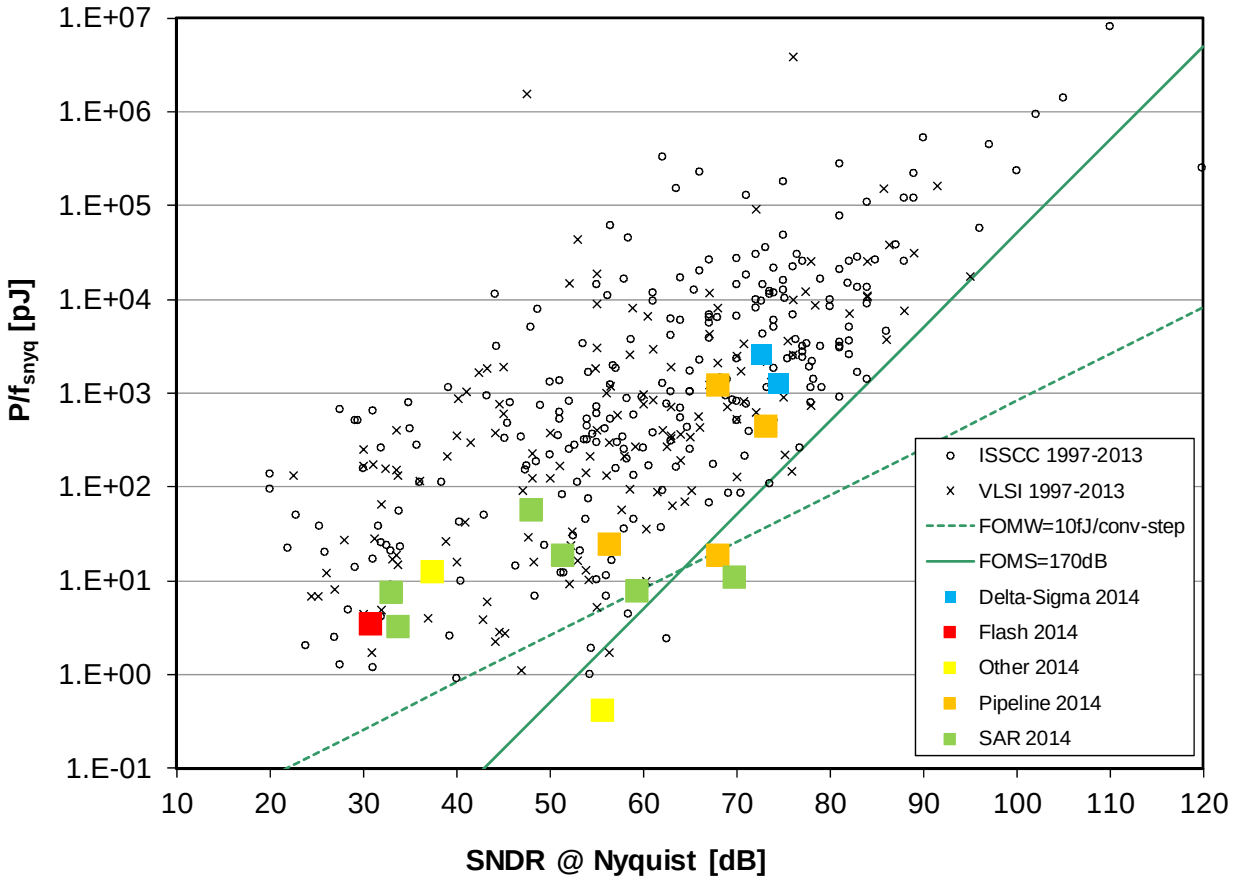
Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA*

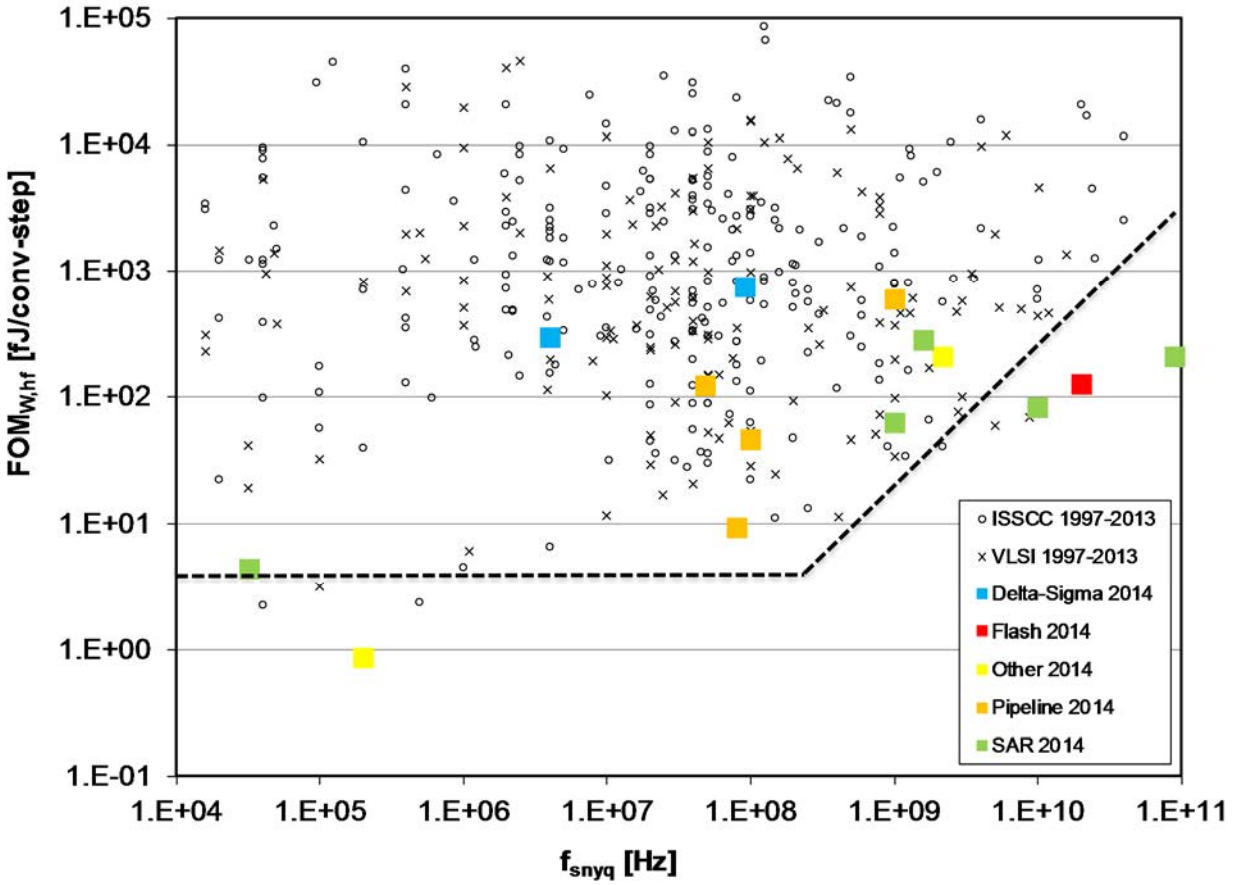
Data converters serve as key building blocks in virtually all electronic systems, and serve to bridge the analog physical world to the digital circuitry prevalent in modern integrated circuits. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be the dominant drivers for innovation, as evidenced by the data converters presented at ISSCC 2014.

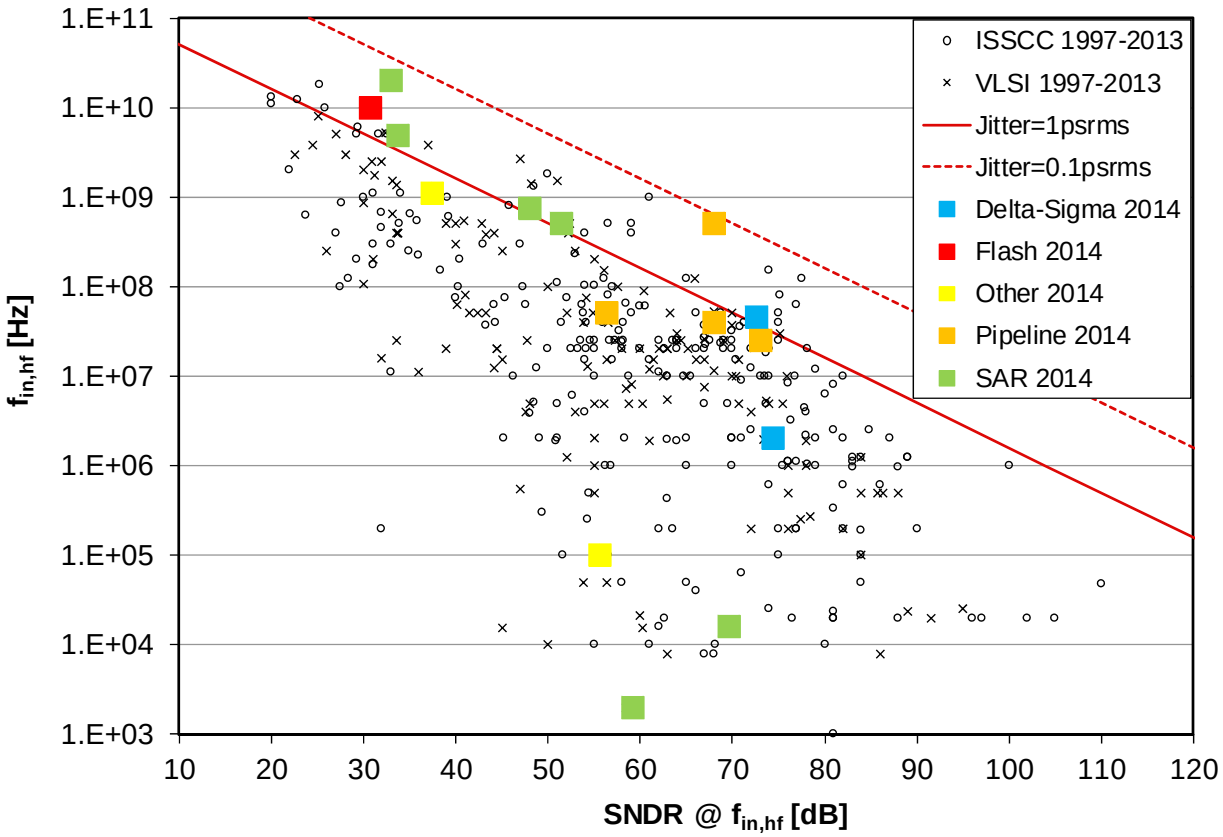
The first figure below is a survey of ADC power efficiency expressed as power dissipated relative to the effective Nyquist rate (P/f_{snyq}), and as a function of signal-to-noise and distortion ratio (SNDR). For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; the efficiency of this operation can be measured as the energy consumed per conversion step. The dashed trend-line represents a benchmark of 10fJ/conversion-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of signal-to-noise ratio shown by the solid line. Contributions at ISSCC 2014 are indicated by the colored dots representing various converter architectures with contributions from previous years denoted by smaller dots. (Note that a lower P/f_{snyq} metric represents a more efficient circuit.) Several new SAR-based converters at various SNDR design points continue to push the limits of energy efficiency.

The second figure shows energy per conversion step vs. the Nyquist sampling rate. This figure elucidates the difficulty of maintaining good efficiency at higher speeds of operation. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the entire spectrum of conversion rates. Most notably, we are seeing for the first time converters with good efficiency at speeds of several tens of gigasamples per second.

The final chart plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2014, we see many examples setting a new standard in this metric utilizing several different converter architectures.







HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

(RF SUBCOMMITTEE, WIRELESS SUBCOMMITTEE, WIRELINE SUBCOMMITTEE)

RF Subcommittee – 2014 Trends

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France*

Introduction:

This year, ISSCC 2014 will show increased innovation, integration, and technical maturity across the RF frequency bands from a few GHz to above 500GHz. In addition, 28nm CMOS technology is being adopted for the first time to wireless transceivers. This exposition outlines the emerging RF trends that will be displayed at ISSCC 2014: the drive toward increasing levels of integration will be presented. This trend can be seen in all areas of RF design, from cellular and wireless sensors to mm-Wave and imaging.

In cellular applications, efforts continue to increase the efficiency of integrated transmitters and PAs, moving towards multipath solutions, such as Doherty or Envelope Elimination and Restoration topologies. In addition to that, the power transfer to the antenna is maximized through closed-loop architectures that detect the effective RMS output-power transmitted, or allow tunable matching with the antenna. On the receiver side, the **multipath approach,** a well-established strategy to reduce noise of the input termination (using a noise cancelling topology), is appearing in the design of beam-forming and blocker-tolerant receivers, defining a new path towards the next generation of multi-standard transceivers.

The frequency synthesizer is still one of the most power-hungry elements in the entire transceiver; besides the continuing attempt to reach the best power efficiency, **mitigation of frequency pulling** and coexistence of multiple local oscillators are emerging as key aspects for the next generation of carrier aggregation systems. As well, **Multiplying Delay Locked Loops (MDLLs)** are becoming popular in wireless applications in the attempt to replace the large PLLs based on LC-tank oscillators. This year, at ISSCC 2014, for the first time, a fractional MDLL will be presented showing performance in terms of phase-noise comparable to the state-of-the-art traditional PLL-based approaches.

In mm-Wave designs, now that complete systems can be easily integrated, **the frequency of operation is moving rapidly towards THz**, where imaging applications are waiting for fully integrated solutions. 65nm CMOS is establishing itself as the most used technology for RF even above 100GHz, where, however, several designs still use SiGe for its higher f_t, f_{max},and breakdown voltage. Overall, solutions presented at ISSCC 2014 confirm that RF devices will continue to see larger levels of integration at the chip and package level for years to come. Over the past decade, the papers submitted to ISSCC have indicated clear trends in the continuing push to higher frequencies of operation in CMOS and BiCMOS. Thus, this year, the psychological barrier of 0.5THz has been overcome, looking towards THz applications! With the consolidation of mm-Wave designs, multipath solutions are emerging above 100GHz with phase array designs that take advantage of shorter wavelengths for compact single-chip solutions.

These trends are exemplified by presentations at ISSCC 2014 as described below:

Complexity and Maturity in the mm-Wave and sub-mm-Wave Ranges:

The high cutoff frequency of bipolar transistors and highly downscaled MOS transistors enables the realization of circuits and systems operating in the mm-Wave range. In the past few years, high-data-rate communication in the 60GHz band and automotive radar around 77GHz have garnered much attention. The 100GHz barrier for the operating frequency of silicon circuits was broken a few years ago. Whereas initially elementary building blocks like a VCO and an amplifier operating above 100GHz have been realized, we now witness the trend of increasing complexity in circuits operating above 100GHz, aiming at imaging and spectroscopy.

While the integration level in these domains is high, we see an improvement in the performance of individual building blocks: the output power of mm-Wave and sub-mm-Wave sources and PAs increases, (see Figures) and VCOs are operating at ever-increasing frequencies with a higher tuning range. This year, PAs are especially designed to minimize AM-PM distortion, and to be compliant with wideband modulations. In addition, the frequency of operation has increased above 300GHz while maintaining efficiency and output power comparable with the state-of-the-art.

Co-Existence and Efficiency for Cellular Applications:

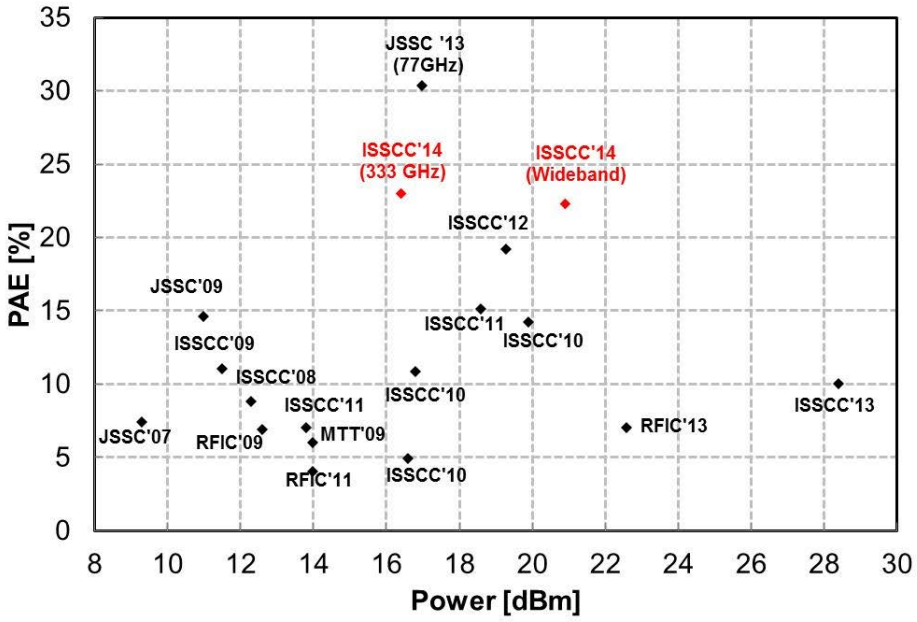
Recevier Linearization: In the past few years there has been increasing interest in techniques to improve the linearity of receivers. Improved linearity will ease the requirements on the RF filtering of out-of-band blockers which can then be accomplished by adopting frequency-translated BPF and noise cancelling techniques.

Efficiency: At ISSCC 2014, PA efficiency improvements demonstrated will directly impact the battery life in portable applications. These techniques include antenna tuning, envelope elimination and restoration. and the Doherty architecture.

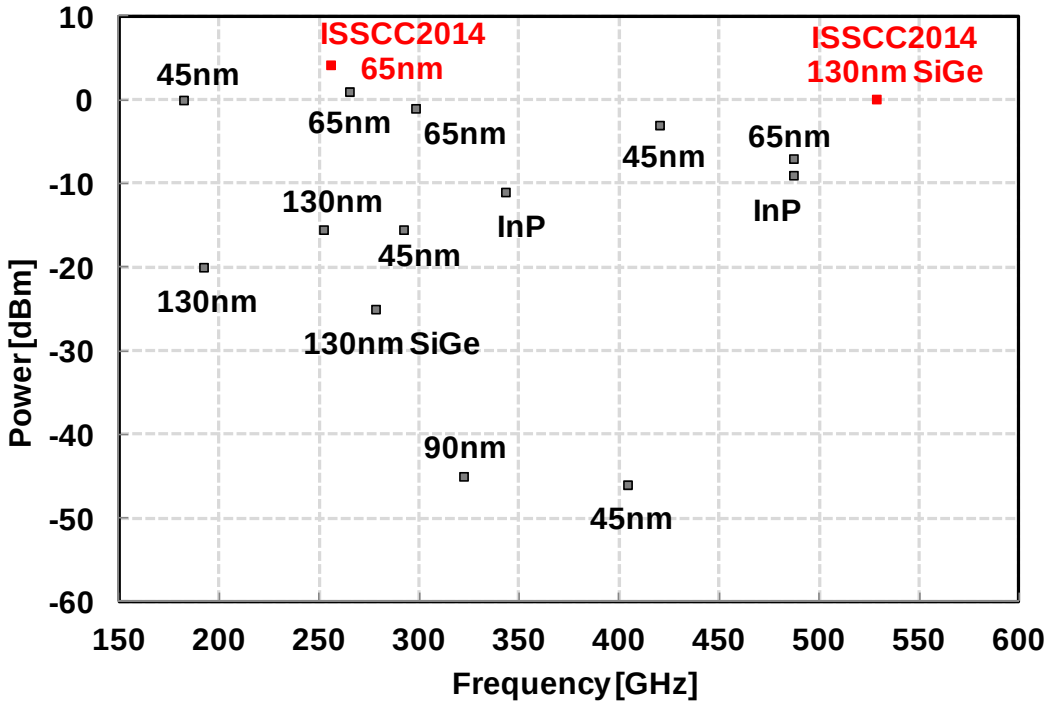
Digitally-Assisted RF: The trend towards digitally-assisted RF continues and is increasingly applied in mm-Wave chips. Such calibration techniques are being demonstrated in order to improve the overall performance of the transceiver by reducing the impact of analog impairments at the system level. This year, a new concept for improving the problematic VCO pulling effect will be presented.

VCOs: Without degredation of the phase-noise figure-of-merit (FOM), several techniques have been introduced to achieve wideband tuning in a compact area, and to overcome the problems of frequency pulling. The next Figure shows trends in VCO performance for some of the most significant VCOs published in the past decade.

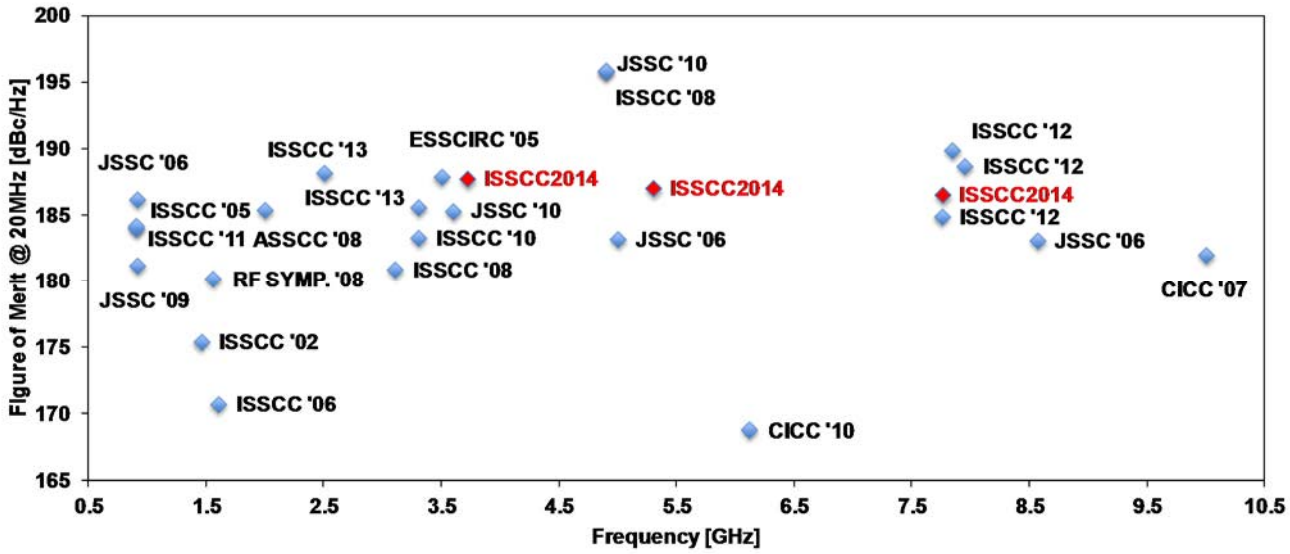
PLLs: New architectures have been proposed to improve PLL performance. These techniques include divider-less PLLs, sub-sampling Fractional PLLs, MDLLs, and direct-digital frequency synthesizers.



PAE (%) vs. output power for recent submicron mm-Wave CMOS PAs
The circuits to be revealed at ISSCC 2014 operate at very high frequency and/or are wideband compared to previous designs.



Output power versus frequency for mm-Wave and sub-mm-Wave sources.
Record output power levels are being revealed at ISSCC 2014.



Phase-noise FOM at 20MHz offset frequency versus oscillation frequency. While conventional FOMs remain at competitive levels, the circuits revealed at ISSCC 2014 are digitally assisted to reduce the impact of analog impairment effects on performance.

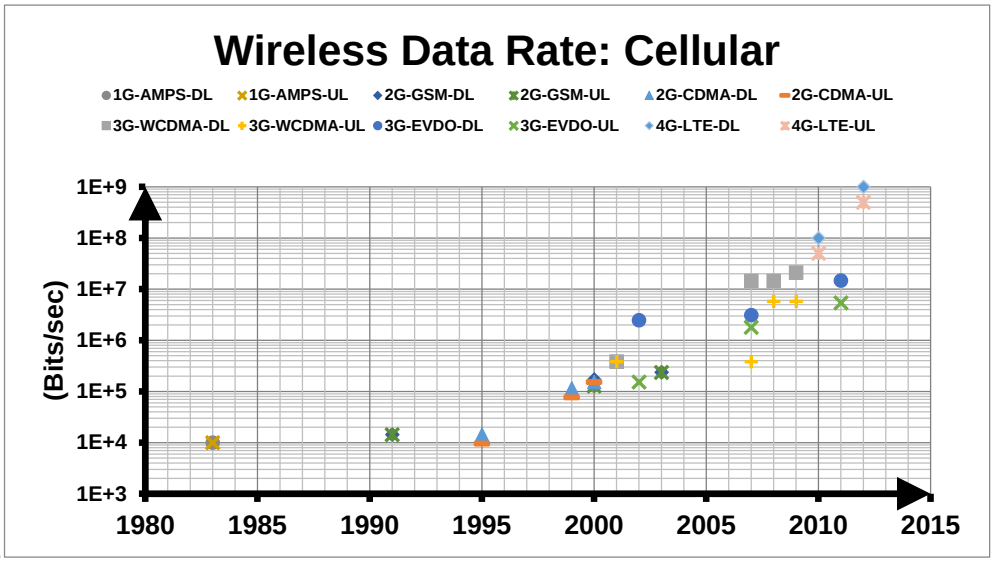
Wireless – 2014 Trends

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Finland*

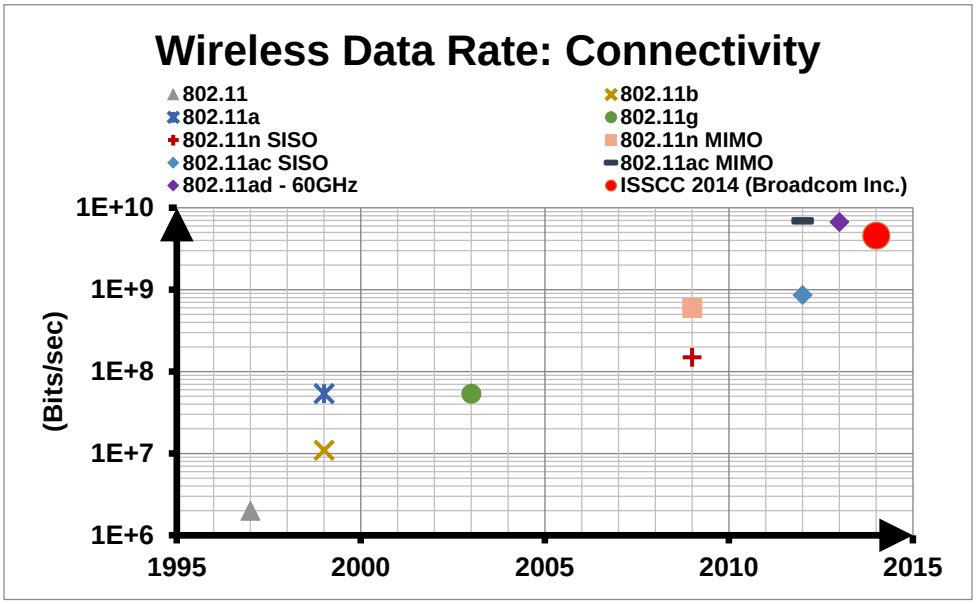
The exponential increase of data-rate of cellular devices is a major driver of new wireless standards as reflected in the first Figure. The latest generation of cellular wireless standards, such as Long Term Evolution (LTE), includes multiple frequency bands, a wide range of channel bandwidths, and variousduplexing and diversity schemes, as well as new features, such as carrier aggregation. Fundamental trade-offs in data-rate, power consumption, functionality, and cost, continue to drive research and innovation. Despite the added complexity, the power consumption of cellular transceivers continues to improve thanks to semiconductor technology scaling and the exploitation of techniques, such as envelope tracking in the transmitter. Circuit innovations in various aspects such as highly-linear receiver front-ends and digital calibration enable inclusion of more features in a compact complex multi-function System-on-a-Chip (SoC).

The exponential increase in data-rate is also evident in wireless connectivity devices, including Wireless Local Area Networks (WLAN), as shown by the maximum achievable data rates of wireless-connectivity standards in the next Figure . The latest WLAN SoCs in the traditional 2.4/5GHz frequency bands achieve over 1Gb/s data-rate due to increased channel bandwidth, complex modulation formats, and larger numbers of antenna elements, in a Multi-Input-Multi-Output (MIMO) configuration. Wireless connectivity at a higher carrier frequency of 60GHz enables even higher data rates, thanks to larger available bandwidth. The mm-wavelength of these signals enables compact realization of phased arrays, leading to more robust and high-data-rate wireless links. At ISSCC 2014, with a 60GHz carrier frequency, commercial CMOS chipsets achieve 4.6Gb/s over 10m links, while CMOS front-end solutions reach 28Gb/s for proximity wireless communications.

A major vision for the future of electronics includes Wireless Sensor Networks (WSN) and the Internet-of-Things (IoT), where ubiquitous devices and sensors are embedded in, and harvest energy from, the environment, while staying connected through low-power low-cost short-range wireless. An intriguing application is the Body Area Network (BAN,) where a wirelessly-connected network of sensor nodes spread over the body, monitors human health. While early implementations of such radios used proprietary protocols, many newer implementations apply standards such as Zigbee and IEEE 802.15.6. The key challenge in these low-power radios is maintaining low energy consumption while preserving robustness to environmental change, especially due to the presence of other wireless signals.



Data Rate of Cellular Standards



Data Rate of Wireless Connectivity Standards (802.11x). Here, the red dot represents a state-of-the-art circuit, to be described at ISSCC 2014.

Subcommittee Wireline – 2014 Trends

Subcommittee Chair: *Daniel Friedman, IBM T.J. Watson Research, Yorktown Heights, NY*

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2× to 3× every 2 years. Demand for bandwidth is driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth is enabled by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data-rate. The first Figure shows that per-pin data-rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Keeping pace with these standards, the second Figure shows data-rates for published transceivers enabled in part by process-technology scaling. However, continuing with this rather amazing trend for I/O scaling will require more than just transistor size reduction: Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems.

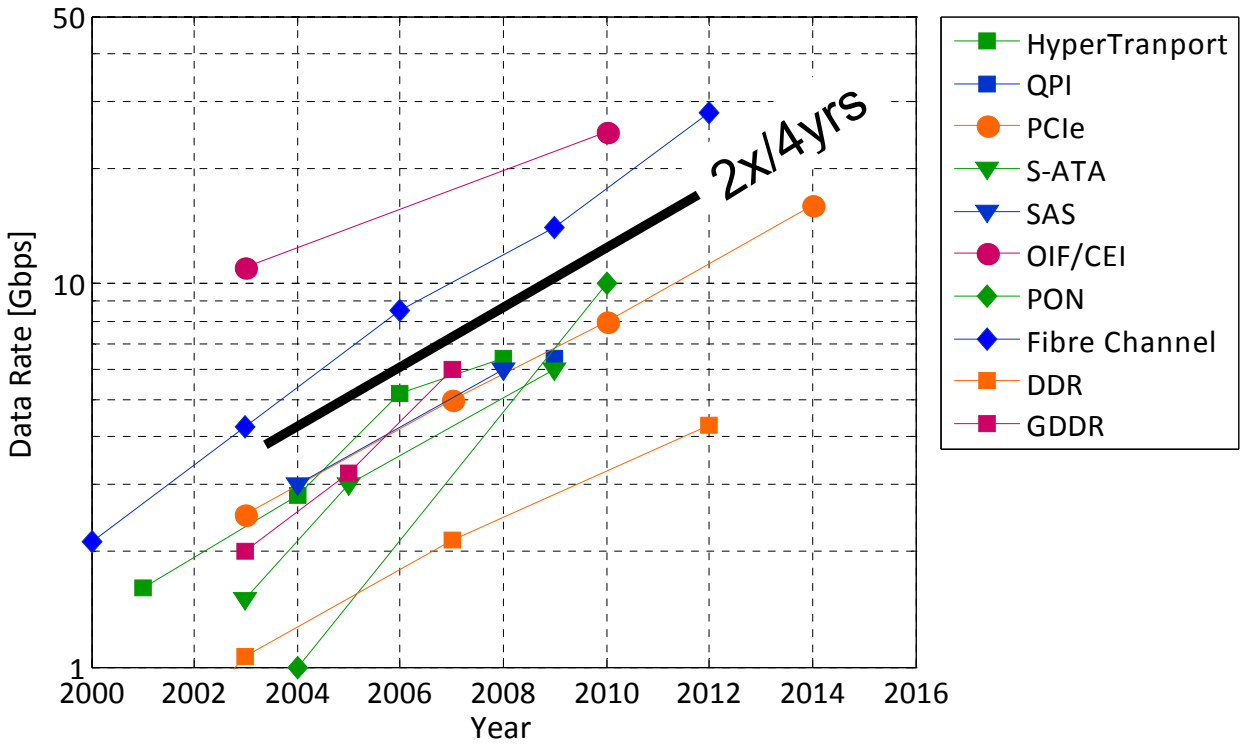
Energy Efficiency and Interconnect Density:
Power consumption for I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data-rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data-rates, and offers some energy-efficiency improvement, especially for digital components. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. This year, ISSCC 2014 includes the lowest-reported long-range 28Gb/s transceiver, achieving 20pJ/b [2.1], and 2 DFE receivers operating at 0.25pJ/b [2.4, 2.5].

Simply increasing per-pin data-rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. The third Figure shows the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss, for recently reported transceivers. The data indicate that the scaling factor between link power and signaling loss is approximately unity. In other words, the required link power approximately doubles with every additional 6dB of channel loss. At ISSCC 2014, a new coded signaling scheme is presented that transmits 8 bits over 8 wires enabling 96Gb/s at 4.3pJ/b/wire over 15dB loss channels [26.3]. As a result, the pin efficiency is doubled, making the approach suitable for pin-constrained systems such as memory interfaces. In an alternative approach [26.2], the combined optimization of channel and connector, a scalable bi-directional serial transceiver at 32Gb/s/lane achieves an efficiency of 6.3pJ/b while equalizing 17dB channel loss.

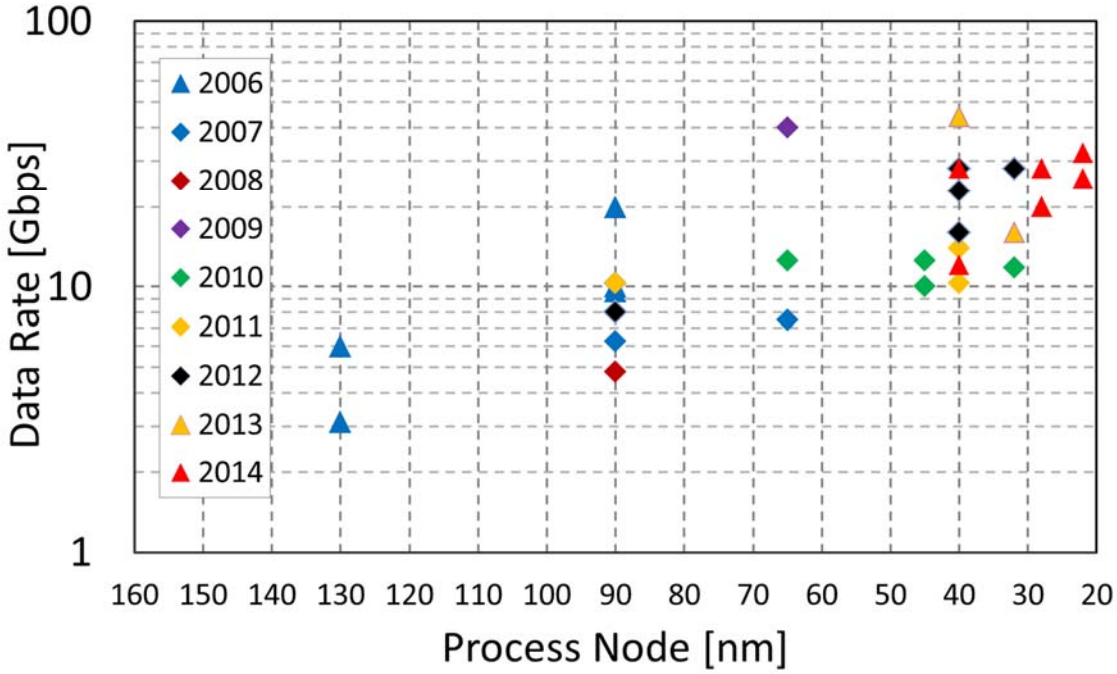
Electrical Interconnect:
Some types of channels, especially those related to medium-distance electrical I/O such as in server backplanes, must support high data-rates over high-loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent transceivers achieve data-rates above 20Gb/s with channels that have 30dB or more loss. This year, ISSCC 2014 includes a 28Gb/s transceiver operating over a 30dB-loss channel, as well as a paper that demonstrates a 60Gb/s transmitter — the highest transmit data-rate reported to date. As well, ISSCC 2014 includes one of the fastest aggregate links presented to date, specifically, 320Gb/s (20Gb/s × 16) [26.1].

Optical Interconnect:
As the bandwidth demand for traditionally electrical wireline interconnects has accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communication offers clear benefits for high-speed and long-distance interconnects. Relative to electrical interconnects, optics provides lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical with extremely low power. This trend has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. ISSCC 2014 includes a 2-dimensional (12×5) optical array achieving an aggregate data-rate of 600Gb/s [8.2]. Pre-emphasis using group-delay filtering extends the useful date rate of a 25Gb/s VCSEL to 40Gb/s [8.9]. Additional examples of low-power-linear and non-linear equalizers tackle electronic dispersion compensation in multi-mode and long-haul cables [8.1, 8.3].

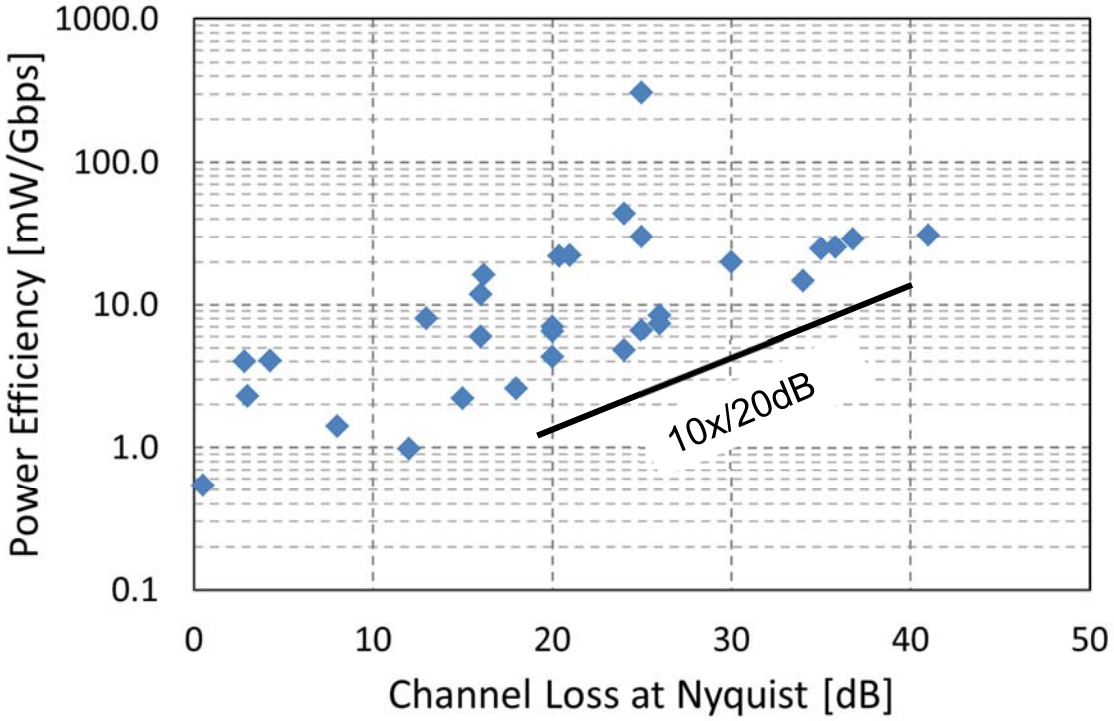
Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2014.



Per-pin data-rate vs. year for a variety of common I/O standards.



Data-rate vs. process node and year.



Transceiver Power Efficiency vs. Channel Loss.

HISTORICAL TRENDS IN TECHNICAL THEMES

Digital Systems

(Energy-Efficient Digital Subcommittee
High-Performance Digital Subcommittee
Memory Subcommittee)

Energy Efficient Digital – 2014 Trends

Subommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO*

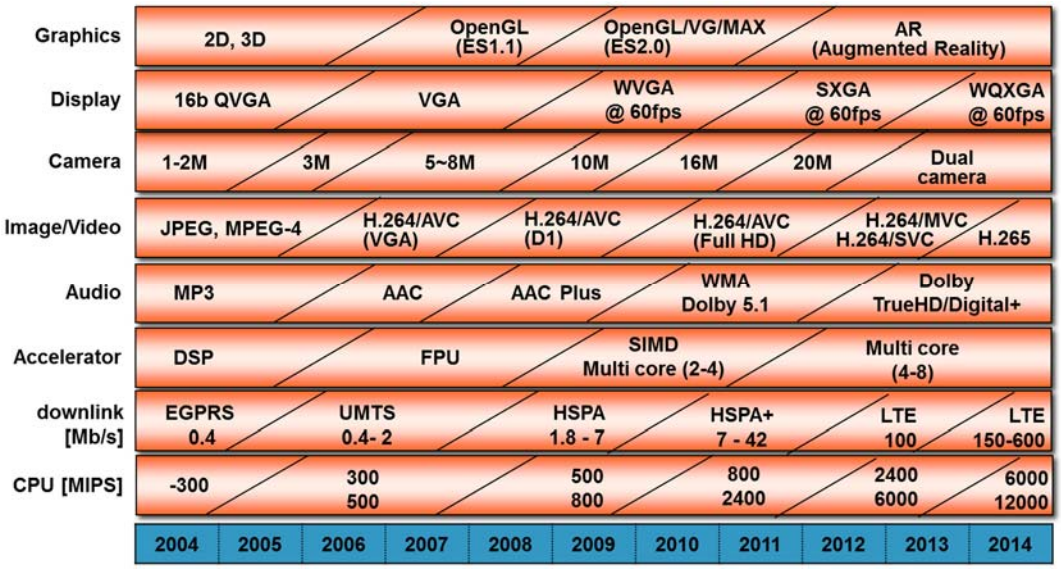
The demand for ubiquitous mobile functionality to achieve enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive innovation in systems-on-chip, while also improving battery life and lowering cost. While the performance of embedded processors has increased to meet the rising demands of general-purpose computing, dedicated multimedia accelerators are necessary to provide dramatic improvements in performance and energy efficiency of emerging applications. At the other end of the spectrum, sensor nodes for the Internet-of-Things require low-energy wireless and computational capabilities.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as lowering the area required to implement specific functions. Processors unveiled at ISSCC 2014 are built in a variety of technologies, with best-in-class results accomplished with higher integration, and improved performance-per-watt. These are demonstrated in various processes ranging from 90nm down to 28nm bulk, and SOI CMOS technologies.

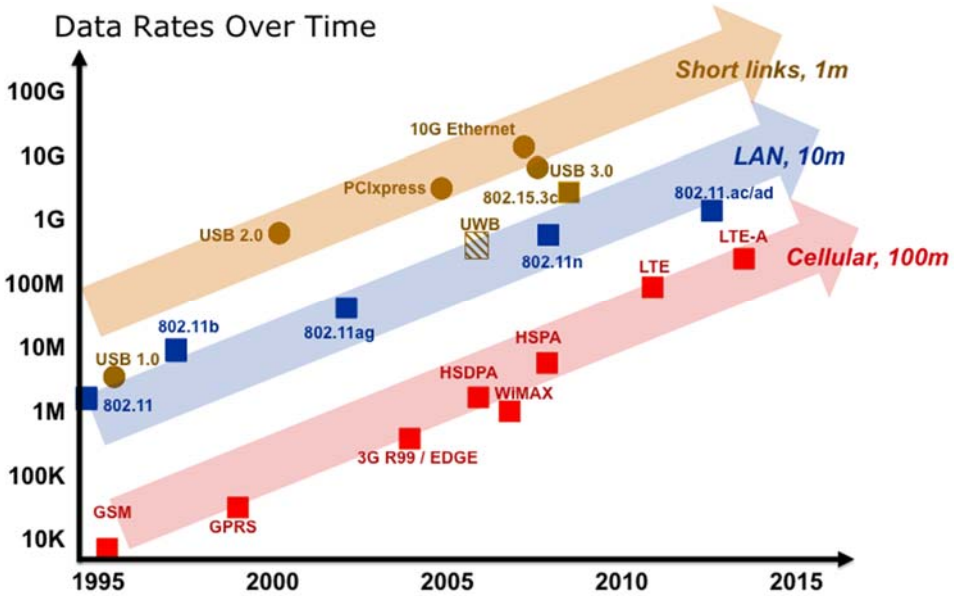
Adaptive, near-threshold operation paves the road to further supply voltage reduction. A clock frequency of 460MHz for DSP processing is now possible at a supply voltage of 400mV, with a processor implemented in 28nm UTBB FDSOI. This supply voltage will further decrease in the near future thanks to advanced technology development and novel circuit techniques that compensate for process variations. Explicit trends in voltage and frequency are difficult to quantify because of the variety of applications that are addressed. Consequently, the operations performed by the different systems are not directly comparable in terms of energy or clock frequency.

The first Figure illustrates the major trends in smartphones and tablets relevant to energy-efficient digital circuits. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300MHz in the early 2000s, there has been a sudden spurt towards 1GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and recent smartphones incorporate four- and even eight-core processors, running up to 2GHz. Battery capacity, mostly driven by the required form factor, as well as thermal limits, implies a power budget of roughly 3W for a smartphone (including the power amplifier for cellular communications and the display). The available power budget for everything digital has been holding steady in the range of 2W (peak) to 1W (sustained). As a result, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth). For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, augmented reality. and computational imaging, to name a few. For all digital circuits, the limited power budget leads to more fine-grained clock gating, various forms of adaptive voltage-frequency scaling, variable device threshold-schemes, and elaborate power and thermal management.

The second Figure shows the evolution of bit-rates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links, consistently show a 10× increase in data-rate every five years, with no sign of abatement. With essentially-constant power and thermal budgets, energy efficiency has become a central theme in designing digital circuits for mobile processing. Historically, CMOS feature sizes have halved every five years. For a brief period in the 1990s, CMOS scaling (a.k.a. Dennard scaling) provided a 2^3 (α^{-3}) increase in energy efficiency every five years, almost matching the required 10×. During the past decade, however, CMOS scaling offers a roughly 3× improvement in energy efficiency every five years. The resulting ever-widening gap has spawned alternative approaches to improving energy efficiency, namely, new standards, smarter algorithms, more-efficient digital signal processors, highly-optimized accelerators, smarter hardware-software partitioning, as well as the power management techniques mentioned above.



Application processor trends in smart phones.



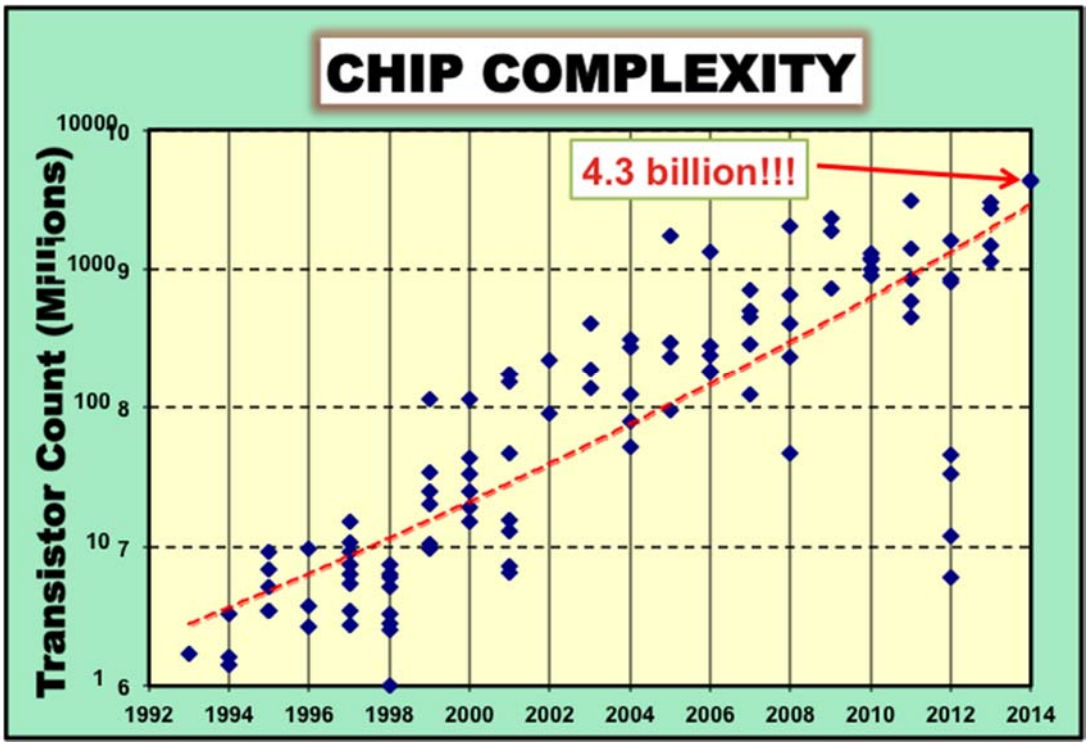
Wireless and wired data-rates over time.

High-Performance Digital – 2014 Trends

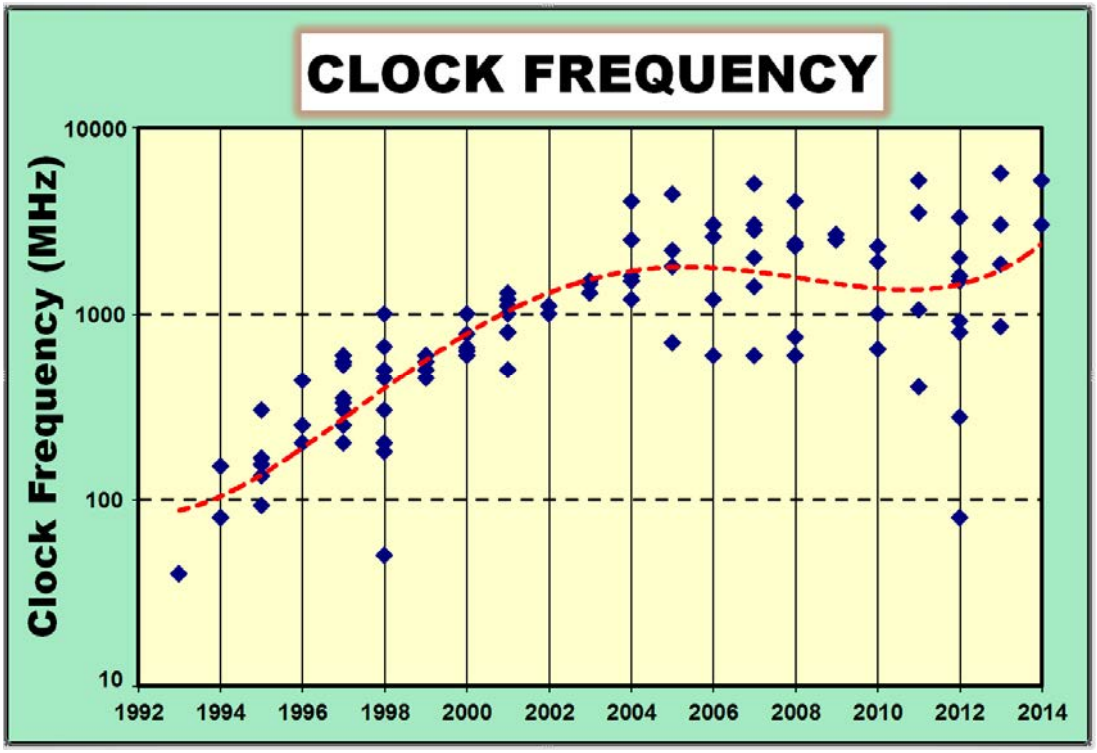
Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA*

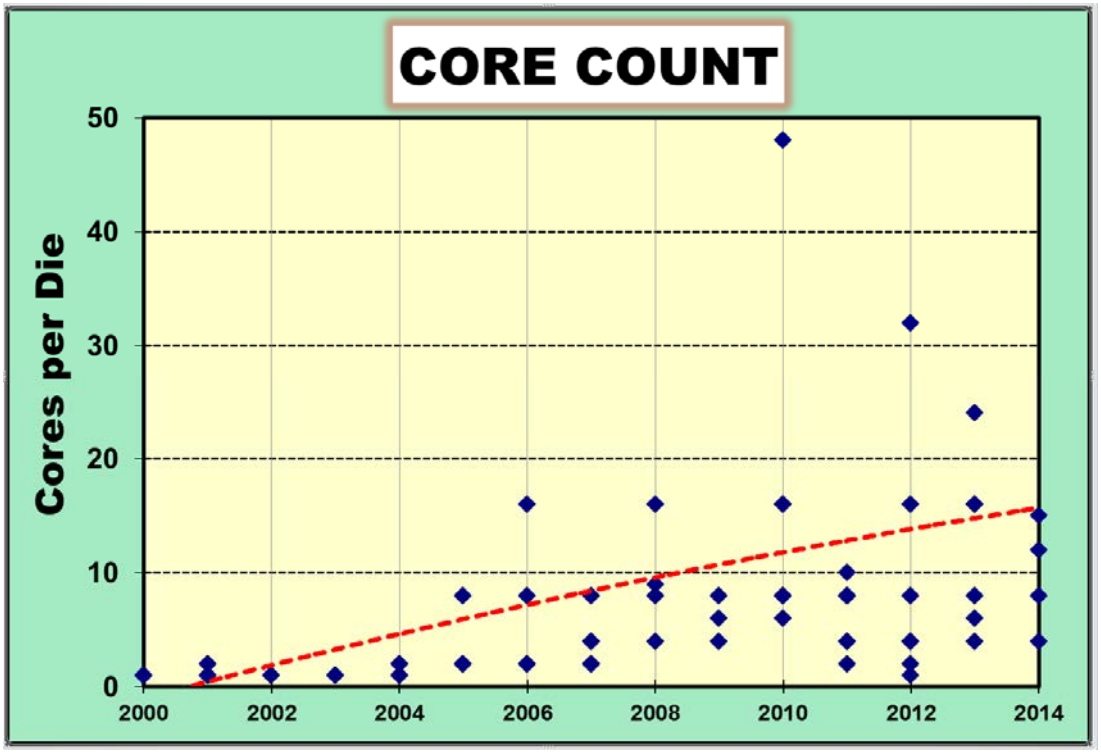
The relentless march of process technology brings increasing integration and energy-efficient performance to enterprise and cloud servers. ISSCC 2014 features IBM's 12-core, 96-thread POWER8™ processor in 22nm SOI, with 96MB of eDRAM shared L3 cache, all employing 4.2B transistors, and offering up to 2.5× higher socket performance over its 32nm POWER7+™ predecessor . Intel's 15-core, 30-thread next-generation Xeon® server processor in 22nm tri-gate technology with 37.5MB shared SRAM L3 cache integrates 4.31B transistors. Intel's Haswell processor in a 22nm tri-gate process introduces a 128MB multichip package eDRAM L4 cache to boost integrated graphics performance.

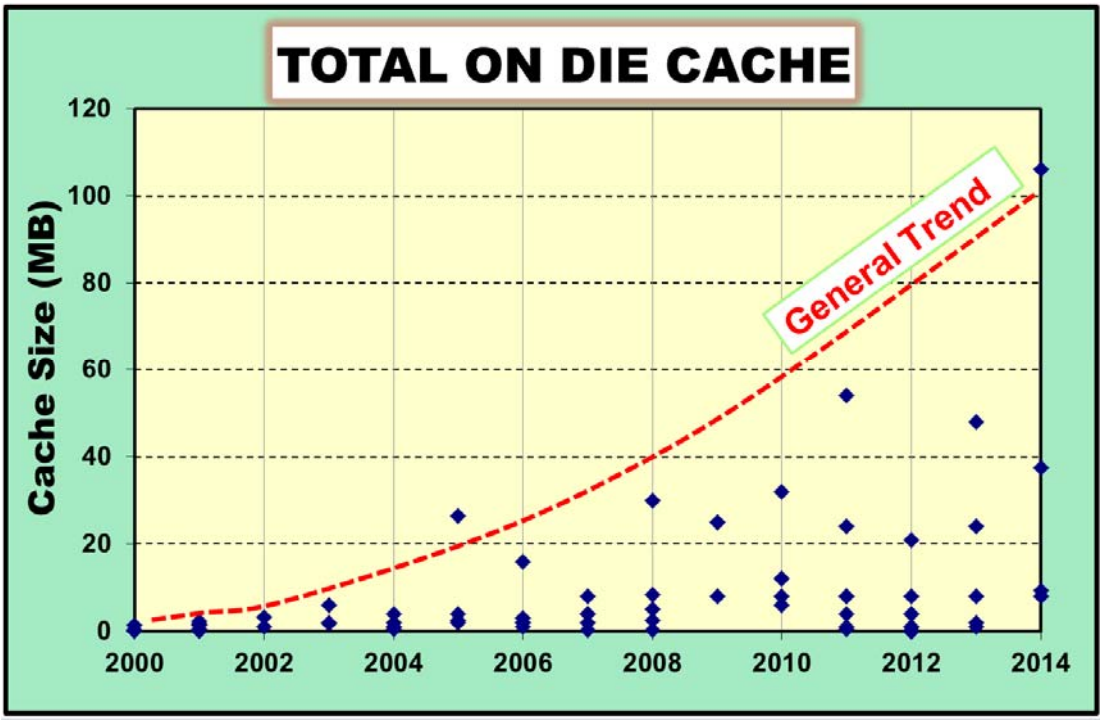
The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration threshold was achieved some years ago, we now commonly see processors incorporating more than 4B transistors on a die.



The maximum core clock frequency seems to have saturated in the range of 5 to 6GHz, primarily limited by thermal considerations. Thus, the IBM POWER8™ processor core reports a nominal 5GHz+ operation. The energy-efficient 64b ARM v8 processor for micro-servers operates nominally at 3GHz in 40nm bulk CMOS.

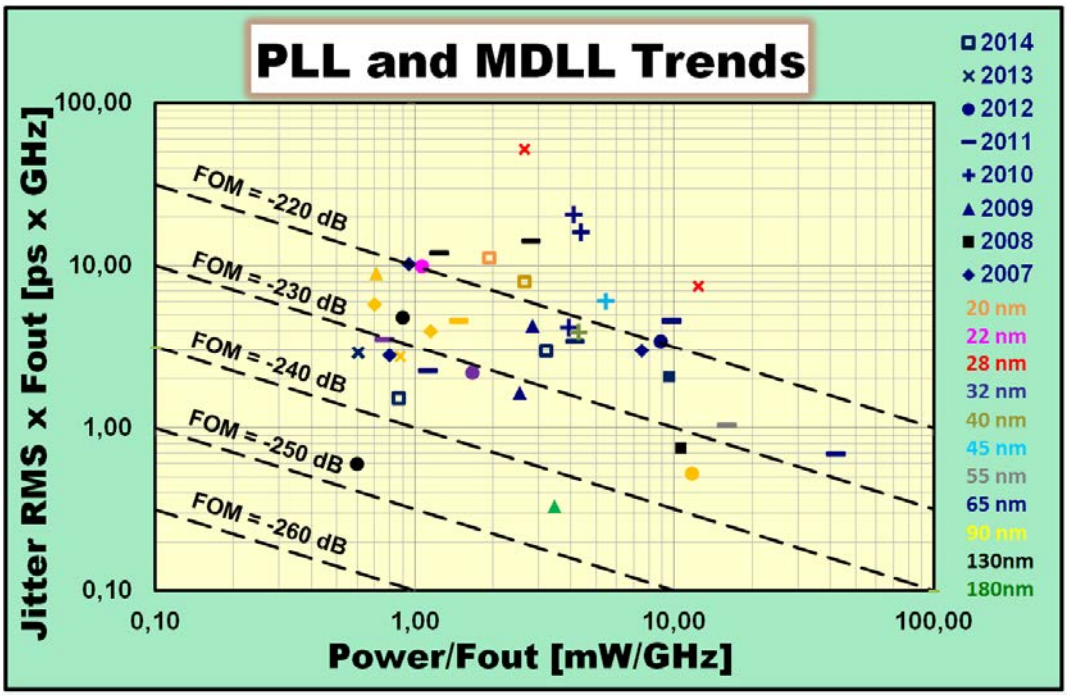






This year, there is renewed focus on improving overall energy efficiency of integrated systems-on-chip via use of more independently controlled voltage and clock domains using smart on-die control. IBM uses many integrated micro-linear regulators on die in the POWER8™, and Intel demonstrates fully-integrated buck voltage regulators on the Haswell. Adaptive clocking is used in IBM's POWER8™, and in AMD's Steamroller chips to reduce the impact of process-voltage-temperature (PVT) variation on energy efficiency and performance. Resonant clocking that also supports dynamic voltage-frequency scaling (DVFS) is used in both of the chips to reduce clock-grid power.

Another trend evident this year is the continued emergence of digital phase-locked loops (PLL) and delay-locked loops (DLL) to better exploit nanometer feature-size scaling, and reduce power and area. Through use of highly innovative architectural and circuit design techniques, the features of these digital PLLs and DLLs have improved significantly over the recent past: The diagram below shows the jitter performance vs. energy cost for PLLs and multiplying DLLs (MDLL).



Overall, digital processors continue to grow in complexity, with additional focus on integrated fine-grain power management for better energy efficiency. We observe that traditional analog building blocks are being implemented using digital techniques to cope with variability and ease scaling to finer geometries.

MEMORY – 2014 Trends

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR*

In memory systems, we continue to see progressive scaling in embedded SRAM, DRAM, and floating-gate-based Flash for very broad applications. However, with ever-increasing scaling challenges in all mainstream memory technologies, smart design algorithms and error-correction techniques are widely adopted to compensate growing device variability. FinFET technology is quickly becoming the mainstream logic technology to provide SRAM scaling, along with various read- and write-assist circuits in 22nm and beyond. Emerging memory technologies continue to make steady progress towards product intercepts, including PCRAM and ReRAM, while STT-MRAM is beginning to become a strong candidate for both stand alone and embedded applications.

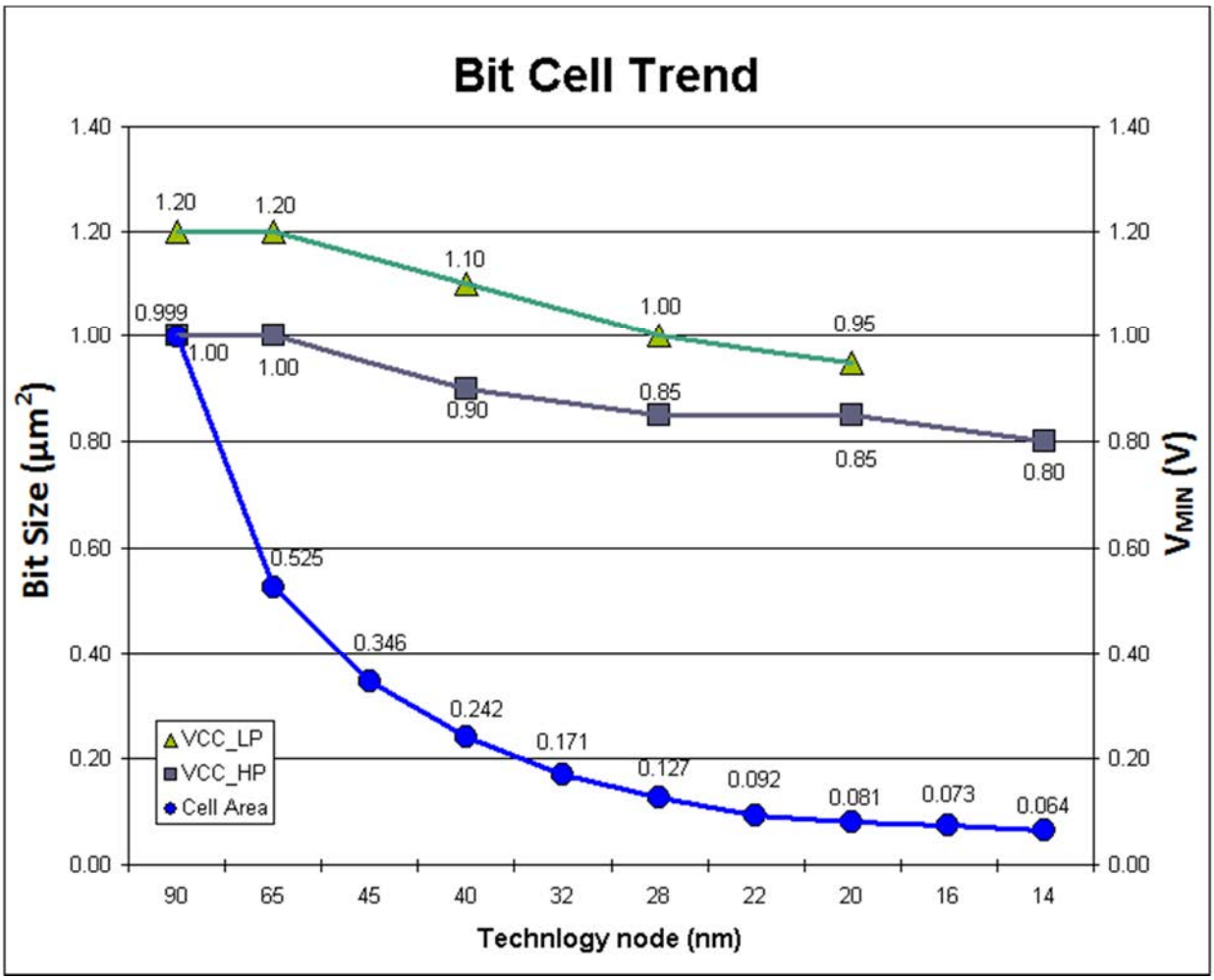
Some state-of-the-art developments from ISSCC 2014 include:

- A 1Gb eDRAM using a 22nm tri-gate logic process and capable of being clocked at 2GHz
- A 128Gb 2 bit-per-cell NAND-Flash design using 3-dimensional cell technology with 24-WL stacked layers
- A 128Gb 2 bit-per-cell NAND-Flash design using 16nm planar cell technology
- A 128Mb SRAM designed in 14nm FinFet CMOS using a 6T bitcell with V_{min}-enhancement techniques
- An embedded ReRAM in 28nm capable of working down to 270mV
- A 1Gb 8 Channel 128GB/s High-Bandwidth Memory(HBM) DRAM
- A 3.2Gb/s/pin 8Gb 1.0V LPDDR4 SDRAM with integrated ECC engine

SRAM:

Embedded SRAM continues to be a critical technology enabler for a wide range of applications from high-performance computing and graphics to mobile applications. Challenges for SRAM include V_{min}, leakage and dynamic power reduction, while relentlessly following Moore's law to shrink the area by 0.5× for every generation of technology. As the transistor feature size diminishes below 20nm, device variation has made it very difficult to shrink the bit-cell size at the 50% rate while maintaining or lowering V_{min} between generations. Introduction of high-κ metal-gate (at 45nm) and FinFET or fully-depleted SOI transistors (at 22nm) reduces the V_{th} mismatch and have enabled further device scaling. This year, eDRAM is introduced at 22nm as a means for memory scaling in high-performance CPU designs. Design solutions such as read-/write-assist circuitry and variation-tolerant sensing schemes have been used to improve SRAM V_{min} performance starting at 32nm, and are now ubiquitous in SRAM designs below 20nm. Dual-rail SRAM design emerges as an effective solution to enable dynamic voltage-frequency scaling (DVFS) by decoupling logic supply rails from SRAM arrays, and thus allowing a much wider operating window. The use of assist-circuit techniques, FinFET transistors, and dual-rail architectures has extended the viability of using the high-density 6T SRAM bitcell down to 16nm/14nm designs.

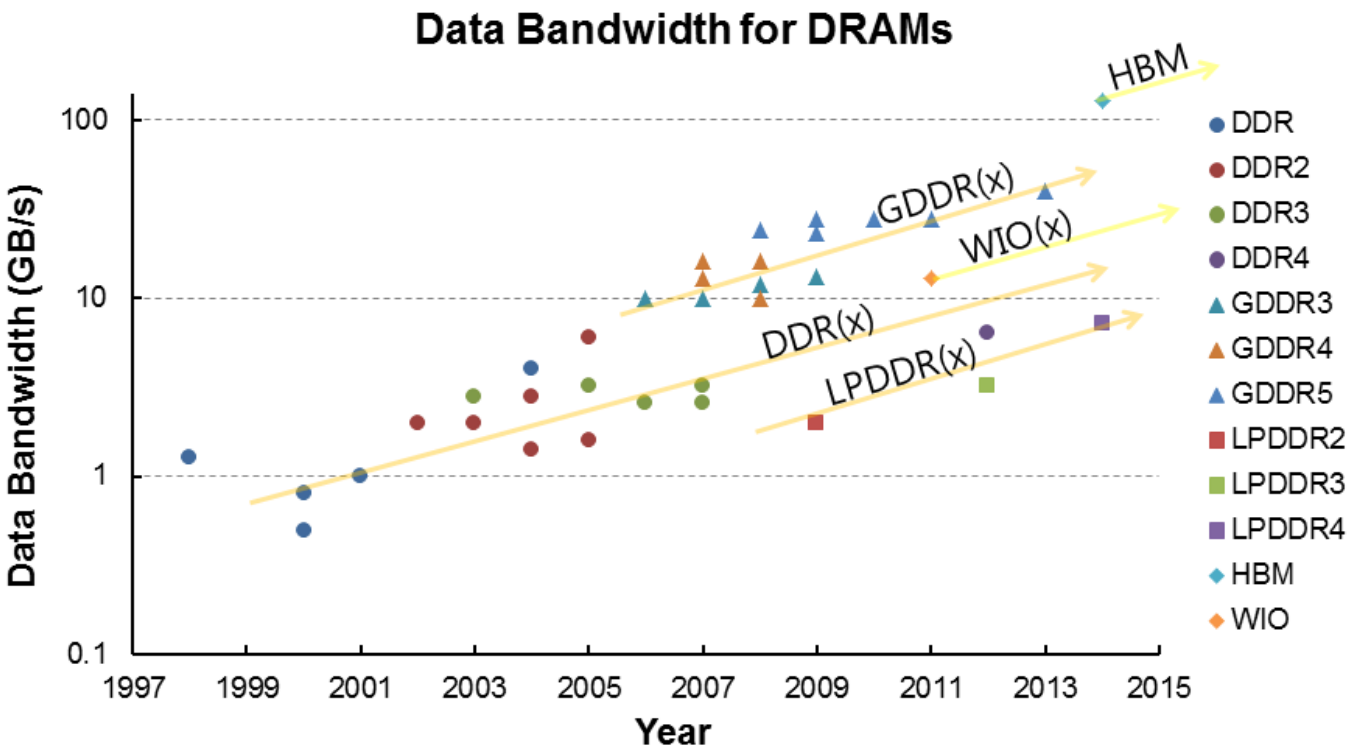
It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope at the next technology node. Sleep transistors, fine-grain clock gating, and clock-less SRAM designs have been proposed to reduce leakage and dynamic power. Aggressive uses of these techniques are resulting in designs with extremely low leakage which allows SRAM to replace non-volatile memories in selected applications. The Figure shows the bit cell and V_{dd} scaling trend of SRAM from major semiconductor manufacturers.



Bit cell and V_{dd} scaling trend of SRAM from major semiconductor manufacturers.

High-Bandwidth DRAM:

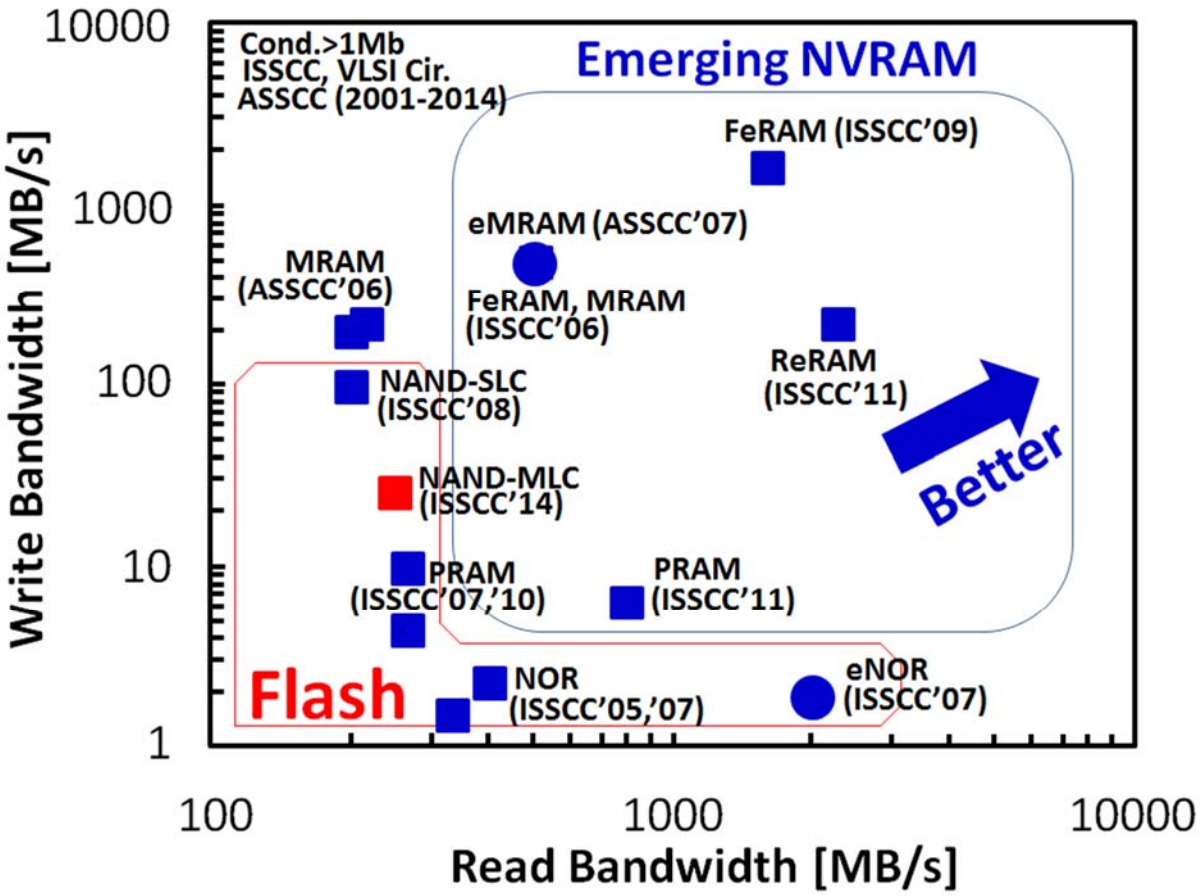
In order to reduce the bandwidth gap between main memory and processor performance, DRAM data rates continue to increase at the memory interface, using schemes such as DDRx, LPDDRx, and GDDRx, as shown in next **Error! Reference source not found.**. Currently, DDR4 and GDDR5 memory I/Os operate around 3Gb/s/pin and 7Gb/s/pin, respectively, which represent aggregate rates of 6GB/s and 28GB/s, respectively. To achieve higher bandwidth of 128GB/s, 4 TSV layers are stacked with 8 channels using a total of 1024 I/Os. This high-bandwidth memory (HBM) device is targeted for high-performance next-generation high-end devices including graphics and network applications. The LPDDR4 SDRAM achieves a data rate of 3.2Gb/s/pin with a 1.0V supply, and has an integrated ECC engine for sub-1V operation. For mobile graphics memory, a GDDR5M achieves low standby power of only 5.4mW using WCK auto-sync mode. Additional circuit techniques including clock timing skewing and error-adaptive duty-cycle correction are applied to improve signal integrity.



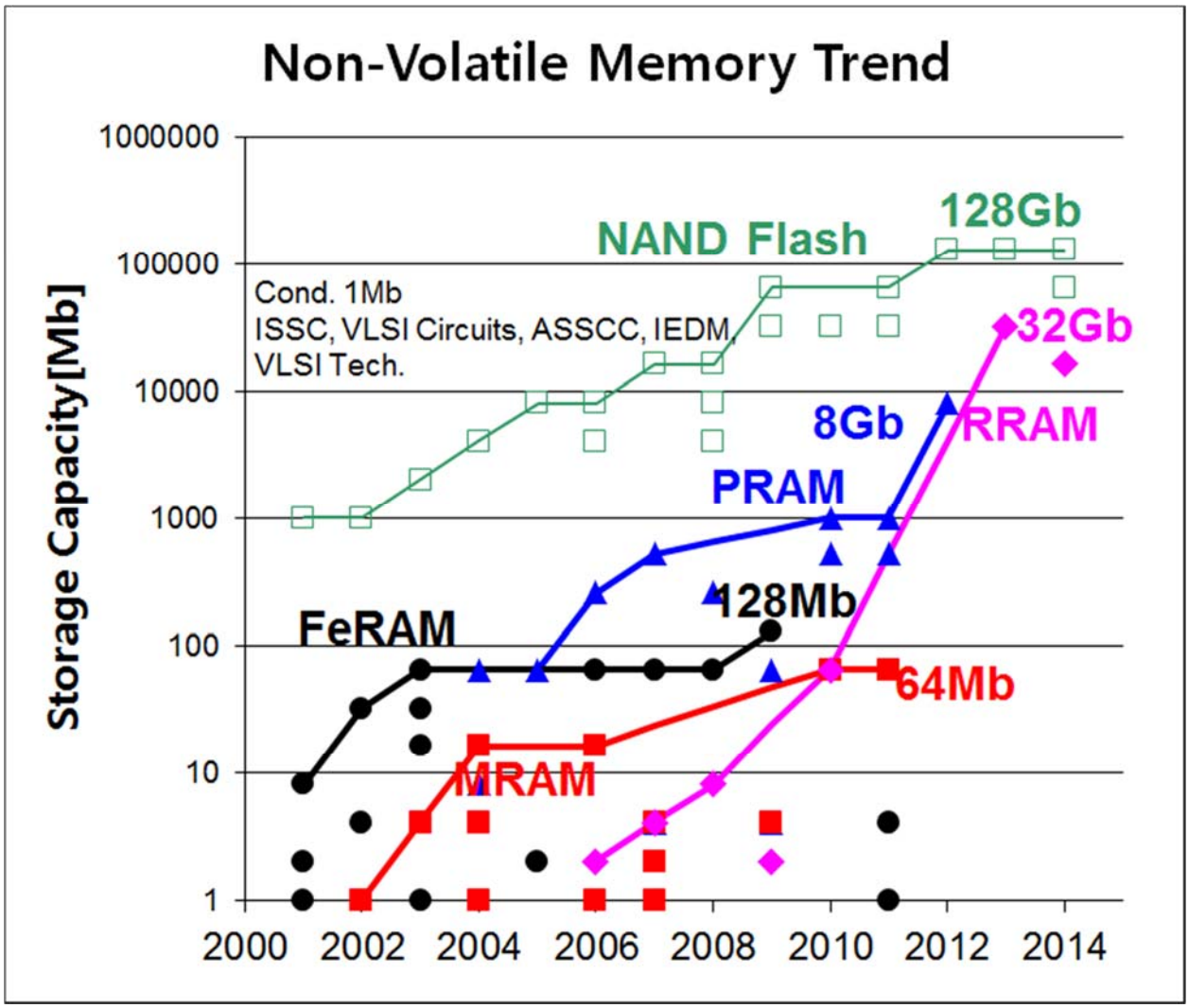
DRAM Data bandwidth trends.

Non-Volatile Memories (NVMs):

In the past decade, significant investment has been put into emerging memories to find an alternative to floating-gate based non-volatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Some commercial applications, such as cellular phones, have recently started to use PRAM, demonstrating that reliability and cost competitiveness in emerging memories is becoming a reality. Fast write speed and low read-access time are the potential benefits of these emerging memories. At ISSCC 2014, a high-density ReRAM with a buried WL access device is introduced to improve the write performance and area. The next Figure highlights how MLC NAND Flash write throughput continues to improve. However, while the Figure following shows no increase in NAND Flash density over the past year, recent devices are built with finer dimensions or more sophisticated 3-dimensional vertical bit cells.



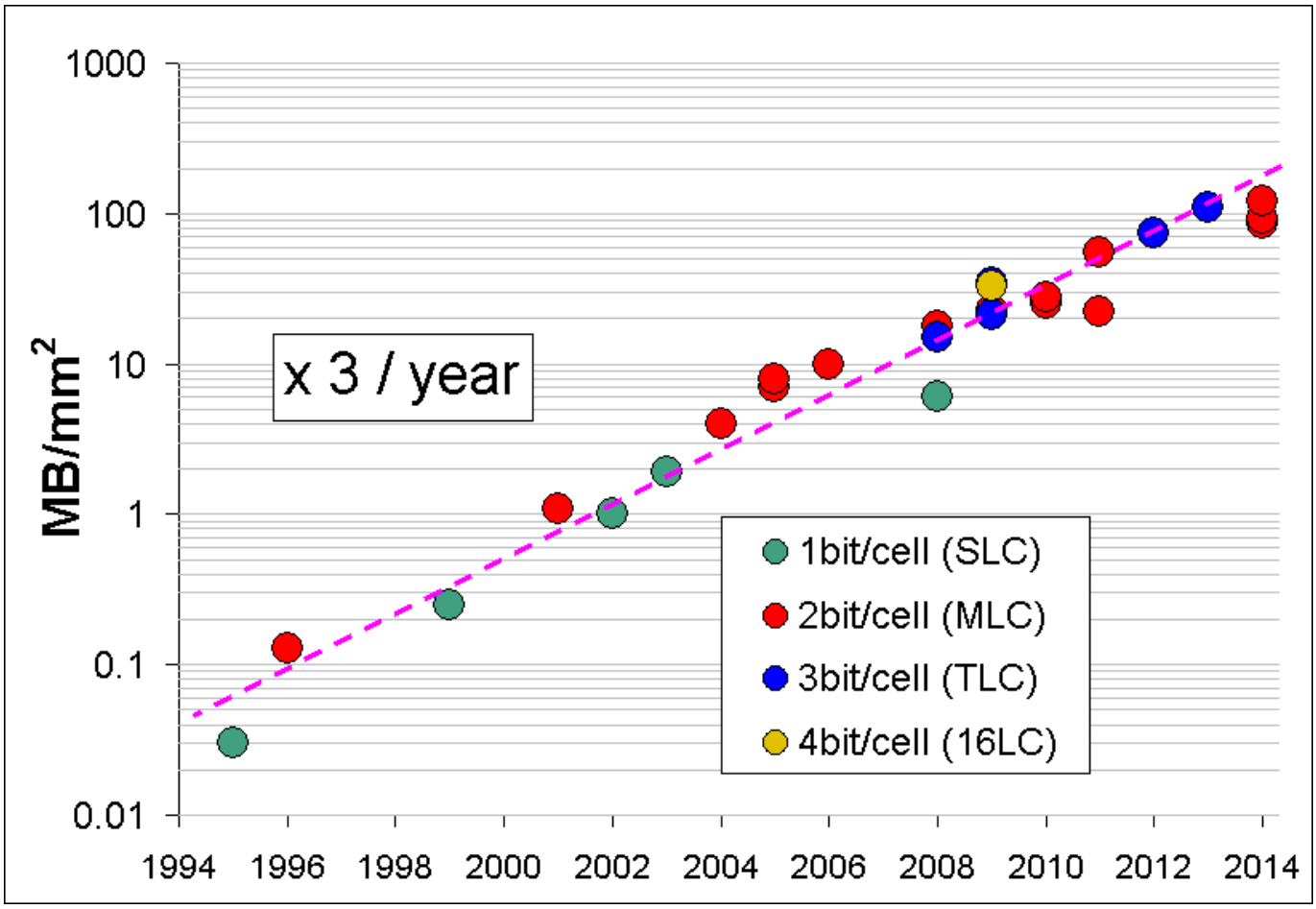
Read/write bandwidth comparison of nonvolatile memories.



Memory capacity trend of emerging nonvolatile memories.

NAND-Flash Memory:

NAND-Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). Despite growing difficulties with further down scaling of planar cell technology, the latest 2D NAND Flash technology has scaled from 20nm down to 16nm.The next **Error! Reference source not found.** shows the observed trend in NAND Flash capacities presented at ISSCC over the past 20 years. Along with scaling, to overcome the increased device variability and error rates, sophisticated control algorithms to offset this trend have been implemented outside the NAND silicon in the system memory controller, especially ECC and data management methods. This year, to address the ever-growing scaling challenges, such as manufacturing cost increase and reliability degradation, in conventional 2D NAND Flash memories, 3D stacked NAND vertical gates is being introduced as an alternative technology solution to further increase NAND density, and lower manufacturing cost.



NAND-Flash memory trends.

HISTORICAL TRENDS IN TECHNICAL THEMES

Innovative Topics

(Imagers/MEMS/Medical/Displays Subcommittee
Technology Directions Subcommittee)

Imagers/MEMS/Medical/Displays – 2014 Trends

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany*

Imagers:

The CMOS-image-sensor business is one of the fastest-growing segments of the semiconductor industry. Key applications include cell-phone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-cinema cameras, and gaming.

The resolution and miniaturization races are ongoing, and while the performance requirements stay constant, pixel size continues to scale down. Images of over 40M Pixels are commercially available. A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Backside illumination is now a mainstream technology for mobile imaging. Wafer stacking of the image array on a CMOS image signal processor will become common.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. While HDR combines multiple distinct images, new work is progressing with specialized architectures to extend the dynamic range in single exposures, and thus avoid movement artifacts. As well, global shutters are being introduced to avoid movement artifacts.

For precision scientific and medical applications, we now employ single-photon avalanche diode (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high resolution, high accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors.

Sensors & MEMS:

MEMS has now enabled the world's smallest 32kHz ultra-low-power timing sources. Low-power timing has normally been supplied by quartz tuning forks, but miniaturization of that technology is proceeding slowly. MEMS oscillators are available in 1.5×0.8mm^2 chip-scale packages, and consume under 1µA supply current. Temperature compensation provides 3 parts per million accuracy over temperature.

On another front, gesture recognition for computers, tablets, and phones will become very important. This can be implemented using capacitive, image, or ultrasonic sensors, where the latter has a potential power advantage. MEMS transducers will be a key component of such ultrasonic systems, employing specialized driver chips. This technology has now been demonstrated, and can track multiple objects with high resolution.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy and supporting wider applications. Strides in low-power architectures continue to eclipse previous results with record-setting efficiency which support battery-operated and mobile applications. For applications in fine-geometry systems, we are seeing DTMOS-based sensors becoming more accurate, particularly at low supply voltages.

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Medical:

Medical applications continue to emphasize smaller implantable and wearable devices. While often these must operate at low power levels using miniature battery or energy-scavenging , the required data transmission rates can be large, for instance for neural-recording arrays. To minimize power consumption, and thus minimize size, such devices will require local signal pre-processing and feature extraction.

For improved capability and quality, medical ultrasound is developing toward 3D imaging with large arrays. As these arrays increase in size, the number of connections to the front-end processing circuitry, and the amount of required signal processing are becoming bottlenecks. To resolve this congestion, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together.

Smart wearable sensors for medical applications will support continuous remote monitoring with data transmission to centralized analysis systems. These sensors will adapt their algorithms to match specific user's vital signs. Potentially, closed-loop control will allow therapy to be applied directly, for instance to suppress seizures or arrhythmias.

Displays:

Touch- and gesture-sensing systems for large displays are in development. These will require extensions of capacitive-sensing technology beyond the present state-of-the --art. Applications will require sensing hand gestures at a distance (30cm), and high-resolution touch for writing recognition.

LCD panels with integrated touch sensing are being driven toward thinner and lower-cost single-chip solutions. Robust circuit technology that is immune to display-driver noise is a key design factor.

Higher-resolution and higher-definition displays are being developed for mobile applications. Displays with 440 pixels-per-inch (ppi) are now in production, with new work focused beyond 500 ppi for 6-inch and smaller displays. While low-temperature polysilicon (LTPS) technology seems to be superior to amorphous-silicon (a-Si), traditional a-Si TFT and oxide TFT technologies supported by compensating driver systems are being prepared to compete.

Plastic organic light-emitting diodes (OLEDs) are entering into commercial production for curved smartphones. These will give improved user experiences, being very thin, light, and un-breakable. They are also expected to find applications in wearable displays.

Technology Directions – 2014 Trends

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

The Need for Innovative Systems:

This year, at ISSCC 2014 the theme is, "*Silicon Systems Bridging the Cloud*". System considerations are extremely important for circuit engineers. The system designer defines the parameters such as performance, power, bandwidth, SNR, QoS, etc. to which engineers design their hardware. In addition, the system designer can help the hardware engineer optimize across the entire system. Thus, it is apparent that the next level of innovative technology will come out of a broad understanding of how all parts of the system work together so that engineers can optimize across multiple layers. Correspondingly, we are highlighting two diverse systems which will drive future innovation: Biomedical Systems for Improved Quality of Life, and High-speed Systems for Data Networks.

Innovative Biomedical Systems:

A breakthrough concept in biomedical electronics is the development of "anytime and anywhere" human monitoring systems using wearable/implantable devices. Such devices will enable improved of quality of life, through self-health checks, remote examination by doctors, and constant monitoring for acute diseases.

Key technologies such system include:

(1) Small-footprint devices and flexible electronics to enhance the comfort of wearable devices.
(2) High-accuracy monitoring devices.
(3) Low-power monitoring and communication systems for long-duration autonomous operation.

Correspondingly, highly integrated biomedical SoCs capable of sensor detection, diagnosis and wireless communication have been developed to ensure a small footprint. To this end, development of 3D-integrated electrodes and sensors with MEMS, and new-materials such as organic devices, has also contributed. In order to monitor weak vital-signs (such as electrocardiogram (ECG) and electroencephalogram (EEG)) with a high degree of accuracy, there has beenclear progress in the variation-correction methodologies needed to address environmental change and the misalignment of wearable devices. Furthermore, state-of-the-art biomedical SoCs increasingly embody multimodal bio-monitoring systems for diverse signal detection. To operate reliably over long periods, such SoCs have evolved to contain a power-efficient dedicated processor running algorithms for diagnosis, along with ultra-low-power circuit designs for body-area networking, and energy-harvesting technologies. Illustrating these trends, Session 18 at ISSCC 2014 features the latest in biomedical systems.

Innovative High-speed Data Networks:

In the past few decades, many new applications such as mobile devices and the Internet have driven the growth of high-performance computing systems. The next big application drivers will include cloud computing, Big-Data, and the Internet-of-Things, which will require increasing performance demands on the backbone of the infrastructure. Important trends and challenges of the future that necessitate system innovation include:

(1) Satisfying performance demands that increase at an exponential rate.
(2) Containing the power dissipated in data centers whose electricity and cooling costs are skyrocketing.

To meet these challenges, innovative architectures for the infrastructure (such as servers, network routers, andmobiles) are under development to support increased performance demands. For example, minimizing latency of memory access is critical to network processing performance. For this purpose, novel network-on-chip (NoC) architectures that optimize memory bandwidth and implement advanced memory access protocols/algorithms are needed. Furthermore, low-power processor architectures are needed to contain the power dissipated by high performance systems. As protocols and software can make significant impact, these need to be co-optimized with the architecture.

New circuit technology is also needed to reach the power and performance requirements of data networks. For example, advanced clocking techniques are needed within the required GHz ICs. As well, power-management techniques traditionally used for energy limited applications are being employed within high-performance systems. Furthermore, new packaging techniques, such as 3D interconnects with homogeneous and heterogeneous usage are being investigated for high-performance systems. Session 6 at ISSCC 2014 features innovative high-performance data network systems where challenging system requirements spur the development of novel solutions.

5. INDEX

5.1 Notation

Paper numbers mentioned in the Index follow the convention S.P, where S is the session number and P is the paper order number. For example 20.2 will be second paper in the twentieth session. To quickly obtain more information about a particular paper (for example 20.2), go to the SESSION OVERVIEW part of this Press Kit, to Session 20 and down to paper 2. Some of the papers may also be included in the SESSION HIGHLIGHTS part of this Press Kit, in paper number order. Note, again, that sessions and papers are in ascending order in both the Session Overviews and Session Highlights.

5.2 Subcommittees mapped to Sessions

Analog: 4, 17, 23

Data Converters: 11, 22, 29

Energy-Efficient Digital: 10, 27

High-Performance Digital: 5, 15, 16

Imagers/MEMS/Medical/Displays (IMMD): 7, 12, 24

Memory: 13, 19, 25

Radio Frequency (RF): 3, 14, 21

Technology Directions (TD): 6, 18, 30

Wireline: 2, 8, 26

Wireless: 9, 20, 28

5.3 Technical Themes mapped to Sessions

Technical Themes	Sessions
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Analog Systems (including Analog and Data Converters)	4, 11, 17, 22, 23, 29
Digital Systems (including Energy-Efficient Digital, High-Performance Digital , and Memory)	5, 10, 13, 15, 16, 19, 25, 27
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5.4 Presenting Company/University/Laboratory mapped to Papers

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ASICentrum	18.1
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