2013

PRESS KIT

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The material presented here is preliminary.
As of November 9, 2012, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

ISSCC
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2013
Conference Overview

CONFERENCE THEME

The ISSCC 2013 Conference theme is:

"60 YEARS OF (EM)POWERING THE FUTURE"

ISSCC 2013 is the 60th Conference in an incredibly long-lasting series. Following the invention of the transistor in 1947, there was a developing interest in transistor circuit design. This coalesced in 1954, with the creation of the first "Conference on Transistor Circuits," held in Philadelphia, sponsored by the IRE, one of the predecessors of the IEEE. Since then, transistor-circuit design, which evolved into integrated-circuit design, has changed the world like no other technology ever has. Propelled by this sixty-year history, ISSCC 2013 will provide a special opportunity for looking "back to the future", toward further exciting developments in solid-state circuits and systems. ISSCC remains the premier forum in the world where circuit innovations are presented. In this role, ISSCC will continue to (em)power the future!

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PAPER STATISTICS

OVERALL:

- **4** papers invited
- **629** papers submitted to ISSCC 2013
- **209** papers accepted
    - **74** papers from North America, including
        - **30** Industry papers
        - **43** University papers
        - **1** Institution/Lab papers
    - **84** papers from the Far East, including
        - **33** Industry papers
        - **50** University papers
        - **1** Institution/Lab papers
    - **51** papers from Europe, including
        - **17** Industry papers
        - **22** University papers
        - **12** Institution/Lab papers
- **27** Sessions, over 3 days

INTERNATIONAL SCOPE:	2013	2012	2011	2010	2009
Americas:	35%	34%	38 %	41 %	38 %
Far East:	40%	36%	33 %	31 %	35 %
Europe:	24%	30%	29 %	28 %	27 %

WIDE COVERAGE:	2013	2012	2011	2010	2009
Analog:	12%	13%	10 %	9 %	11 %
Data Converters:	7%	8%	8 %	7 %	7 %
Energy-Efficient Digital:	8%	7%	6 %	6 %	6 %
High-Performance Digital:	9%	10%	7 %	10%	4 %
IMMD:	13%	13%	14 %	12 %	12 %
Memory:	9%	10 %	10 %	11 %	9 %
PLL:	--	--	--	6 %	--
RF:	12%	10%	12 %	8 %	11 %
Technology Directions:	9%	9%	10 %	12 %	13 %
Wireless:	10%	9%	11 %	11 %	13 %
Wireline:	12%	10%	11 %	8 %	14 %

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PLENARY SESSION

PAPER 1.1:

Architecting the Future through Heterogeneous Computing

Lisa Su

Senior Vice President and General Manager, AMD, Austin, TX

Heterogeneous computing is changing the way system designers, software developers, and end users, are creating and experiencing the future of technology. The most-compelling emerging algorithms are parallel in nature rather than serial CPU-centric. Virtually every computing device – whether smartphone, tablet, or PC – is transitioning to a new world: with smaller, lighter, and cooler form factors; with more media and less text; with higher DPI screens and high-definition video; and with a transformation from traditional user interfaces to more-natural ones, involving touch and gesture recognition.

This metamorphosis opens up tremendous opportunity for computing to impact today's norms, where most parallel code still runs on CPUs that are optimized for scalar workloads. Such mismatches are highly inefficient and waste a tremendous amount of power. Similarly, video and multimedia content is best handled by parallel processing, and GPUs are much more efficient at running those workloads. In general, the key to efficient affordable optimized computing is running the right workload on the right processor at the right time. This talk addresses the industry's efforts to accelerate the adoption of heterogeneous computing, and expands upon the benefits that the end users can expect from these advances in our every day lives.

PAPER 1.2:

"Smart Life Solutions" from Home to City

Yoshiyuki Miyabe

Managing Director and CTO, Panasonic, Osaka, Japan

It has been predicted that the global demand for electricity will be twice the current level by 2035. In this event, even efficient use of resources can ensure only a limited energy supply. This energy bottleneck is one of the serious social issues in our future. Meanwhile, other inter-related developments proceed: electronic products are becoming increasingly sophisticated; users are aging; and, as a result, the demand for user-friendly interfaces is growing. To resolve these social issues, we are working to provide "Smart Life Solutions", which support both the eco-solution concept of intelligent energy saving, and the

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smart-solution concept of providing products and services optimized for individual lifestyles, by means of information and communication technology.

In the history of consumer electronics, evolving component technology has driven functional evolution: Television is a good example of this. We entered this arena in 1952, with a 17-inch black-and-white TV that contained 22 vacuum tubes. Subsequently, advances in components (transistors, ICs, microprocessors, and system LSIs), directly enabled the progress of TV sets to color, satellite, analog high definition, digital high definition, 3D, and Smart. The latest 3D and Smart TVs include system LSIs in 40-nm CMOS that contain 700 million transistors operating at 1 GHz. It is not an exaggeration to say that all growth in digital products has been driven by the progress in semiconductor technology.

In this talk, I will introduce examples of “Smart Life Solutions”: Smart Homes to provide safe and comfortable living environments while saving energy; Smart Surveillance to provide safe and intelligent retail environments; Smart Mobility to provide more convenient transportation – automobiles with lower environmental impact; and Smart Cities to provide lifestyle values through comprehensive town planning.

To achieve these solutions, key developments include advanced sensing technology, communications technology (which has drastically reduced costs), and power-device technology (which contributes to energy saving). These developments are all supported by innovative semiconductor technology.

This talk will also introduce initiatives for applying semiconductor technology to new fields, with examples from our research and development activities such as artificial photosynthesis. As well, it will describe expectations for the evolution of semiconductor technology.

PAPER 1.3:

Continuing to Shrink: Next-Generation Lithography – Progress and Prospects

Martin van den Brink

Executive Vice President and Chief Product & Technology Officer, ASML, Veldhoven, The Netherlands

Optical lithography has been the key manufacturing technology for integrated-circuit production, enabling a million-fold reduction in average transistor length over 50 years. The development of projection scanners, step and repeat tools, and now, step and scan systems at higher numerical apertures and shorter wavelengths have led to today’s main lithographic production tool: the 193nm immersion scanner. With 20nm half-pitch fabrication, at half the effective resolution limit, it is necessary to use multiple patterning, either through pattern splitting and multiple exposures, or through a self-aligned spacer process. This leads to one of two consequences: on the one hand, to a significant increase in the number of mask levels, process cost, and manufacturing complexity; and, on the other hand, to significant layout restrictions which require closer collaboration between semiconductor design and manufacturing for optimal imaging results and high yield. Even so, for lithography systems to achieve these small

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resolutions, there are other requirements: a sharp increase in process overlay (to achieve nanometer-specific positioning of the projected image on the silicon wafer); and Critical Dimension Uniformity (CDU) (to specify the nanometer consistency of the projected image). Computational lithography and high-speed diffraction-based metrology are needed to meet these challenges. To relax the complexity of the double-patterning process and layout restrictions, EUV lithography has been developed to support 1x-nm logic and memory fabrication, and has been demonstrated to meet imaging and overlay requirements. The major challenge remaining is productivity!

PAPER 1.4:

The Evolution of Technology

Carver Mead

Professor Emeritus, Caltech, Pasadena, CA

Faraday's Law of induction gave us generators, motors, telegraph, telephone, etc.
The vacuum tube gave us long-distance telephone, radio, hi-fi audio, television, and early computers.
Microcircuits have given us personal computers, cell phones, the Internet, and GPS positioning.

Now, What?

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60TH ANNIVERSARY DISTINGUISHED EVENING PANEL

TITLE: ANTIQUES FROM THE INNOVATIONS ATTIC

Organizer: **Trudy Stetzler,** *Texas Instruments, Stafford, TX, USA*

Moderators: **Anantha Chandrakasan**, *MIT, Cambridge, MA, USA*
Bram Nauta, *University of Twente, Enschede, The Netherlands*

When you clean up your attic you may find things that you have totally forgotten about. Old toys you used to play with, old books with lost stories. And then you think back to those past days and view them in the context of today's busy life. This panel does a similar thing; we have asked 6 experts from academia and industry to dig into their memories and find lost treasures in circuit design. This panel features surprises from the past sixty years (or more) and the panelists explain why the concept is significant today and should be pulled from the innovations attic.

Panelists:

Robert Brodersen, *University of California, Berkeley, CA, USA*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Yoshiaki Daimon Hagihara, *Sojo University, Kumamoto-city, Japan*
Thomas Lee, *Microsystems Technology Office, DARPA, Arlington, VA, USA*
Nicky Lu, *Etron Technology, Hsinchu, Taiwan*
Eric Vittoz, *Independent Consultant, Cernier, Switzerland*

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60 YEARS OF EUROPEAN CONTRIBUTIONS TO THE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

The Role of Europe in the Past and the Future of Electronics

The amazing development of electronics in the past decades has driven the transformation of our lifestyle: from the way we interact with each other, to how we work and play. The personal computer has become more and more portable and powerful, having turned into a tablet that is always with us. Consumer electronics has seen a rapid transformation from a model centered on bulky TV sets and sound-reproduction systems to extremely-thin large-area OLED displays and ultra-portable smart phones, which concentrate communication, gaming, and entertainment in one place. The advent of the Internet, empowered by increasingly more-capable and less-costly computing and communication, is transforming our whole world into a single global village where distance does not matter. This has had an impressive impact on our society and economy, with far-reaching consequences that are driving the future.

In this context, the International Solid-State Circuits Conference (ISSCC), the foremost global forum for presenting developments in the integrated-circuits industry, will celebrate next February its 60th Anniversary. This year, the Conference theme is: "60 Years of (Em)Powering the Future". This is a good opportunity to look back at the huge contribution that the circuit-design community has made in creating the pervasive electronics world of today with its far-reaching effects, and to look with renewed interest to what is next.

Europe's contribution to these 60 years of electronics has been notably strong in many fields: We have created a vital academic tradition and a powerful industrial sector, from which we have given a decisive push to the creation and success of many innovative products (from the CDs to mobile phones, and beyond). Today, Europe is the leader in electronics for wireless communications, automotive, and industrial applications. Correspondingly, at ISSCC 2013 next February (17-21) in San Francisco, Europe will present 51 extremely-high-quality papers. A glimpse of these contributions indicates some exciting new directions for the future:

- Ultra-low-power wireless communications and computation, destined to enable increasingly lightweight portable equipment, and wireless energy-autonomous micro-sensors that will be deployed everywhere. Such sensors can be used to optimize lighting, climate control, and solar sources, with many positive consequences, such as lowering our carbon footprint.

- Innovative sensor front-end electronics enabling a variety of advanced applications; such as biomedical assays, material analysis, and security. These devices will allow us an increasingly better awareness of a variety of factors having a profound impact on our lives.

Europe is also a key player in providing the sophisticated tools for worldwide integrated-circuit manufacturing. At ISSCC 2013, the plenary talk from Europe will be presented by Martin van den Brink, Executive Vice-President and Chief Product and Technology Officer of ASML. In his presentation, "Continuing to Shrink: Next-Generation Lithography – Progress and Prospects", van den Brink will give his views on the future of integrated-circuit manufacturing, and on the key enabling technologies that the global IC industry needs.

The ISSCC 2013 Press Kit, which can be downloaded from http://www.miracd.com/isscc2013/Press/ highlights many outstanding EU papers, which provide examples of the development directions discussed above. This information is available only to members of the Press: for access, please contact the ISSCC Press-Relations Liaison Laura Fuijno (lcfujino@aol.com). For your convenience, the table on the next page summarizes the ISSCC highlights from Europe that you will find in the Press Kit.

ISSCC is important for the growth of Europe, and Europe is important to ISSCC! For these reasons, we hope to excite much interest in this global event from your journal, magazine, or web newsletter. Both Laura Fuijno (lcfujino@aol.com) and I (aarno.parssinen@ieee.org) are at your disposal to help with any specific information you may need. Do not hesitate to contact us.

Aarno Pärssinen
European Regional Chair, ISSCC 2013 International Technical-Program Committee

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ISSCC 2013: Highlights from Europe

Paper #	Title	Technical domain
4.7	A 1 W-to-1mW Energy-Aware Interface IC for Piezoelectric Harvesting with 40nA Quiescent Current and Zero-Bias Active Rectifiers	Analog
5.1	SAW-Less Analog Front-End Receivers for TDD and FDD	RF
6.5, 6.6	A 4b ADC Manufactured in a Fully-Printed Organic Complementary Technology Including Resistors An Organic VCO-Based ADC for Quasi-Static Signals Achieving 1LSB INL at 6b Resolution	Technology Directions
6.7	A 1024×8 700ps Time-Gated SPAD Line Sensor for Laser Raman Spectroscopy and LIBS in Space and Rover-Based Planetary Exploration	Technology Directions
10.1	A 0.1-to-1.2GHz Tunable 6th-Order N-Path Channel-Select Filter with 0.6dB Passband Ripple and +7dBm Blocker Tolerance	Analog
11.3	A Versatile Timing Microsystem Based on Wafer-Level Packaged XTAL/BAW Resonators with Sub- W RTC Mode and Programmable HF Clocks	Technology Directions
13.6	A 2-to-16GHz 204mW 3mm-Resolution Stepped-Frequency Radar for Breast-Cancer Diagnostic Imaging in 65nm CMOS	RF
19.5	A Receiver for LTE Rel-11 and Beyond Supporting Non-Contiguous Carrier Aggregation	Wireless communication
26.4	A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS	Data Converters
27.5	An 8×16-pixel 92kSPAD Time-Resolved Sensor withOn-Pixel 64ps 12b TDC and 100MS/s Real-Time Energy Histogramming in 0.13 m CIS Technology for PET/MRI Applications	Imagers, MEMS, Medical and Displays

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TECHNICAL HIGHLIGHTS

ANALOG:

- Resonant wireless power transfer demonstrated up to 6W with 5V output voltage [4.1]
- A power management circuit with zero bias active rectifiers provides an energy-aware regulated voltage. [4.7]
- The first integrated filter that replaces external SAW-LNA filters in wireless transceivers and is tunable over a decade in frequency [10.1]
- Highest efficiency of 90.6% reported for LED drivers at 22W. [21.4]
- Sub-ns transient response time for a switched-capacitor CMOS DC-DC converter is the fastest ever reported for a switch-mode power supply. [21.6]

DATA CONVERTERS:

- This 28nm CMOS continuous-time $\Delta\Sigma$ modulator achieves 18MHz bandwidth, 78dB dynamic range, and 73.6dB peak SNDR while using 3.9mW of power and occupying only 0.08mm2, achieving an unprecedented figure-of-merit of 28fJ/conversion-step among comparable oversampling modulators [15.1]
- The fastest-ever single-channel 8b SAR ADC - runs at 1.2GS/s. [26.4]

ENERGY-EFFICIENT DIGITAL:

- 8 cores in two clusters on a single 28nm die suitable for both high performance and low power [9.1]
- Renesas presents a single-chip communications processor with a dual-core 1.5GHz CPU [9.2]
- First ARM based mobile application processor with a full precision, advance feature GPGPU capability and a 10x energy-efficiency over CPU solution for fused multimedia application is presented. [9.4]
- TI demonstrates a processor with NVM having a wake-up time of 358ns and 3.6% area overhead [24.7]

HIGH-PERFORMANCE DIGITAL:

- IBM introduces the next generation System z design, assembling 6 processors and 2 memory chips onto a ceramic package to create a 36 core/socket solution. [3.1]
- AMD presents Jaguar, a flexible 4-core modular processing element created for SoC integration, with a power envelope below 0.5W or frequency envelope above 1.85GHz. [3.4]
- Tokyo Institute of Technology presents a 0.022mm2 970mW dual-loop injection-locked PLL [14.1]
- Oregon State University presents a 90nm digital-clock multiplier with a 3-reference-cycle lock time for mobile SoC platforms and servers [14.5]
- Pohang University, Samsung and the University of Michigan describe a 65nm low-power transceiver for on-chip global interconnects [14.8]

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IMAGERS, MEMS, MEDICAL AND DISPLAYS:

- A fully integrated closed-loop epileptic seizure control system-on-chip with seizure detection and adaptive neural stimulation is presented. The chip is powered and configured wirelessly enabling fully implantable seizure detection. [16.1]
- A remotely powered, dual channel, micro-fluorimeter is presented for use in long-term implantable biosensor applications. The IC is packaged with a flip-chip-mounted LED, and a ferrite antenna for a fully implantable glucose-monitoring system that uses less than 1mJ per measurement. [16.7]
- Noise immunity is improved by adopting differential signaling and pseudo-noise chopping in the case of the accelerometer. [22.1]
- Code-division multiple sensing is used to drive all transmission lines simultaneously on the touch screen sensor to increase its robustness. [22.5]
- An 8×16 pixel sensor with 92160 SPADs (192×480) offers a real-time output of the total detected energy up to 100Msamples/s. A timing resolution of 263ps FWHM is achieved. [27.5]
- A 2.1M 3D vision image sensor with 2.75×2.75mm2 pixels provides right-eye and left-eye images at 30fps. Buried sub-wavelength micro lenses successfully suppress the crosstalk between right-eye and left-eye pixels to 6%. [27.8]

MEMORY:

- The Highest density in ReRAM developments: 32Gb with the chip size of 130.7mm2 [12.1]
- This paper describes a single-ended transceiver design with highest reported data rate at 6.4Gb/s/pin for high-density dual-rank DIMM modules for commercial applications. [17.1]
- Smallest reported 6T-SRAM bit cell area of 0.081mm2 [18.1]

RF:

- Best-in-class power and size SAW-less receiver for cellular applications. [5.1]
- The world's first CMOS source operating above 200GHz with an output power above 0dBm [8.2]
- The world's first 4-element phased-array radar transceiver with short pulse-forming capabilities and integrated front-end and back-end decision electronics. [8.6]
- The world's first Class-D CMOS VCO drastically reduces the power consumption without compromising phase noise. [20.1]

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TECHNOLOGY DIRECTIONS:

- First adaptive iontophoresis drug delivery system provides accurate drug dosage and compensates for tissue impedance and temperature changes [6.1]
- Sensor front-ends and data converters are becoming a reality in organic electronics. [6.4][6.5]
- The largest Single Photon Avalanche Diode (SPAD) line sensor ever built is reported. [6.7]
- A miniature generic timing microsystem relying on low frequency Quartz and BAW resonators to deliver clocks whose frequencies span a range from 32kHz to several tens of MHz has been implemented using vacuum sealing wafer level packaging technologies [11.3]
- “Non-contact connector” technologies achieve record speed and energy efficiency [11.5][11.6]

WIRELESS:

- First 60GHz chipset for new WiGig/IEEE 802.11ad multi-Gb/s standard [13.1]
- All-digital transmitter supporting 256-QAM OFDM [19.3]
- First reported LTE receiver supporting non-contiguous carrier aggregation [19.5]
- The world’s first 802.15.6 wireless body area network (WBAN) transceiver with electro-acupuncture application [25.7]

WIRELINE:

- Researchers from UC Berkeley report the first 66Gb/s CMOS Multi-Tap Decision Feedback Equalizer [2.2]
- Technologists from Broadcom describe the first fully integrated CMOS chipset for 40Gb/s OC-768 applications [2.3]
- Robust quad 25Gb/s TIA [7.1]
- High sensitivity quad 25-28Gb/s TIA [7.2]
- This paper is the first ever to report a baud-rate ADC-based receiver with blind clock [7.4]
- 16Gb/s 64-ch differential package-to-package serial link with 2.6pJ/bit [23.2]
- 20Gb/s multi-channel single-ended in-package serial link with 0.54pJ/bit [23.3]

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ISSCC 2013
SESSION OVERVIEWS
AND HIGHLIGHTS

CONDITIONS OF PUBLICATION

PREAMBLE

- The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2013 in February in San Francisco
- OBTAINING COPYRIGHT to ISSCC press material is EASY!
- You may quote the Subcommittee Chair as the author of the text if authorship is required.
- You are welcome to use this material, copyright- and royalty-free, with the following understanding:
    - That you will maintain at least one reference to ISSCC 2013 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.
    - That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 60th appearance of ISSCC, on February 17th to the 21th, 2013, in San Francisco.

> This and other related topics will be discussed at length at ISSCC 2013, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 17-21, 2013, at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: Ultra-High-Speed Transceivers and Equalizers

WIRELINE SUBCOMMITTEE

Session Chair: *Ken Chang, Xilinx, San Jose, CA*
Session Co-Chair: *Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY*

With the continuing growth in and demand for data communication bandwidth, designs targeting standards such as 100GbE, OIF CEI-25G, SONET OC768, and beyond are increasingly important. The transmission and reception of such high data rates through challenging electrical channels requires sophisticated yet energy-efficient equalizer design techniques. This session includes 8 papers, describing 32Gb/s to 66Gb/s transceivers and equalizer designs for backplane and chip-to-chip applications, a 20+G decision feedback equalizer (DFE) technique, and an ADC based 10GKR backplane transceiver.

- In paper 2.1, Fujitsu presents a 32Gb/s receiver with a low-frequency equalizer (LFEQ) is implemented in 28nm CMOS. The LFEQ compensates for losses due to skin effect while the medium frequency loss is compensated by a continuous-time linear equalizer (CTLE) and the high frequency loss by a 2-tap DFE. The receiver achieves BER < 10-12 over a -40dB channel.
- In paper 2.2, UC Berkeley presents a 66Gb/s 3-tap DFE implemented in a 65nm GP CMOS process. The DFE core occupies 30um by 55um and dissipates only 46mW, representing an energy-efficiency of ~0.7pJ/bit at 1.5× higher line-rate than the fastest reported CMOS DFE to-date.
- In paper 2.3, Broadcom presents a 39.8-to-44.6Gb/s TX and RX fully integrated chipset is realized in 40nm CMOS. The TX implements a 2-tap FIR with delay-based de-emphasis, while the RX uses a quarter-rate CDR architecture. The TX output shows 0.9pspp ISI and 0.2psrms random jitter (RJ) at 0.87W. The RX achieves a jitter tolerance of 0.6UIpp at 80MHz and an input sensitivity of 20mVpp-diff at 1.05W. Channel loss handling ability is 20.4dB at Nyquist.
- In paper 2.4, Broadcom presents a dual-path receiver AFE is designed to operate over a wide range of channels at 8.5 to 11.5Gb/s. The ADC-based path has a 6-bit time-interleaved rectifying ADC, compensates 34dB loss for a copper channel and achieves >6dB margin for MMF stressors, consuming 195mW with FOM of 0.59pJ/step at 5GHz. The 55mW Slicer-based path uses a CTLE to provide 10dB equalization. The AFE occupies 0.82mm2 in 40nm CMOS.
- In paper 2.5, Fujitsu presents a 32Gb/s over-sampled data-interpolator receiver for backplane communications is presented. The receiver has a CTLE and a 2-tap loop unrolled DFE using adjustable-threshold comparators. Implemented in 0.24mm2 in a 28-nm CMOS process, the total power consumption is 308.4mW from a 0.9V supply.
- In paper 2.6, UCLA presents an 88mW 32-to-48 Gb/s serial-link transmitter. The operating range is maximized and optimally positioned using a high-speed final multiplexing stage with multiphase sampling to avoid timing violations. In addition, multiphase sampling allows significant power and area savings by minimizing the number of latches required for inter-stage resynchronization.
- In paper 2.7, Fujitsu presents 32Gb/s transmitter that uses a quarter-rate time-interleaved front-end in 28nm CMOS is presented. The transmitter uses 4-way interleaved sub-drivers generating a 2UI-wide unit-pulse response, eliminating the need for a power-hungry 2-to-1 MUX. An ordinary decision-feedback equalizer (DFE) receiver for a non-return-to-zero (NRZ) signal can receive the signal.
- In paper 2.8, UC Berkeley and Rambus present a 2-tap partial-response DFE receiver that eliminates the sequential element overhead from the critical feedback path is demonstrated in a 40nm LP CMOS process. At

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22Gb/s, the receiver achieves 0.26UI timing margin at BER of 10-12 over an AC-coupled 10” FR4 channel while demonstrating energy efficiency of 0.94mW/Gb/s.

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Session 2 Highlights: Ultra-High-Speed Transceivers and Equalizers

[2.2] A 66Gb/s 46mW 3-Tap Decision Feedback Equalizer in 65nm CMOS
[2.3] A Sub-2W 39.8-to-44.6Gb/s Transmitter and Receiver Chipset with SFI-5.2 Interface in 40nm CMOS

Paper 2.2 Authors: *Y. Lu, E. Alon*
Paper 2.2 Affiliation: *University of California, Berkeley, CA*
Paper 2.3 Authors: *Bharath Raghavan, Delong Cui, Ullas Singh, Hassan Maarefi, Dave Pi, Anand Vasani, Zhi Huang, Afshin Momtaz, Jun Cao*
Paper 2.3 Affiliation: *Broadcom, Irvine, CA*
Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY*

CONTEXT AND STATE OF THE ART

- Given the insatiable and ever-growing demand for additional bandwidth, electrical transceivers are under continual pressure to supply ever-higher serial data rates. Meeting this demand without increasing the power footprint of the I/O solution, especially in the context of the limited pin resources of widely available packaging solutions, is driving electrical transceiver solutions to 40Gb/s and beyond data-rates on a per-lane basis. As these transceivers must meet stringent timing and performance constraints, success in realizing such solutions in turn demands increased levels of integration, performance, and energy efficiency that push the limits of standard CMOS technology.

TECHNICAL HIGHLIGHTS

- **Researchers from UC Berkeley report the first 66Gb/s CMOS Multi-Tap Decision Feedback Equalizer**
- In paper 2.2, a 66Gb/s CMOS 3-tap decision feedback equalizer (DFE) is implemented in a 65nm GP process. The DFE core occupies 30×55 m^2 and dissipates only 46mW, representing an energy-efficiency of ~0.7pJ/bit at 1.5× the line-rate of the fastest reported CMOS DFE to-date.

- **Technologists from Broadcom describe the first fully integrated CMOS chipset for 40Gb/s OC-768 applications**
- In paper 2.3, A 39.8-to-44.6Gb/s TX and RX chipset is designed in 40nm CMOS. The TX implements a 2-tap FIR with delay-based de-emphasis. The RX uses a quarter-rate CDR architecture. The chipset consumes less than 2W.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of complete transceivers and energy-efficient equalizers operating at 40-60+ Gb/s suggests the possibility of a proliferation of highly integrated advanced CMOS implementations at data rates previously demanding multi-chip solutions in exotic technologies.
- A parallel bus of next-generation 60+Gb/s links with pJ/b efficiencies would enable terabyte per second throughputs at low power.

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Session 3 Overview: Processors

HIGH PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Se-Hyun Yang, Samsung Electronics, Yongin, Korea*
Session Co-Chair: *Eric Fluhr, IBM, Austin, TX*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital*

Exploding data growth in the computing industry surpasses Moore's Law and brings new performance and power challenges for today's microprocessor designs. This year's processor session introduces high-end processor and systems papers. These processors show increases in core/thread counts, frequency, on-chip cache memory and system-level scalabilities. This creates performance-power-balanced systems which can handle the "Big Data" demands of today's datacenters. Other papers in this session demonstrate solutions to problems encountered in mobile and network computing, such as power reduction, data security, and on-chip communication.

- In Paper 3.1, IBM presents their latest System z microprocessor chip that features six 5.5GHz cores and a 48MB eDRAM L3 cache. The processor has 2.75B transistors on a 598mm^2 die. The chip is implemented in a 32nm high-κ metal-gate SOI technology with 15 layers of metal. Six of such chips are placed on a 102-layer multi-chip module with two 192MB L4 cache chips to achieve a total bandwidth of 530GB/s.
- In Paper 3.2, Oracle introduces their next-generation SPARC T5 processor in 28nm process technology with 13 metal layers containing 1.5B transistors. The chip integrates 16 3.6GHz cores and a shared 8MB L3 cache with a 9-port crossbar. Compared to its 40nm predecessor, T5 doubles core count and L3 cache size and triples memory bandwidth, while improving power efficiency.
- In Paper 3.3, researchers from the National Chiao Tung University present a 1.38mm^2 elliptic-curve cryptographic (ECC) processor with 342k gates in 90nm technology, supporting IEEE P1363 public key. The processor improves system performance, achieving 521b elliptic-curve scalar multiplication in 3.40/2.77ms, while demonstrating resilience against a variety of side-channel attacks.
- In Paper 3.4, AMD introduces their first 28nm 11-metal layer x86 processor code-named "Jaguar", supporting applications from sub-5W SoCs to 25W client products. The 26.2mm^2 quad-core processor runs at up to 1.85GHz and is implemented with an emphasis on design efficiency, while improving instructions-per-cycle, frequency and power compared to the prior generation 40nm dual-core "Bobcat".
- In Paper 3.5, Loongson Technology demonstrates their latest 8-core microprocessor, Godson-3B1500, fabricated in a 32nm high-K metal-gate process with 10 layers of metal, containing 1.14B transistors. The processor operates at 1.35GHz, while achieving 172.8GFLOPS at 40W. Architectural and circuit improvements enable an operating voltage range from 0.9 to 1.3V, and improve power efficiency by 35% relative to its 65nm predecessor.
- In Paper 3.6, a team from Fudan University presents a 24-core processor in 65nm that integrates packet-switched and circuit-switched layers into a 435Gb/s network-on-chip achieving 11Tb/s/W. The processor utilizes 4 reconfigurable execution arrays to augment core performance. The 18.8mm^2 processor operates at 850MHz and 1.2V.
- In Paper 3.7, Oracle's SPARC T5 system demonstrates glueless scaling to 8 sockets, or 128 cores, to deliver a total of 1024 threads in a single system. Its new I/O system architecture enables over 5TB/s bandwidth. The processor implements thermal and current throttling techniques with DVFS and cycle-skipping for power management. The long-reach SerDes achieves a power efficiency of 16.7mW/Gbps at 15Gbps.
- In Paper 3.8, Fujitsu presents their next-generation SPARC64-X processor that runs at 3.0GHz and contains 16 cores with 24MB shared L2 cache and interfaces for system, DDR3, as well as PCIe. Fabricated in 28nm CMOS technology with 13 metal layers on a 588mm^2 die, the 3B-transistor processor employs newly-developed register files and 14.5GB/s SerDes for mission-critical server applications.

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Session 3 Highlights: Processors

[3.1] 5.5GHz System z Microprocessor and Multichip Module
[3.4] Jaguar: A Next-Generation Low-Power x86-64 Core

Paper [3.1] Authors: *J. Warnock[1], Y. Chan[2], H. Harrer[3], D. Rude[2], R. Puri[1], S. Carey[2], G. Salem[4], G. Mayer[3], Y.-H. Chan[2], M. Mayo[2], A. Jatkowski[2], G. Strevig[5], L. Sigal[1], A. Datta[6], A. Gattiker[5], A. Bansal[1], D. Malone[2], T. Strach[3], H. Wen[5], P.-K. Mak[2], C.-L. Shum[2], D. Plass[2], C. Webb[2]*
Paper [3.1] Affiliation: *[1]IBM T.J. Watson, Yorktown Heights, NY, [2]IBM Poughkeepsie, NY, [3]IBM, Boeblingen, Germany, [4]IBM, Williston, VT, [5]IBM, Austin, TX, [6]IBM, Bangalore, India*
Paper [3.4] Authors: *S. Southard, T. Singh, J. Bell*
Paper [3.4] Affiliation: *AMD, Austin, TX*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA; High Performance Digital*

CONTEXT AND STATE OF THE ART

- Physical scaling continues, with greater penetration of 32nm and 28nm technology nodes in commercial products, demonstrated this year by IBM's System z and AMD's Jaguar products.
- As the demands of cloud computing and workload diversity increase, these modern microprocessors adapt by integrating higher numbers of cores, larger cache sizes, and advanced I/O topologies.
- Despite the ever-increasing integration, maintaining control of device power and engineering around process variability or reliability issues remain key challenges.

TECHNICAL HIGHLIGHTS

- **IBM introduces the next generation System z design, assembling 6 processors and 2 memory chips onto a ceramic package to create a 36 core/socket solution.**
- IBM presents their latest System z processor that features six 5.5GHz cores and a 48MB eDRAM L3 cache. The processor has 2.75B transistors on a 598mm^2 die. The chip is implemented in a 32nm high-κ metal-gate SOI technology with 15 layers of metal. Six of such chips are placed on a 102-layer multi-chip module with two 192MB L4 cache chips to achieve 36 cores/socket with a total MCM bandwidth of 530GB/s.
- **AMD presents Jaguar, a flexible 4-core modular processing element created for SoC integration, with a power envelope below 0.5W or frequency envelope above 1.85GHz.**
- AMD introduces their first 28nm 11-metal layer x86 processor code-named "Jaguar", supporting applications from sub-5W SoCs to 25W client products. The 26.2mm^2 quad-core processor runs up to 1.85GHz and is implemented with an emphasis on design efficiency, while improving instructions-per-cycle, frequency and power compared to the prior-generation 40nm dual-core "Bobcat".

APPLICATIONS AND ECONOMIC IMPACT

- The IBM and AMD processors represent two major aspects of processor development: extreme performance and power efficiency. These greater levels of performance in ever-more dense form factors will extend our abilities in

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science, such as understanding the human genome. Businesses will be able to consolidate workloads, increasing their data-processing capabilities and enabling lower cost to consumers.

- In contrast, extremely power-efficient designs enable ubiquitous computing. Portable devices such as tablets are becoming more capable and less costly, enabling widespread use in areas such as early education and medical care. Reduced energy requirements enable greater freedom from the power grid and open up opportunities for alternate or renewable power sources, and enhanced social computing increases societal well-being.

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Session 4 Overview: Harvesting and Wireless Power

ANALOG SUBCOMMITTEE

Session Chair: *Jae-Youl Lee, Samsung Electronics, Korea*
Session Co-Chair: *Saska Lindfors, Texas Instruments, Finland*

Subcommittee Chair: *Bill Redman-White, Southampton University, UK, Analog Subcommittee*

Powering devices either wirelessly or from ambient energy sources continues to be a topic of great interest. Achieving high power efficiency over a wide range of power levels is equally important in both wireless power and harvesting techniques. This session begins with two papers introducing techniques to advance power efficiency and capacity in wireless or inductive power transfer followed by six papers focusing on photovoltaic and piezoelectric harvesters. The main areas of interest in harvesters are achieving faster or lower power implementation of a maximum power point tracking (MPPT) algorithm, and high efficiency over a wide power range.

- In paper 4.1, KAIST presents a resonant regulating rectifier in 0.35μm BCD for a 6.78MHz wireless charger with 86% efficiency. An output power of 6W at 5V is achieved utilizing the receiver coil as part of a new switch-mode power converter concept.
- In paper 4.2, HKUST describes the first 13.56MHz 1x/2x rectifier with integrated capacitors for inductive power in medical applications. The device is implemented in 0.35μm CMOS and it achieves 32mW maximum power and 84.2% peak power efficiency with the aid of a compensating current to reduce reverse leakage. A new rectifier topology is proposed, increasing the effective capacitance in both 1x and 2x operating modes.
- In paper 4.3, Nanyang Technological University describes a dual-input-tri-output DC-DC Buck-Boost converter in 0.18μm CMOS for photovoltaic energy harvesting. The converter regulates two outputs at 1V and 1.8V and consumes only 400nW quiescent power. It achieves 83% peak power efficiency with up to 10mW output power and tracks the maximum power point of the photovoltaic cell by using the Perturb and Observe MPPT algorithm.
- In paper 4.4, National Cheng Kung University presents a photovoltaic energy harvesting integrated circuit in 0.5μm CMOS with 94% peak power conversion efficiency. In order to adapt to changing external conditions, a fast MPPT technique achieving 470μs settling is introduced.
- In Paper 4.5, National Chung Cheng University presents a 3.4mW photovoltaic energy-harvesting charger in 0.35μm CMOS with integrated MPPT and battery management. With a sectored hill-climbing based MPPT scheme, it realizes 89% maximum power efficiency and 10μs locking time under wide-range illumination variation for wireless sensor applications.
- In Paper 4.6, IMEC presents an integrated 5 to 60V input voltage and 25 to 1600μW input power DC-DC converter in 0.35μm BCD. A fully analog variable-step perturb-and-observe MPPT algorithm with 99.9% tracking efficiency is realized by using a low-leakage sample and hold (S/H) scheme, which has at least 300 times lower leakage than a standard circuit and consumes less than 1.3μA. The overall system achieves 88.7% peak efficiency at 30V input voltage.
- In Paper 4.7, IMEC demonstrates a 1μW-to-1mW energy-aware interface IC in 0.25μm CMOS for piezoelectric harvesting with zero-bias active rectifiers. This rectifier realizes 40nA quiescent current and 94% efficiency. The energy-aware supply-voltage regulator consumes less than 140nW.
- In Paper 4.8, Georgia Institute of Technology presents a piezoelectric energy harvester, which invests energy into a piezoelectric transducer to increase the electrical damping force and enhance net output power. By using a single-inductor switching converter in 0.35μm CMOS, the prototype produces 6μW to 51μW from periodic vibrations whose acceleration rates range from 0.09m/s2 to 0.24m/s2. The system can also charge a 475nF output capacitor by 505nJ to 825nJ from aperiodic inputs such as a finger-tapping motion.

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Session 4 Highlights: Harvesting and Wireless Power

***[4.1* A Resonant Regulating Rectifier (3R) Operating at 6.78 MHz for A 6W Wireless Charger with 86% Efficiency**
***[4.7]* A 1µW-to-1mW Energy-Aware Interface IC for Piezoelectric Harvesting with 40nA quiescent current and Zero Bias Active Rectifiers**

Paper [4.1] Authors: Jun-Han Choi[1], Sung-Ku Yeo[2], Chang-Byong Park[1], and Gyu-Hyeong Cho[1]
Paper [4.1] Affiliation: [1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Suwon, Korea
Paper [4.7] Authors: Younis Allasasmeh[1], Stefano Stanzione[1], Chris Van Liempd[1] and Chris Van Hoof[2,3]
Paper [4.7] Affiliation: [1]imec - Holst Centre, Eindhoven, The Netherlands, [2]imec, Leuven, Belgium, [3]KU Leuven, Leuven, Belgium
Subcommittee Chair: *Bill Redman-White, Southampton University, UK*

CONTEXT AND STATE OF THE ART

- Wireless power transfer to mobile devices permits charging batteries at a distance but receivers require the highest possible efficiency. [4.1]
- Previous implementations of piezoelectric energy harvesting circuits using rectifiers and supply voltage regulators suffer from high-energy losses, especially when considering intermittent harvested powers. [4.7]

TECHNICAL HIGHLIGHTS

- **Resonant wireless power transfer demonstrated up to 6W with 5V output voltage [4.1]**
- 86% efficiency including diode losses [4.1]
- **A power management circuit with zero bias active rectifiers provides an energy-aware regulated voltage. [4.7]**
- Fully autonomous IC accumulates and regulates charge on a storage capacitor while consuming only 40nA quiescent current. [4.7]
- The efficiency of the rectifiers is 90 to 94% for powers in the range of 1 W to 1mW. [4.7]

APPLICATIONS AND ECONOMIC IMPACT

- Wireless power transfer has become a recent trend for mobile phones. [4.1]
- Autonomous smart sensor systems drive an intensive use of ultra-low-power circuit techniques. [4.7]

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Session 5 Overview: RF Techniques

RF SUBCOMMITTEE

Session Chair: *Mike Keaveney, Analog Device, Limerick, Ireland*
Session Co-Chair: *Joe Golat, Motorola Solutions, Schaumburg, IL*

Subcommittee Chair: *Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee*

New circuit architectures continue to evolve to enhance the performance of highly integrated CMOS radios. Cancellation schemes have been implemented to improve immunity to high blocker levels at the receiver front-end. In the transmitter, advancements have been made in efficiency improvement and also in achieving higher output power in deep submicron CMOS.

- In Paper 5.1, the Unversity of Pavia presents a 0dBm blocker-tolerant SAW-less receiver in 40nm CMOS with +16dBm out-of-band IIP3 and +65dBm IIP2. The receiver also utilizes a current-mode passive mixer with baseband LC series resonance that provides 56/65dB 3rd/5th-order harmonic rejection.
- In Paper 5.2, the University ot Twente and TNO the authors demonstrate both spatial and RF filtering techniques to achieve a 4-element phased-array receiver in 65nm CMOS tolerant to +10dBm out-of-band blockers.
- In Paper 5.3, Broadcom describes a new architecture capable of minimizing the effects of phase noise and spurs on the receiver NF in the presence of a large blocker. This new topology relaxes the performance requirements of the integrated local oscillator and is implemented in a 40nm CMOS technology.
- In Paper 5.4, Stanford presents a scalable power amplifier array in 65nm CMOS capable of delivering 30.3dBm output power at 5.3GHz with a PAE of 17.8%. The authors utilize both series-parallel transformer combining and transistor stacking to achieve this high level of performance.
- In Paper 5.5, Toshiba describes a 3.3V linear power amplifier in 65nm CMOS which achieves 27.2dBm output power at 1.8GHz. This PA incorporates a new supply-path switching scheme capable of envelope tracking that improves PAE in the power back-off mode.
- In Paper 5.6, KAIST and PHY CHIPS propose a new dead-zone amplifier-based technique for TX -leakage suppression into an RFID receiver, at 0.18µm CMOS, improving SNR by up to 15.8dB.
- In Paper 5.7, Scintera demonstrate an 11th-order analog predistorter with 25dB linearly improvement from 100MHz to 4GHz. This consumes less that 200mW from 1.8V and is implemented on 0.18µm CMOS technology.

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Session 5 Highlights: RF Techniques

[5.1] SAW-Less Analog Front-End Receivers for TDD and FDD

Paper Authors: *I. Fabiano, M. Sosio, A. Liscidini*, R. Castello*
Paper Affiliation: *University of Pavia, Pavia, Italy*
**Now at the University of Toronto, Toronto, Canada*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Modern smart phones incorporate upwards of a dozen SAW filters to support all the bands required in today's multimode/multiband world phones. Historically, these filters have been required for the phones to operate in the presence of large out-of-band interferers. Unfortunately these filters add a very large cost and size to the end product.

TECHNICAL HIGHLIGHTS

- **Best-in-class power and size SAW-less receiver for cellular applications.**
- The University of Pavia presents a 0dBm blocker-tolerant SAW-less receiver in 40nm CMOS with +16dBm out-of-band IIP3 and +65dBm IIP2. The receiver also utilizes a current-mode passive mixer with baseband LC series resonance that provides 56/65dB 3rd/5th-order harmonic rejection.

APPLICATIONS AND ECONOMIC IMPACT

- SAW-less transceivers have the potential to significantly reduce the cost of handsets and pave the way to smaller overall designs.

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Session 6 Overview: Emerging Medical and Sensor Technologies

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *David Ruffieux, CSEM, Switzerland*
Session Co-Chair: *Yogesh Ramadass, Texas Instruments, Dallas*

Subcommittee Chair: *Hoi-Jun Yoo, KAIST, South Korea, Technology Directions*

This session presents recent advances in semiconductor devices for health status diagnosis and therapy, from ICs for adaptive drug delivery to wearable monitoring and analysis of physiological signals including EEG and EMG. The second half of the session focuses on emerging technologies for sensor applications including ADCs implemented in fully-printed organic technologies, capacitive sensors made completely with carbon nano-tube FETs and SPAD line sensors for Raman spectroscopy in Mars rover applications.

- In paper 6.1, KAIST demonstrates a 110nm, 5.5mm2, 2.2mW, 87mA·min iontophoresis smart controller IC with dual-mode impedance sensors for a patch-type transdermal drug delivery system. It can measure skin temperature and contact/tissue impedance to adapt the stimulation allowing real-time monitoring of the delivered drug dosage.
- In paper 6.2, Masdar Institute of Technology introduces a 180nm, 25mm2, non-linear support vector machine-based seizure classification SoC with multichannel EEG data acquisition and storage for epileptic patients monitoring. The system achieves a seizure detection accuracy of 95%, a false alarm rate below 1% while consuming1.8μJ per classification.
- In paper 6.3, National Chiao Tung University presents a single die microsystem consisting of a 16-channel neural microprobe array connected with Through Silicon Vias to 180nm CMOS readout circuitry to enable low noise EEG measurements. The front-end achieves 1μVrms input-referred noise in a 0.4 to 7.3kHz bandwidth, while consuming 350μW.
- In paper 6.4, University of Tokyo presents a 18cm2 64-channel surface electromyogram measurement sheet implemented with 2V organic transistors for prosthetic hand control. A 4-fold increase in electrode density is achieved using a distributed and shared amplifier architecture while a post-fabrication select-and-connect method reduces transistor mismatch and power consumption.
- In paper 6.5, Eindhoven University of Technology describes a 4b ADC manufactured in a fully-printed organic complementary technology. With the help of an R2R DAC, the converter achieves rail-to-rail 40V operation with an SNDR of 19.6dB, SNR of 25.7dB and 2Hz bandwidth. The DAC's DNL and INL are 0.24 and 0.42LSB, respectively.
- In paper 6.6, Eindhoven University of Technology presents a 6b organic VCO-based ADC. Implemented in a p-only double-gate organic TFT technology, the ADC achieves an INL of 1LSB, DNL of 0.6LSB without calibration and consumes 2.4uA of current for a die area of 19.4mm2.
- In paper 6.7, Delft University of Technology presents a 30mm2, 1024x8 time-gated SPAD line sensor for time-resolved laser induced Raman spectroscopy. Intended for next generation Mars rovers, the 0.35μm HV CMOS sensor has a 44% fill factor, achieves 21% photon detection probability at 475nm, 250ps time resolution and fast 1.1ns gating.
- In paper 6.8, Stanford University unveils a fully digital capacitive sensor interface built using carbon nanotube FETs and implemented in a VLSI compatible fashion. It is the first demonstration of a complete system implemented with such a technology. The sensor interface based on a sensor controlled oscillator consumes 336uW from a 3V supply while achieving a 1.83% nonlinearity.

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Session 6 Highlights: Emerging Medical and Sensor Technologies

[6.1] An 87mA-min iontophoresis Controller IC with Dual-Mode Impedance Sensor for Patch-Type Transdermal Drug Delivery System

Paper Authors: *K. Song, U. Ha, J. Lee, K. Bong, H. Yoo*
Paper Affiliation: *KAIST, Daejeon, South Korea*

Subcommittee Chair: *Hoi-Jun Yoo, KAIST, South Korea*

CONTEXT AND STATE OF THE ART

- To date, iontophoresis drug delivery systems have not directly measured and controlled the quantity of drug delivered.
- This work demonstrates the first adaptive, real-time system for monitoring and control of drug delivery that compensates for contact/tissue impedances and changes in skin temperature.

TECHNICAL HIGHLIGHTS

- **First adaptive iontophoresis drug delivery system provides accurate drug dosage and compensates for tissue impedance and temperature changes**
- Dual-mode impedance sensor compensates for a 200:1 variation in skin impedance.
- 5.5mm2 implementation in 0.11um CMOS
- Adaptive stimulation from 16 to 512uA to accurately control drug delivery

APPLICATIONS AND ECONOMIC IMPACT

- Medical drug delivery through skin patches for a range of applications including pain management, chronic edema, diabetes and rheumatic conditions.
- Ease of use, higher accuracy of drug dosage, and safety features can expand the adoption rate of this technology.

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Session 6 Highlights: Emerging Medical and Sensor Technologies

[6.4] 1µm Thickness 64-Channel Surface Electromyogram Measurement Sheet with 2V Organic Transistors for Prosthetic Hand Control
[6.5] A 4b ADC Manufactured in a Fully-Printed Organic Complementary Technology Including Resistors
[6.6] An Organic VCO-based ADC for Quasi-Static Signals Achieving 1 LSB INL at 6b Resolution

Paper [6.4] Authors: H. Fuketa[1,2], K. Yoshioka[1,2], Y. Shinozuka[1,2], K. Ishida[1,2], T. Yokota[1,2], N. Matsuhisa[1,2], Y. Inoue[1,2], M. Sekino[1,2], T. Sekitani[1,2], M. Takamiya[1,2], T. Someya[1,2], T. Sakurai[1,2]
Paper [6.4] Affiliation: [1]University of Tokyo, [2]JST/ERATO, Tokyo, Japan
Paper [6.5] Authors: S. Abdinia[1], M. Benwadih[2], R. Coppard[2], S. Jacob[2], G. Maiellaro[3], G. Palmisano[3], M. Rizzo[4], A. Scuderi[4], F. Tramontana[4], A. van Roermund[1], E. Cantatore[1]
Paper [6.5] Affiliation: [1]Eindhoven University of Technology, Eindhoven, the Netherlands, [2]CEA-Liten, Grenoble, France, [3]University of Catania, Catania, Italy, [4]STMicroelectronics, Catania, Italy
Paper [6.6] Authors: D. Raiteri[1], P. Van Lieshout[2], A. Van Roermund[1], Eugenio Cantatore[1]
Paper [6.6] Affiliation: [1]Eindhoven University of Technology, [2]PolymerVision, Eindhoven, the Netherlands

Subcommittee Chair: Hoi-Jun Yoo, KAIST, South Korea

CONTEXT AND STATE OF THE ART

- Organic electronics is an extremely inexpensive technology that is suitable to fabricate large area and flexible electronics on thin plastic films
- As the technology is making progress in terms of yield and reliability, integration of more key building blocks such as microcontrollers, ADC, DAC has been demonstrated at previous ISSCCs allowing building increasingly complex systems.

TECHNICAL HIGHLIGHTS

- **Sensor front-ends and data converters are becoming a reality in organic electronics.**
- Paper 6.4 demonstrates the first front-end amplifier array for EMG measurement with organics electronics. Transistor mismatch and power consumption of the amplifier are reduced by 92% and 56%, respectively, by selecting and connecting the transistors through a post-process inkjet printing step. Distributed and shared amplifier (DSA) architecture enables an in-situ amplification of the myoelectric signal with a 4 times increase of EMG electrode density.
- Papers 6.5 and 6.6 present advances in ADCs for sensing applications. Paper 6.5 demonstrates the first printed ADC that integrates on the same chips resistors and n and p-type transistors. The ADC achieves an SNDR of 19.6dB, SNR of 25.7dB and BW of 2Hz. In Paper 6.6, an ADC made only with p-type transistors is presented that

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has the highest linearity without calibration and that is 14 times smaller than previous implementations using the same technology.

APPLICATIONS AND ECONOMIC IMPACT

- These papers pave the way toward large area sensors on plastic films in a cost-effective way through new manufacturing approaches.
- Application examples include large man-machine interface panels based on touch and light, monitoring food freshness and the safety of pharmaceuticals.

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Session 6 Highlights: Emerging Medical and Sensor Technologies

[6.7] A 1024×8 700ps Time-Gated SPAD Line Sensor for Laser Raman Spectroscopy and LIBS in Space and Rover-Based Planetary Exploration

Paper [6.7] Authors: *Y. Maruyama[1], J. Blacksberg[2], E. Charbon[1]*
Paper [6.7] Affiliation: *[1]Circuits and Systems, Delft University of Technology, Delft, the Netherlands, [2]Jet Propulsion Laboratory, California Institute of Technology, Pasadena, Ca.,USA*

Subcommittee Chair: *Hoi-Jun Yoo, KAIST, Korea, Technology Directions*

CONTEXT AND STATE OF THE ART

- Raman spectroscopy is a nondestructive label-free optical analysis technique used to obtain structural and compositional information without advance preparation.
- The technology presented in this paper improves the extraction of the Raman signature by filtering out in the time domain, the unwanted background fluorescence. The technology presented reduces the time-gating below 1ns and implements an array to overcome limitations of single pixel detectors.

TECHNICAL HIGHLIGHTS

- **The largest Single Photon Avalanche Diode (SPAD) line sensor ever built is reported.**
- It has one of the shortest gate widths ever reported and the shortest gate width for a SPAD line sensor above 128 pixels ever published.
- The 1024x8 time-gated, single-photon avalanche diode line sensor has a 44.3% fill factor, 21% photon detection probability at 475nm, 250ps time resolution, fast 1.1ns gating and a 24.6mm focal plane for large gratings.

APPLICATIONS AND ECONOMIC IMPACT

- Optical detection is an important technology area. The ability to do temporal filtering of the background fluorescence paves the way for smaller instrumentation.
- This technology can be applied to material analysis and space exploration.

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Session 7 Overview : Optical Transceivers and Silicon Photonics

WIRELINE SUBCOMMITTEE

Session Chair: *Ichiro Fujimori, Broadcom, Irvine CA, USA*
Session Co-Chair: *Masafumi Nogawa, NTT, Kanagawa Japan*

Subcommittee Chair: *Daniel Friedman, IBM T.J. Watson, Yorktown Heights, NY*

The continued scaling of information processing using modern technology has made conventional electrical interconnects a potential bottleneck for many applications. One approach to addressing such bottlenecks is enabling more widespread use of optical interconnects and silicon photonics. In ISSCC 2013, several breakthroughs in CMOS transceivers for optical interconnects will be presented demonstrating 25Gb/s operation which enable further emergence and penetration of 100GbE solutions. In silicon photonics-linked advances reported at ISSCC 2013, a PAM4/NRZ MZI modulator, as well as further advancement in ring modulator-based transmitters, are demonstrated. Finally, the industry's first 10Gb/s ADC based optical transceiver using blind baud rate sampling is introduced.

- In Paper 7.1, Finisar describes a quad 25Gb/s 270mW TIA in 0.13μm SiGe BiCMOS. A novel TIA architecture outputs a differential signal directly at the input stage allowing less than 0.15-dB inter-channel crosstalk penalty. The quad TIA dissipates 83mA from a 3.3V supply with better than -12dBm optical modulation amplitude sensitivity.
- In Paper 7.2, Hitachi demonstrates a 4-channel 25-to-28Gb/s CMOS optical receiver for board-to-board interconnects. The RX incorporates a novel TIA operating at 25Gb/s that achieves the highest sensitivity (-9.7dBm) at the widest eye-opening (65%) reported to date.
- In Paper 7.3, National Taiwan University presents a complete 100Gb/s Ethernet chipset in 65nm CMOS, including the gearbox Tx/Rx, LDD array, and TIA/LA array. The LDD and TIA/LA arrays achieve 25Gb/s data rate, with the TIA featuring 21GHz bandwidth and gain of 72.5dBOhm.
- In Paper 7.4, the University of Toronto demonstrates the first 10Gb/s blind baud-rate ADC-based CDR. The blind baud-rate operation is made possible through the use of 2UI integrate-and-dump at the front end in conjunction with a 2-tap DFE. The blind samples are interpolated to recover center-of-the-eye samples for a speculative Mueller-Muller CDR.
- In Paper 7.5, Texas A&M University describes a ring-resonator-based silicon photonic 65nm CMOS transceiver for optical interconnects. By employing high-swing (2Vpp and 4Vpp) drivers, novel automatic bias-based tuning for wavelength stabilization, and an adaptive sensitivity-power receiver to trade-off power for uncertainties in input capacitance and modulator/photodiode performance, efficiencies of 808fJ/bit at 5Gb/s for the TX and 275fJ/bit at 8Gb/s for the Rx are demonstrated.
- In Paper 7.6, MIT demonstrates a monolithically-integrated photonic carrier-injection ring modulator and a configurable all-digital driver circuit operating in the multi-gigabit regime, realized in a commercial 45nm SOI process. A data rate of 2.5Gb/s, which is 10× the bandwidth of the optical device, at an energy-cost of 1.23pJ/bit is achieved.
- In Paper 7.7, U. of Pennsylvania describes a NRZ/PAM-4 CMOS-photonic based optical transmitter employing a 1V supply for an MZI modulator driver operating at a data rate of 20Gb/s. The system consists of an electrical driver in 40nm CMOS and an optical MZI modulator with an RF length of less than 0.5mm (smallest MZI ever reported) in 0.13μm SOI CMOS. Modulation power efficiency of 4pJ/b for NRZ data is achieved.
- In Paper 7.8, IBM presents an optical receiver using a novel DFE-based architecture. Two proof-of-concept chips in 90nm CMOS and 0.13μm SiGe BiCMOS demonstrate power efficiencies of 0.93pJ/b at 9Gb/s and 3.52pJ/b at 15Gb/s, respectively. Measured sensitivities at BER ≤ 10-12 are -8dBm (9Gb/s, 90nm CMOS) and -10dBm (15Gb/s, 0.13μm SiGe).

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- In Paper 7.9, Delft University of Technology presents the first fully-digital-controlled distributed amplifier with the fastest rise/fall times of 15ps in 0.18μm SiGe (60GHz peak-fT), producing a 6Vpp differential output swing at a data rate of 10Gb/s. The area of the prototype is 2.8mm2.

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Session 7 Highlights: Optical Transceivers and Silicon Photonics

[7.1] A Quad 25Gb/s 270mW TIA in 0.13µm BiCMOS with Less Than 0.15dB Cross-Talk Penalty
[7.2] A 4×25Gb-28Gb/s 4.9mW/Gb/s -9.7dBm High-Sensitivity Optical Receiver based on 65nm CMOS for Board-to-Board Interconnects

Paper 7.1 Authors: *G. Kalogerakis, T. Moran, G. Denoyer, T. Nguyen*
Paper 7.1 Affiliation: *Finisar, Sunnyvale, CA*

Paper 7.2 Authors: *T. Takemoto[1], H. Yamashita[1], T. Yazaki[2], N. Chujo[2], Y. Lee[1], Y. Matsuoka[1]*
Paper 7.2 Affiliation: *[1]Central Research Laboratory, Hitachi, Tokyo, Japan [2]Yokohama Laboratory, Hitachi, Kanagawa, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY*

CONTEXT AND STATE OF THE ART

- The emergence of 100Gb/s Ethernet is driving an increasing need for integrated, high-sensitivity, and robust parallel optical interfaces.

TECHNICAL HIGHLIGHTS

- **Robust quad 25Gb/s TIA**
- In paper 7.1, Finisar demonstrates a quad 25Gb/s TIA in 0.13µm BiCMOS technology dissipating 270mW that uses a front-end single-ended to differential conversion to enable the achievement of a crosstalk penalty of just 0.15dB.
- **High sensitivity quad 25-28Gb/s TIA**
- In paper 7.2, Hitachi describes a quad 28Gb/s TIA in 65nm CMOS technology with the highest sensitivity (-9.7dBm) and widest eye opening (65%) at 25Gb/s reported to date. At 28Gb/s, the design achieves 4.8pJ/bit energy efficiency.

APPLICATIONS AND ECONOMIC IMPACT

- Robust and high sensitivity optical receivers in low-cost technologies will accelerate the adoption of 100Gb/s solutions, satisfying the ever-increasing demands for data-throughput in cloud servers and racks.

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Session 7 Highlights: Optical Transceivers and Silicon Photonics

[7.4] A Blind Baud-Rate ADC-Based CDR

Paper [7.4] Authors: *C. Ting, J. Liang, A. Sheikholeslami, M. Kibune, and H. Tamura*
Paper [7.4] Affiliation: *University of Toronto, Canada, and Fujitsu Laboratories, Japan*

Subcommittee Chair: *Ichiro Fujimori, Broadcom, Irvine, CA*

CONTEXT AND STATE OF THE ART

- Current ADC-based receivers with blind clock sample the received data at a rate higher than the data rate (typically by a factor of 2) in order to tolerate jitter and frequency offset between the received data and the blind clock.
- The oversampling of the data limits the maximum data rate that can be handled by these receivers

TECHNICAL HIGHLIGHTS

- **This paper is the first ever to report a baud-rate ADC-based receiver with blind clock**
- Researchers at the University of Toronto and Fujitsu Laboratories of Japan have invented a technique for wireline receivers that samples the incoming signal blindly at the data rate and yet recover the data without any errors (BER < 10-12).
- The new technique allows for extensive equalization of the received signal in digital domain.
- The new technique works even when the sampling rate of the ADC is below the actual data rate.

APPLICATIONS AND ECONOMIC IMPACT

- Architecture's dependence on only an ADC and synthesizable back-end logic improves design portability and will reduce time-to-market for new CDR realizations.

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Session 8 Overview: Millimeter-Wave Techniques

RF SUBCOMMITTEE

Session Chair: *Ullrich Pfeiffer, University of Wuppertal, Germany*
Session Co-Chair: *Gabriel Rebeiz, University of California, San Diego, CA*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France, RF Subcommittee*

Millimeter-Wave CMOS and SiGe BiCMOS transceivers for radar and imaging applications are becoming more complex with a higher level of integration and performance. Also, CMOS amplifiers and transmitters are continuously being pushed into the higher mm-Wave range (> 200GHz) using novel circuit- and power-combining techniques. The papers presented in this session focus on CMOS and BiCMOS systems-on-chip, LNAs, VCOs, transmitters and power amplifiers at mm-Wave frequencies.

- In Paper 8.1, the University of California, Irvine, presents a 210GHz transmit-receive chip with OOK modulation incorporating a 2x2 spatial-combining PA with integrated antennas and an EIRP of 5.13dBm, a fundamental frequency VCO, and an 18dB gain LNA in 32nm SOI CMOS.
- In Paper 8.2, Cornell University presents a high-power 260GHz radiation source with coupled-line oscillators and pulse-modulation capability in 65nm bulk CMOS technology. The chip achieves an output power of 1.1mW and an EIRP of 15.7dBm. When the radiation is modulated by narrow pulses, the measured output bandwidth is 24.7GHz.
- In Paper 8.3, the University of California, Davis, introduces a 260GHz 9.2dB-gain amplifier in a 65nm CMOS process. An output 1dB compression power of -5.5dBm, a saturated power of -3.9dBm and a peak PAE of 1.35% are measured at 255GHz.
- In Paper 8.4, Carnegie Mellon University and North Carolina State University show a 0.7W, fully integrated Q-band PA with 18.5dB gain and 10% PAE in 130nm SiGe BiCMOS. A 16-way combiner with low insertion loss and wideband impedance transformation is used. The 3dB output power bandwidth is 9GHz.
- In Paper 8.5, the University of California, Irvine, presents a 93-to-113GHz 9-element imaging system consisting of four 2x2 spatial-overlapping sub-arrays in 0.18um SiGe BiCMOS. The sub-arrays show a beam-steering angle of 18 degrees, a responsivity of 800MV/W, and an NEDT of 0.45K with 20ms integration time.
- In Paper 8.6, National Taiwan University demonstrates a 94GHz imaging radar using a 4-element beamforming transceiver in 65nm CMOS. Very fine 3D imaging is obtained by measuring the ToF using a variable counting clock. The system achieves 2m detection range and a 28-degree detection angle.
- In Paper 8.7, IHP, Silicon Radar, Karlsruhe Institute of Technology and the University of Paderborn show an integrated mixed-signal 120GHz FMCW/CW radar chipset in a 130nm SiGe BiCMOS technology. It features a harmonic transceiver, software linearization (SWL) circuits and a digital interface. The chip has been tested in a low-cost package with external antennas.
- In Paper 8.8, Ohio State University presents a 37.8GHz VCO optimized for minimal excess noise in a 130nm SiGe BiCMOS process. The VCO consumes 10mW, shows a 30% tuning range, and achieves an average phase noise and FOM_T at 1MHz offset of -103.6dBc/Hz and -193.5dBc/Hz, respectively.

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Session 8 Highlights : Millimeter-Wave Techniques

[8.2] A 260GHz Broadband Source with 1.1mW Continuous-Wave Radiated Power and EIRP of 15.7dBm in 65nm CMOS
[8.6] A 94GHz 3D Image Radar Engine with 4TX/4RX Beamforming Scan Technique in 65nm CMOS

Paper [8.2] Authors: Ruonan Han and Ehsan Afshari
Paper [8.2] Affiliation: Cornell University, Ithaca, NY, USA
Paper [8.6] Authors: P. Chen, P. Peng, C. Kao, Y. Chen, J. Lee
Paper [8.6] Affiliation: National Taiwan University, Taipei, Taiwan
Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- CMOS sources have generated 0.3mW at 288GHz and 420GHz as continuous wave sources.
- Phased-array receivers or transmitter front-ends with 4, 8 and 16 elements are available in CMOS and BiCMOS technologies at 60GHz, 77 to 85GHz, 94GHz and 110GHz. Single and two-element FMCW or pulse radars are available as systems-on-chip up to 150GHz.

TECHNICAL HIGHLIGHTS

- **The world's first CMOS source operating above 200GHz with an output power above 0dBm**
- A high-power 260GHz broadband radiation source with pulse-modulation capability in 65nm CMOS is reported. The source is integrated in an 8-element array resulting in 1.1mW radiated power and 5.7EIRP at 260GHz.
- **The world's first 4-element phased-array radar transceiver with short pulse-forming capabilities and integrated front-end and back-end decision electronics.**
  A 65nm CMOS radar system-on-chip is packaged in an LTCC module with high-efficiency antennas, and a radar demonstration is performed with high resolution imaging.

APPLICATIONS AND ECONOMIC IMPACT

- Compact and low-cost high-resolution sources approaching THz frequencies can be achieved using short-pulse radar systems-on-chip. Application areas include security systems, industrial monitoring and imaging.

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Session 9 Overview: Mobile Application Processors and Media Accelerators

ENERGY EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: *Michael Polley, Texas Instruments, Dallas, TX*
Session Co-Chair: *Yongha Park, Samsung, Yongin, Korea*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital*

This session presents three state-of-the art mobile application processors: the first features high-performance mobile multicore CPUs; the second features single-chip integration of applications and modem processing; and, the third features GPU-based fused multimedia processing. Additionally, five power-efficient media accelerators are presented to address next-generation video decoding, computational photography, and object recognition and classification for machine vision applications.

- In Paper 9.1, Samsung presents a 28nm high-κ metal-gate (HKMG) implementation of a heterogeneous dual-CPU configuration containing two quad-core CPU clusters, one cluster for high performance applications running at 1.8GHz with a 2MB L2, and the other used for highly energy-efficient operation running at 1.2GHz with 6× lower mW/MHz.
- In Paper 9.2, Renesas presents a 28nm high-κ metal-gate low-leakage CMOS bulk process implementation of a single-chip application processor with a dual-core 1.5GHz CPU integrated with a LTE/HSPA+ multimode-baseband modem processor, 2D/3D graphics accelerators, a power management unit and a low-leakage standby mode SRAM design.
- In Paper 9.3, National Chung Cheng University, the Industrial Technology Research Institute, National Chiao Tung University, Andes Technology and TSMC present an energy-efficient 0.48V 0.57nJ/pixel H.264 video-recording SoC in 65nm CMOS. The energy reduction is achieved using ultra-low voltage cell libraries, leakage-aware 8T-SRAM, in-situ performance monitors and pulsed variation-tolerant flip-flops.
- In Paper 9.4, Samsung presents a 32nm low-power high-κ metal-gate 72.5 GFLOPS GPGPU computing, 240Mpixels/s sustainable image processing and 60fps 1080p multi format codec capabilities are integrated with a 1.7GHz out-of-order execution dual core ARM v7A architecture CPU and a 12.8GB/s memory subsystem.
- In Paper 9.5, MIT and Texas Instruments present a video decoder implementation of the new High-Efficiency Video Coding (HEVC) draft standard. At 200MHz, the decoder achieves 249Mpixel/s, enabling Quad-Full HD resolution (3840×2160), while consuming 76mW at 0.9V.
- In Paper 9.6, MIT presents a 40nm CMOS reconfigurable processor for the new field of computational photography, providing high-dynamic range imaging, low-light enhancement and glare reduction offering two orders of magnitude improved energy efficiency compared with previous CPU and GPU solutions.
- In Paper 9.7, the University of Michigan presents an energy-efficient full-frame feature-extraction accelerator for micro-autonomous vehicle navigation in 28nm CMOS. Utilizing low-voltage operation at 470mV, the chip consumes only 2.7mW at 27MHz, while processing 640×480 30fps video input.
- In Paper 9.8, KAIST presents a 96% recognition accuracy multi-classifier many-core processor combining SIFT and HMAX machine vision algorithms. The 130nm mixed-mode CMOS chip consumes only 9.4nJ/pixel, operating on 30fps HD video.

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Session 9 Highlights : Mobile Application Processors and Media Accelerators

[9.1] 28nm High-κ Metal-Gate Heterogeneous Quad-Core CPUs for High-Performance and Energy-Efficient Mobile Application Processor
[9.2] A 28nm High-κ Metal-Gate Single-Chip Communications Processor with 1.5GHz Dual-Core Application Processor and LTE/HSPA+-Capable Baseband Processor
[9.4] 72.5GFLOPS 240Mpixel/s 1080p 60fps Multi-Format Video Codec Application Processor Enabled with GPGPU for Fused Multimedia Application

Paper 9.1 Authors: Y. Shin[1], K. Shin[1], R. Kashyap[2], H.-J. Lee[1], D. Seo[1], P. Kenkare[2], Y. Kwon[1], B. Millar[2], M.-S. Kim[1], R. Iyengar[2], A. Chowdhury[2], S.-I. Bae[1], I. Hong[1], W. Jeong[2], A. Lindner[2], U. Cho[1], K. Hawkins[2], J.-C. Son[1], S.-H. Hwang[1]
Paper 9.1 Affiliation: [1]Samsung Electronics, Yongin, Korea, [2]Samsung Electronics, Austin, TX
Paper 9.2 Authors: M. Fujigaya[1], N. Sakamoto[1], T. Koike[1], T. Irita[1], K. Wakahara[1], T. Matsuyama[1], K. Hasegawa[1], T. Saito[1], A. Fukuda[1], K. Teranishi[1], K. Fukuoka[2], N. Maeda[2], K. Nii[2], T. Kataoka[1], T. Hattori[1]
Paper 9.2 Affiliation: [1]Renesas Mobile, Tokyo, Japan, [2]Renesas Electronics, Tokyo, Japan
Paper 9.4 Authors: Y. Park, C. Yu, K. Lee, H. Kim, Y. Park, C. Kim, Y. Choi, J. Oh, C. Oh, J. Choi, G. Moon, J. Jang, J. Lee, Y. Shin, J. Son, C. Kim, S. Park,
Paper 9.4 Affiliation: Samsung Semiconductor, Yongin, Korea

Subcommittee Chair: Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital

CONTEXT AND STATE OF THE ART

- Demand for better user experience and all-day battery life in mobile devices has challenged the semiconductor industry to harness leading-edge process technologies and architectural innovations for application processors.

TECHNICAL HIGHLIGHTS

- **8 cores in two clusters on a single 28nm die suitable for both high performance and low power:**
- In Paper 9.1, Samsung presents a 28nm high-κ metal-gate (HKMG) implementation of a heterogeneous dual-CPU configuration containing two quad-core CPU clusters, one cluster for high performance applications running at 1.8GHz with a 2MB L2, and the other used for highly energy-efficient operation running at 1.2GHz with 6× lower mW/MHz.
- **Renesas presents a single-chip communications processor with a dual-core 1.5GHz CPU:**
- In Paper 9.2, Renesas presents a 28nm high-κ metal-gate low-leakage CMOS bulk process implementation of a single-chip application processor with a dual-core 1.5GHz CPU integrated with a LTE/HSPA+ multimode-baseband modem processor, 2D/3D graphics accelerators, a power management unit and a low-leakage standby mode SRAM design.
- **First ARM based mobile application processor with a full precision, advance feature GPGPU capability and a 10x energy-efficiency over CPU solution for fused multimedia application is presented.**

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- In Paper 9.4, Samsung presents a 32nm low-power high-κ metal-gate 72.5 GFLOPS GPGPU computing, 240Mpixels/s sustainable image processing and 60fps 1080p multi format codec capabilities are integrated with a 1.7GHz out-of-order execution dual core ARM v7A architecture CPU and a 12.8GB/s memory subsystem.

APPLICATIONS AND ECONOMIC IMPACT

- These processors and techniques will enjoy mainstream distribution in smartphones and tablets in 2014, enabling new levels of processing power and energy efficiency, improving the user experience and battery life. Beyond 2014, we expect this technology to become prevalent in other markets, including automotive, industrial and consumer.

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Session 10 Overview : Analog Techniques

ANALOG SUBCOMMITTEE

Session Chair: *Jafar Savoj, Xilinx, San Jose, CA*
Session Co-Chair: *Chris Mangelsdorf, Analog Devices, San Diego, CA*

Subcommittee Chair: *Bill Redman-White, University of Southampton, UK, Analog*

Analog technology continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. Entries span the range of filters, amplifiers, audio, and oscillators. New frontiers of precision, power, and performance are established.

- Paper 10.1 by University of Twente presents a 0.1-to-1.2GHz tunable 6th order channel-select filter in 65nm CMOS. It is based on N-path filters coupled with gyrators, achieving a flat pass-band and high out-of-band linearity. It has a NF of 2.8dB, gain of 25dB, and IIP3 of 26dBm. It consumes 11.7mA from a 1.2V supply.
- Paper 10.2 by Delft University of Technology presents a 65nm CMOS 7th-order discrete time IIR filter operating at up to 1GS/s sampling rate. The 3dB bandwidth is tunable between 400kHz to 30MHz and the stop-band rejection is 100dB. The IIP3 is +16dBm and the integrated noise is 12nV/sqrt(Hz). The filter consumes 2mW from a 1.2V supply.
- Paper 10.3 by Delft University of Technology presents an outside-the-rail chopper-stabilized opamp. It uses capacitive-coupling to achieve a 20V common-mode range and a multi-path architecture to obtain a smooth transfer function and a step response free of significant chopper-ripple. The opamp achieves 3μV offset, 148dB CMRR and consumes only 8μA from a 5V supply.
- Paper 10.4 by Toyohashi University of Technology and EIIRIS presents a 0.06mm2 current-feedback instrumentation amplifier with 32MHz GBW in a standard 0.18μm CMOS. The amplifier uses the chopper-stabilized technique and a novel digital calibration for ripple suppression. The fabricated chip achieves less than 3.5μV offset voltage, 13.5nV/ sqrt(Hz) input-referred noise and 194μA current consumption.
- Paper 10.5 by NXP Semiconductors presents a class-D audio amplifier with speaker protection in 0.14mm CMOS. A DC-DC booster provides 2.3W of output power to a 4W load. A protection algorithm running on an embedded DSP estimates membrane excursion and voice coil temperature using a speaker model that tracks the speaker impedance.
- Paper 10.6 by Broadcom and Oregon State University presents a stereo class-G headphone driver for battery-operated mobile devices. The circuit employs a hybrid output stage with an adaptive class-B control scheme to facilitate low quiescent current and low THD. The class-G headphone driver consumes 600mA/channel of quiescent current and achieves 108dB dynamic range, 62mW output power and 50mV pop-and-click noise.
- Paper 10.7 by Massachusetts Institute of Technology, Texas Instruments, and MediaTek presents a fully-integrated 18.5kHz RC time-constant-based oscillator in 65nm CMOS for sleep-mode timers in wireless sensors. A comparator offset cancellation scheme achieves 7x temperature stability improvement, leading to an accuracy of ±0.25% over −40 to 90°C and ±0.1% over 0 to 90°C. The oscillator has a long-term Allan stability of 20ppm or better for measurement intervals over 0.5s and consumes only 120nW.
- Paper 10.8 by KU Leuven, SCK-CEN, and KH Kempen presents a relaxation oscillator with the best reported effective Q-factor of 63,000 in 65nm CMOS. It employs a SC integrated error feedback to reduce the close-in phase noise and achieves a FOM of 154dB at 1kHz offset and consumes 82μA from a 1.2V supply. The frequency varies by only ±0.07% over a supply range of 1.1 to 1.5V. From 0 to 80°C, the total frequency variation is within ±0.82%.
- Paper 10.9 by Pohang University of Science and Technology and University of Michigan presents an all-digital MDLL for ultra-low-power sensor platforms with a leakage-based oscillator and a fast frequency acquisition scheme for intermittent operation of sensor node platforms. The MDLL is implemented in 65nm CMOS and consumes 423nW at 3.2MHz.

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Session 10 Highlights : Analog Techniques

[10.1] A 0.1-to-1.2GHz Tunable 6th-order N-path Channel-Select Filter with 0.6 dB Passband Ripple and +7dBm Blocker Tolerance

Paper Authors: *Milad Darvishi, Ronan van der Zee, Bram Nauta*
Paper Affiliation: *University of Twente, Enschede, the Netherlands*
Subcommittee Chair: *Bill Redman-White, Southampton University, UK*

CONTEXT AND STATE OF THE ART

- High-performance RF bandpass filters (BPF) play an important role in ensuring wireless transceivers are robust to out-of-band blockers.
- Designing an integrated BPF that simultaneously achieves satisfactory noise, linearity, tuning range, quality factor, and gain performance has proven challenging leading practical transceivers to employ bulky external surface acoustic wave (SAW) filters.

TECHNICAL HIGHLIGHTS

- **The first integrated filter that replaces external SAW-LNA filters in wireless transceivers and is tunable over a decade in frequency.**
- The first N-path filter that combines a suitable filter shape (0.6dB pass-band ripple), low noise figure (2.8dB), best-in-class out-of-band linearity (+26dBm wideband IIP3 and +7dBm 1dB blocker compression point B1dB,CP) and high stop-band rejection (59dB) while having +25dB gain.

APPLICATIONS AND ECONOMIC IMPACT

- The proposed filter can support multimode, multiband wireless applications. Furthermore, with this high-performance BPF, the bulky SAW filter may be replaced and the channel selection can be realized at RF, enabling more compact wireless terminals.
- This filter can be easily ported to advanced CMOS processes and can take advantage of scaled CMOS technologies to achieve better performance. Successful integration of the N-path filter can reduce the total BOM cost of a transceiver.

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Session 11 Overview : Emerging Memory and Wireless Technology

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan*
Session Co-Chair: *Shinichiro Mutoh, NTT, Tokyo, Japan*

Subcommittee Chair: *Hoi-Jun Yoo, KAIST, South Korea, Technology Directions*

With continuing technology scaling, enabling advances in computation, memory, and communication, energy-efficient memory and wireless communication will become even more important for ubiquitous mobility. This session introduces several emerging memory and wireless technologies enabling improved energy efficiency. Integration of non-volatile memory with logic for data retention, integration of a timing micro-system including crystal oscillators, and integration of NEMS resonators are some of the novelties that will be presented in this session. These technologies will impact computation, future short-distance communication for sensors, body area networks, mobile platforms, and industrial applications making mobile computing truly ubiquitous.

- In Paper 11.1, MIT presents a D-flip-flop with ferroelectric capacitor based non-volatile storage, enabling logic pipelines to be suspended and power-cycled without losing the state. The paper demonstrates a save-restore energy budget of just 3.4pJ/bit.
- In Paper 11.2, Tohoku University describes an MTJ-based logic-in-memory, parallel motion vector prediction accelerator implemented with cycle-based power gating, demonstrating 4X reduction in leakage power and 2X reduction in active power.
- In Paper 11.3, CSEM illustrates a novel timing micro-system achieving sub-microwatt power consumption in real-time clock mode, consuming only 0.1mW when the RC PLL is activated, and 10mW with BAW DCO activation.
- In Paper 11.4, Aalto University introduces a low-noise microwave amplification scheme using a nano-mechanical resonator. Injection of microwave induces a coherent stimulated emission and signal amplification.
- In Paper 11.5, Keio University presents the world's first 0.15mm-thick non-contact connector for Mobile Industry Processor Interface (MIPI) applications. A fully balanced pulse transmitter fabricated in 90nm CMOS technology consumes 1.5pJ/b and significantly suppresses EMI, allowing simultaneous two-channel communications.
- In Paper 11.6, KAIST presents a mono-phase pulse modulation inductive-coupling transceiver for mm-range board-to-board communication. Fabricated in 0.13μm CMOS, it demonstrates 1.2Gb/s data rate, and consumes 3.9pJ/b for the data transceiver and 0.73pJ/b for the clock transceiver at 1.2V.
- In Paper 11.7, Keio University describes an innovative application where a rotating shaft is equipped with sensors, wrapped in a 2D waveguide sheet with a retrodirective transponder array. The system beamforms the power to the wireless mobile sensors without battery or oscillator, and improves the power efficiency by 23X.

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Session 11 Highlights: Emerging Memory and Wireless Technology

[11.3] A Versatile Timing Microsystem based on Wafer-Level Packaged XTAL/BAW Resonators with sub-μW RTC Mode and Programmable HF Clocks

Paper [11.3] Authors: *David Ruffieux, Nicola Scolari, Frédéric Giroud, Thanh Chau Le, Silvio Dalla Piazza, Felix Staub, Kai Zoschke, Charles Alix Manier, Hermann Oppermann, Tommi Suni, James Dekker, Giorgio Allegato*
Paper [11.3] Affiliation: *CSEM, Neuchâtel, Switzerland, Micro Crystal AG, Grenchen, Switzerland, IZM, Berlin, Germany, VTT, Espoo, Finland, ST, Agrate Brianza, Italy*

Subcommittee Chair: Hoi-Jun Yoo, KAIST, South Korea

CONTEXT AND STATE OF THE ART

- Complex SoCs use multiple clock domains. Efficient clock generators are necessary. Miniature generic timing modules are needed in modern SoC systems.

TECHNICAL HIGHLIGHTS

- **A miniature generic timing microsystem relying on low frequency Quartz and BAW resonators to deliver clocks whose frequencies span a range from 32kHz to several tens of MHz has been implemented using vacuum sealing wafer level packaging technologies.**
- The system achieves sub-uW power dissipation in RTC mode, 0.1mW when a 1 to 50MHz programmable clock obtained with a RC PLL is generated and 10mW when low jitter clocks are derived after fractional division of the signal obtained from a BAW DCO.

APPLICATIONS AND ECONOMIC IMPACT

- Although continuously challenged by the buzz raised by silicon resonators counterparts over recent years, quartz still dominates the timing market with several billion units sold yearly.
- Traditional quartz packaging technologies have reached the miniaturization limits. Wafer scale packaging technologies that attracted the attention to silicon resonators can readily be applied to quartz to set forth the miniaturization pace.

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Session 11 Highlights: Emerging Memory and Wireless Technology

[11.5] A 0.15mm-Thick Non-Contact Connector for MIPI using Vertical Directional Coupler
[11.6] 1.2Gb/s 3.9pJ/b Mono-Phase Pulse Modulation Inductive Coupling Transceiver for mm-range Board-to-Board Communication

Paper [11.5] Authors: Wataru Mizuhara, Tsunaaki Shidei, Atsutake Kosuge, Tsutomu Takeya, Noriyuki Miura, Masao Taguchi, Hiroki Ishikuro, and Tadahiro Kuroda
Paper [11.5] Affiliation: *Keio University, Japan*
Paper [11.6] Authors: *Hyunwoo Cho, Unsoo Ha, Taehwan Roh, Dongchurl Kim, Jaehyuck Lee, Yunje Oh, and Hoi-Jun Yoo*
Paper [11.6] Affiliation: *KAIST and Samsung, South Korea*

Subcommittee Chair: Hoi-Jun Yoo, KAIST, South Korea

CONTEXT AND STATE OF THE ART

- Progress continues in the close-range communication field using distributed transmission and inductive coupling technologies.

TECHNICAL HIGHLIGHTS

- **"Non-contact connector" technologies achieve record speed and energy efficiency**
- The world's first 0.15mm-thick non-contact connector for Mobile Industry Processor Interface (MIPI) applications shows a vertical directional coupler with 20dB directionality and a fully balanced pulse transmitter that is fabricated in 90nm CMOS technology. This transmitter consumes 1.5pJ/b and suppresses EMI.
- An inductive coupling interface for mm-range board-to-board data communication with a new mono-phase pulse modulation achieves record low energy consumption of 3.9pJ/b and 1.2Gb/s data rate.

APPLICATIONS AND ECONOMIC IMPACT

- Short-range communications technologies enable better reliability and lower manufacturing cost than traditional mechanical connectors for applications like Mobile Industry Processor Interface (MIPI).

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Session 12 Overview: Non Volatile Memory Solutions

MEMORY SUBCOMMITTEE

Session Chair: Jin-Man Han, Samsung, Korea
Session Co-Chair: Daniele Vimercati, Micron, Italy

Subcommittee Chair: Kevin Zhang, Intel, Hillsboro, OR

While the scaling of conventional nonvolatile memories is slowing, emerging memory technologies are starting to show significant technological progress. At the same time, new circuit techniques for existing nonvolatile memories are being introduced to improve reliability and system performance. The papers in this session highlight various technologies from devices to systems, each paper providing potential solutions to its unique challenges.

- In Paper 12.1, Sandisk and Toshiba presents a 32Gb ReRAM test chip developed in 24nm process, with a diode as the selection device. Die efficiency is maximized by utilizing area under the array for supporting circuitry and by sharing wordlines and bitlines between adjacent blocks.
- In Paper 12.2, Renesas Electronics presents the first-ever 40nm embedded SG-MONOS Flash macros for automotive applications. A SG-MONOS cell, a split-gate memory cell with charge-trapping storage, and three circuit techniques realize random-read access to the code macros at 5.1GB/s. The memory is reliable even at a junction temperature of 170°C.
- In Paper 12.3, Keio University presents an inductive-coupling wake-up transceiver able to reduce by 500× the standby power consumption of non-contact memory cards. The transceiver consumes 6nW standby power with 50×50 m^2 of silicon area in 0.18 m CMOS technology.
- In Paper 12.4, Infineon presents a time-differential-sensing scheme for spin-torque-transfer (STT) MRAM that significantly reduces mismatch effects. This allows the bitline voltage to be reduced to 80mV, increasing the read window with only 23ns read time and 1.1V supply voltage.
- In Paper 12.5, Micron presents the first ever 128Gb 3b/cell NAND Flash design using 20nm planar cell technology. The planar cell allows the memory cell to be scaled in both the wordline and bitline directions, resulting in the smallest 3b/cell memory device to date. The sensing scheme is able to detect hard and soft states, based on a novel ramping technique.
- In Paper 12.6, Panasonic presents an ReRAM filament-scaling forming technique and level-verify-write scheme with endurance over 10^7 cycles for a 16nm cell. It is realized within a 1T1R ReRAM array. A 2-step forming circuit with self-consistent and current-limiting schemes in 0.11μm technology and 256Kb array is presented.
- In Paper 12.7, Macronix presents a 45nm 6b/cell charge-trapping Flash memory using LDPC-based ECC and drift-immune soft-sensing engine. Using multiple techniques the cell is boosted up to 6b/cell and no error remains after LDPC decode over a 10-year lifetime.
- In Paper 12.8, TSMC presents a cycling-endurance optimization scheme for 1Mb STT-MRAM in 40nm technology with a dynamic load balance circuit. It improves endurance by maintaining uniform voltage and current across the MTJ and proves a 100K cycling without yield loss.
- In Paper 12.9, Chuo University, Japan, presents a solid-state storage architecture that merges NAND Flash memory and ReRAM targeted at big-data applications. The system tolerates a 32× higher BER from the NAND cells by using techniques of reverse-mirroring, error-reduction synthesis, page-RAID, and error-masking.

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Session 12 Highlights : Non Volatile Memory Solutions

[12.1] A 130.7mm^2 2-Layer 32Gb ReRAM Memory Device in 24nm Technology

Paper Authors: Tz-Yi Liu, et al.
Paper Affiliation: Sandisk, Toshiba
Subcommittee Chair: Kevin Zhang, Intel, Hillsboro, OR

CONTEXT AND STATE OF THE ART

- Emerging nonvolatile memories (NVMs) such as PRAM, ferroelectric RAM (FeRAM), MRAM, and ReRAM are all targeting high cycling capability and lower power per bit in read/write. But so far, none of the emerging NVMs have achieved memory density on a par with state-of-the-art NAND flash memory.
- The highest density for a single chip published at last year's ISSCC is 64Mb for ReRAM and 8Gb for PRAM, while NAND can reach up to 128Gb.

TECHNICAL HIGHLIGHTS

- **The Highest density in ReRAM developments: 32Gb with the chip size of 130.7mm2**
- MeOx-based ReRAM is based on 24nm technology node with a diode as the selection device and a 2-layered architecture.
- Many circuits are placed underneath the array, including the selection transistor or decoder, bias-control circuit, sense amplifier, page buffer, read/write control circuit and voltage regulator drivers, improving the array efficiency.

APPLICATIONS AND ECONOMIC IMPACT

- With the density of 32Gb on a single chip, ReRAM now has the opportunity to be adopted as a storage-class memory competing with the existing NAND Flash memories for nonvolatile mass storage applications.
- The Flash memory market size is over $20 billion USD and is expected to be growing faster than any other memory markets in the foreseeable future. Storage-class ReRAM can capture a significant portion of the Flash memory market.

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Session 13 Overview: High-Performance Wireless

WIRELESS SUBCOMMITTEE

Session Chair: *Brian Floyd, North Carolina State University, Raleigh, NC*
Session Co-Chair: *Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan*

Subcommittee Chairs:
David Su,Qualcomm Atheros, San Jose, CA, Wireless Subcommittee
Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee

There are a variety of emerging applications for short-range, high-bandwidth, high-frequency integrated systems. One such area is multi-Gb/s short-range communications at 60GHz. For this market to succeed, highly integrated energy-efficient beamformer, transceiver, and baseband solutions are required. The first five papers in this session present state-of-the-art solutions for mm-Wave radios. Another promising market is low-cost, high-performance radar and radio solutions that can benefit from silicon integration and mixed-signal architectures. The second part of this session contains two wideband radar chips, one for medical imaging and the other for short-range remote monitoring, as well as a channel-combining digital satellite IC.

- In Paper 13.1, Panasonic presents the first 60GHz transceiver chipset for WiGig/IEEE802.11ad. The radio achieves 1.8Gb/s MAC throughput while consuming 788mW (TX) and 984mW (RX), and incorporates both mm-Wave front-end and full digital backend in 90nm and 40nm CMOS respectively.
- In Paper 13.2, the University of California, Berkeley, University of Nice and STMicroelectronics present a 4x2 60GHz beamforming transmitter using a quadrature spatial combining technique and digitally-modulated power amplifiers. The transmitter in 65nm CMOS achieves 6Gb/s 16QAM data with average PA efficiency of 16.5% at 6dB power back-off.
- In paper 13.3, the University of California, Berkeley describes a 60GHz phased-array transceiver in 65nm CMOS with four on-chip antennas each with multiple drive points, enabling >10Gb/s communication over 40cm.
- In paper 13.4, imec, Vrije Universiteit Brussel and Panasonic present a four-element 60GHz transceiver chipset employing analog baseband beamforming in both receive and transmit mode. The chipset in 40nm CMOS achieves 2.3Gb/s communication over 3.5meters.
- In paper 13.5, the University of California, Berkeley presents a 65nm CMOS equalizer for a 60GHz baseband using a mixed-signal architecture to reduce power consumption. The chip employs 32-tap feedforward equalization plus 100-tap decision-feedback equalization, consumes 65mW, and has been demonstrated at data rates up to 8Gb/s.
- In paper 13.6, the University of Padova demonstrates a 65nm CMOS radar transceiver for breast cancer diagnostic imaging. The stepped-frequency radar operates over 2 to 16 GHz, consumes 204mW, and achieves 3mm in-body resolution with 107dB dynamic range.
- In paper 13.7, National Tsing Hua University describes a 65nm CMOS impulse radar receiver. The chip supports 15GHz instantaneous bandwidth and employs direct sampling at an equivalent rate of 130GS/s to allow precise time-of-arrival measurements.
- In paper 13.8, NXP Semiconductors describes a 45nm CMOS single-chip, mixed-mode IC that combines 14 parallel satellite channels over the 250MHz to 760MHz band, and reorders and multiplexes them onto a single wire in the 950-to-2150MHz band.

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Session 13 Highlights : High-Performance Wireless

[13.1] A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications

Paper Authors: *T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, N. Saito*
Paper Affiliation: *Panasonic, Yokohama, Japan*
Subcommittee Chairs:
David Su, Qualcomm Atheros, San Jose CA, Wireless Subcommittee
Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee

CONTEXT AND STATE OF THE ART

- 60GHz has been an area of intense research for the past decade with multiple silicon demonstrations of receivers, transmitters, and phased arrays.
- The WiGig/IEEE802.11ad standard is now finalized and the market is ready to launch.

TECHNICAL HIGHLIGHTS

- **First 60GHz chipset for new WiGig/IEEE 802.11ad multi-Gb/s standard**
- This paper presents a fully-integrated standard-compliant 60GHz radio chipset including a transceiver chip and digital baseband chip, and has been used to demonstrate a 1.5Gbps link at 1m.
- Sophisticated frequency-dependent digital calibration is included within a power-efficient baseband signal processor.

APPLICATIONS AND ECONOMIC IMPACT

- 60-GHz radio chipsets can enable data-rate-intensive applications (wireless docking, ultra-fast sync-n-go, wireless video streaming) and can find widespread use in handset, laptop, and consumer electronic devices.
- Standard-compliant solutions allow rapid uptake of the technology.

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Session 14 Overview : Digital PLLs and Building Blocks

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Anthony Hill, Texas Instruments, Dallas, TX*
Session Co-Chair: *Atsuki Inoue, Fujitsu, Kawasaki, Japan*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital*

The nine papers presented in this session highlight developments in clock generation and distribution, on-die sensors, cross-die communication, and timing margin recovery. These designs implement functions traditionally constructed with analog techniques, but now leveraging digital architectures to improve PVT tolerance, area, power efficiency, and enable rapid process migration and technology adoption.

- In Paper 14.1, the Tokyo Institute of Technology presents a 0.022mm2 970mW dual-loop injection-locked PLL implemented in 65nm CMOS and using all-digital PVT-calibration circuits. The small area is achieved using a TDC-less digital FLL with injection-locking. The PLL uses both a main loop and a replica loop for PVT tracking resulting in 0.7ps RMS jitter.
- In Paper 14.2, Seoul National University and Samsung present a 0.032mm2 3.1mW synthesized pixel-clock generator in 28nm CMOS based on an all-digital dual-loop PLL. The 250MHz pixel clock is generated from a 100kHz input and exhibits 30psRMS jitter. The synthesized DCO shows 0.37ps resolution and 1.8LSB differential non-linearity, with a PVT-compensated wide tuning range (10 to 630MHz) and locks within 120 input cycles.
- In Paper 14.3, Infineon Technologies presents a CMOS digital PLL, which uses random modulation to generate a spread-spectrum clock (SSC). It reduces accumulated jitter by 8× with respect to an equivalent triangular modulation without penalty in EMI reduction. The DPLL is implemented in 65nm CMOS, occupies 0.23mm2, and draws 5mA at 500MHz output.
- In Paper 14.4, Samsung Electronics presents a 28nm CMOS digital PLL, which introduces a phase-interpolating phase-to-digital converter, calibration-free DSM noise canceller and supply-insensitive DCO. The DPLL occupies 0.026mm2 and consumes 2.2 to 5.3mW at 1-to-2GHz output frequencies. Measured RMS integrated jitter in integer mode is 20ps and in fractional mode is 26ps.
- In Paper 14.5, Oregon State University presents a digital clock multiplier targeting mobile SoC platforms and servers. It achieves rapid turn-on by accurate frequency presetting and reference insertion. Fabricated in a 90nm CMOS process, the prototype achieves 2psRMS jitter, while consuming 2.2mW/25μW on/off-state power from a 1.1V supply with 12pJ energy overhead due to power cycling at 2.5GHz output frequency.
- In Paper 14.6, Keio University presents a 0.18μm 3D wireless clock system which distributes a 1.1GHz clock across stacked chips using vertically-coupled LC oscillators and horizontally-coupled ring oscillators. Clock skew is <18ps for a 1.8V supply, and <25ps for a 0.9V supply, with RMS jitter <1.72 ps. The proposed frequency-locking and phase-pulling scheme widens the lock range to ±10% at a power dissipation of 196mW at 0.9V.
- In Paper 14.7, KAIST presents a 0.13μm 1.2V CMOS distributed digital-thermal sensing network. This design combines a small number of accurate thermal sensors with a large number of tiny relative thermal sensors, achieving an average area of 2578μm2 per sensing point. By combining these sensor outputs, a thermal-map up-sampler synthesizes a higher-spatial-resolution thermal map. Silicon results demonstrate an average error of 0.2°C over a sensing area of 3.24mm2 resulting in a 57.7% area reduction versus prior art.
- In Paper 14.8, Pohang University, Samsung and the University of Michigan describe a current-mode transceiver for on-chip global interconnects, implemented by series stacking of a current-sensing load as the receiver and an open-drain driver as the transmitter. The transceiver is fabricated in 65nm CMOS and achieves 95fJ/b at 3Gb/s and 0.9V and 108fJ/b at 4Gb/s and 1.0V over a 10mm link with a BER of less than 1E-12.
- In Paper 14.9, The University of Michigan introduces “Razor-Lite” for timing-margin recovery. This approach reduces area and energy overhead of previous error-detection and correction schemes using a simple 8-transistor

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transition detector integrated in a flip-flop. This is done with an energy/area overhead of 2.7%/33%. The technique is validated in a 45nm SOI 7-stage pipeline Alpha processor, showing energy efficiency gains of 83% over a baseline design at 1.2GHz and 1.1V, with 4.42% core area overhead.

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Session 14 Highlights : Digital PLLs and Building Blocks

[14.1] A 0.022mm2 970µW Dual-loop Injection-Locked PLL with -243 dB FOM Using Synthesizable All-Digital PVT Calibration Circuits

[14.5] A 2.5GHz 2.2mW/25µW On/Off-State Power, 2psRMS-Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time

Paper 14.1 Authors: *W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, A. Matsuzawa*
Paper 14.1 Affiliation: *Tokyo Institute of Technology, Tokyo, Japan*
Paper 14.5 Authors: *T. Anand, M. Talegaonkar, M. Elshazly, B. Young, P. Hanumolu*
Paper 14.5 Affiliation: *Oregon State University, Corvalis, OR*
Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital*

CONTEXT AND STATE OF THE ART

- Phase-locked loops (PLLs) and frequency-locked loops (FLLs) provide the heartbeat of all processors – from mobile/handheld to large compute farms in data centers. No modern microprocessor could be constructed without them.
- Historically, PLLs for high-performance and mobile processors were built with analog components. This often required custom fabrication steps and lengthy silicon debug cycles. The emergence of digital PLLs is driving cost reduction in modern processors as they eliminate many custom steps and components. Digital implementations also enable rapid exploitation of cutting-edge process technologies.
- Power optimization of modern processors is critical to maximizing battery life. The development of digital PLLs has directly led to power reduction in processors ,which extends battery life and gives consumers more for less. Digital PLLs offer up to 10× power and area improvement over analog PLLs.

TECHNICAL HIGHLIGHTS

- **Tokyo Institute of Technology presents a 0.022mm2 970mW dual-loop injection-locked PLL.**
- The hybrid PLL is implemented in 65nm CMOS and uses all-digital PVT-calibration circuits. The small area is achieved using a TDC-less digital FLL with injection-locking. The PLL uses both a main loop and a replica loop for PVT tracking, resulting in 0.7psRMS jitter.
- **Oregon State University presents a 90nm digital-clock multiplier with a 3-reference-cycle lock time for mobile SoC platforms and servers**
- The design achieves 2psRMS jitter, while consuming 2.2mW/25mW on/off-state power from a 1.1V supply with 12pJ energy overhead due to power cycling at 2.5GHz output frequency. The rapid turn-on is achieved by accurate frequency presetting and reference-edge insertion. This enables devices to quickly enter or exit sleep modes, resulting in further power savings and faster device response time.

APPLICATIONS AND ECONOMIC IMPACT

- Low-jitter digital PLLs are a key enabler to reduce cost and make complex devices more widely available to consumers. They enable rapid adoption of new technologies and ever-improving consumer devices.

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- This class of digital phase-locked loops will enable future integration of more complex systems on a chip.

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[14.8] A 95fJ/b Current-Mode Transceiver for 10mm On-Chip Interconnect

Paper 14.8 Authors: *S.-K. Lee[1,2], S.-H. Lee[1], D. Sylvester[3], D. Blaauw[3], J.-Y. Sim[1]*
Paper 14.8 Affiliation: *[1]Pohang University of Science and Technology, Pohang, Korea, [2]Samsung, Hwasung, Korea, [3]University of Michigan, Ann Arbor, MI*
Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital*

CONTEXT AND STATE OF THE ART

- The number of processing cores in modern SOCs and microprocessors is increasing as power requirements limit higher clock frequencies.
- Efficient core-to-core communications is becoming important for reducing the energy and performance overhead of parallel operations in multi-core processors.
- Process scaling to nanometer technologies is increasing the wire delay. This requires innovation with fast but energy-efficient on-chip-interconnect architectures.

TECHNICAL HIGHLIGHTS

- **Pohang University, Samsung and the University of Michigan describe a 65nm low-power transceiver for on-chip global interconnects**
- The transceiver is fabricated in 65nm CMOS and achieves 95fJ/b at 3Gb/s and 0.9V, and 108fJ/b at 4Gb/s and 1.0V over a 10mm link with a BER of less than 1E-12. This design uses a pre-emphasis open-drain wire driver with a current-sensing, active inductor device stack in the wire receiver.

APPLICATIONS AND ECONOMIC IMPACT

- Energy-efficient core-to-core communications enables products to satisfy increasing consumer demand for mobile functionality through multi-core architecture.
- Higher energy efficiency in data communications reduces power and extends battery life in mobile applications.

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Session 15 Overview: Data Converter Techniques

DATA CONVERTERS SUBCOMMITTEE

Session Chair: Michael Perrott, Masdar Institute of Technology, Abu Dhabi, UAE
Session Co-Chair: Geert van der Plas, IMEC, Heverlee, Belgium

Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

Data converters are critical building blocks for a wide variety of applications. The papers in this session demonstrate improved resolution and power efficiency for data converters in technology spanning from 0.6μm BiCMOS to 28nm CMOS. The first paper brings new levels of energy efficiency to wideband continuous-time $\Delta\Sigma$ data converters in scaled technology. SAR converters, known for their extreme energy efficiency, are now able to achieve the high resolution claimed by pipeline ADCs. Incremental ADCs achieve high resolution and low power consumption. A static output DAC achieves low noise and sub-ppm INL. These improvements impact a wide range of applications, including next-generation wireless transceivers, ultra-low-power sensors, and advanced medical-imaging systems.

- In Paper 15.1, MediaTek presents a continuous-time $\Delta\Sigma$ ADC in 28nm CMOS that achieves a peak SNDR of 73.6 dB within an 18MHz bandwidth. 27.7fJ/conv-step energy efficiency is obtained using a highly digital multibit, input-tracking quantizer with embedded feedback to compensate for finite opamp bandwidth and excess loop delay.
- In Paper 15.2, Eindhoven University of Technology demonstrates <3 fJ/conv-step power efficiency with a SAR design operating at 0.6V in 65nm CMOS. The converter can be configured for 10b or 12b operation at 40kS/s. A data-driven technique utilizes multiple comparator operations to reduce the impact of comparator noise.
- In Paper 15.3, Panasonic utilizes enhancement techniques such as dithering and adaptive averaging to achieve 71dB SNDR (at low input frequencies) with a 50MS/s SAR structure. Implemented in 90nm CMOS, this converter consumes only 4.2 mW.
- In Paper 15.4, Delft University of Technology introduces an asynchronous incremental ADC in 0.16mm CMOS featuring switched-capacitor zero-crossing-based integrators. 14b resolution is achieved in a conversion time of less than 1ms, drawing only 20mA from a 1V supply.
- In Paper 15.5, Yonsei University (with Delft University of Technology) presents an incremental ADC in 0.16mm CMOS that utilizes a second-order discrete-time $\Delta\Sigma$ loop to digitize the residue of a 6b SAR quantizer. 21b resolution is achieved with 1mV offset at a power consumption of 6.3mW.
- In Paper 15.6, Analog Devices demonstrates a DAC for low frequency signals at 20b resolution with a noise performance of 7.5nV/√Hz above 10Hz and a stability of 0.05ppm/°C. Code-dependent calibration enables sub-ppm INL, and the structure provides a ±10V output range in 0.6mm BiCMOS with a settling time of 1ms.
- In Paper 15.7, National Tsing Hua University utilizes a SAR architecture in 90nm CMOS to achieve scalable operation from 0.5 to 4 MS/s from a supply voltage of 0.4 to 0.7 V while maintaining an SNDR greater than 54 dB. A charge average switching DAC enables an energy efficiency between 2.4 and 5.2fJ/conversion-step across these operating conditions.
- In Paper 15.8, Asahi Kasei Microdevices (with UCSD) leverage an auxiliary amplifier stage to provide nonlinear correction and noise cancellation to achieve 73.3dB SNDR in a 14b pipelined ADC running at 60MS/s. The chip is implemented in 0.18mm CMOS and consumes 68mW from a 1.6V supply.

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Session 15 Highlights : Data Converter Techniques

[15.1] A 28 fJ/conv-Step CT DS Modulator with 78dB DR and 18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer

Paper Authors: Y-S Shu, J. Tsai, P. Chen, T. Lo, and P. Chiu
Paper Affiliation: MediaTek, Hsinchu, Taiwan
Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

CONTEXT AND STATE OF THE ART

- More advanced CMOS technology nodes have smaller transistors with degraded analog performance parameters such as gain and linearity, which makes it increasingly difficult to realize accurate data converters. This paper shows a continuous-time ΔΣ ADC with state-of-the-art power efficiency in an advanced 28nm CMOS technology, defying the perceived difficulties of design in such advanced process nodes.

TECHNICAL HIGHLIGHTS

- **This 28nm CMOS continuous-time ΔΣ modulator achieves 18MHz bandwidth, 78dB dynamic range, and 73.6dB peak SNDR while using 3.9mW of power and occupying only 0.08mm2, achieving an unprecedented figure-of-merit of 28fJ/conversion-step among comparable oversampling modulators.**
- The ΔΣ ADC incorporates a low-power multi-bit quantizer with input-tracking power-on control that consumes only 0.3mW at 640MS/s, a result that has not been achieved in the prior art.

APPLICATIONS AND ECONOMIC IMPACT

- This paper demonstrates a power-efficient and compact ΔΣ ADC that helps to achieve the next milestone by scaling down the power and cost of a variety mobile devices (such as smartphones and tablets) that rely of high-bandwidth, high-fidelity oversampling converters.

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Session 16 Overview : Biomedical Circuits & Systems

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Chair: *Firat Yazicioglu, imec, Belgium*
Session Co-Chair: *Taechan Kim, Samsung, Korea*

Subcommittee Chair: *Roland Thewes, TU Berlin, Germany, IMMD*

This session presents the most recent advances in continuous monitoring of patients, efficient electrical therapy delivery, and increasing efficiency and speed of diagnostics. The first four papers focus on neural interfaces and circuits for power-efficient acquisition and processing of neural signals. A closed-loop system for detection of epilepsy and suppression through electrical stimulation is demonstrated. A high-density neural probe with large number of recording sites demonstrates the use of active electrodes for reducing cross-talk. Low-voltage IC design techniques minimize the power dissipation, and activity-dependent signal conversion improves system power efficiency. Two papers focus on epiretinal prostheses where high-voltage compliance and generation of an accurate stimulation current is demonstrated. Another two papers focus on implants and continuous monitoring of patients. A high-precision bio-impedance measurement circuit is presented for intra-cardiac signal monitoring, and a complete system for continuous glucose measurements is introduced.

- In Paper 16.1, National Chiao Tung University (with National Cheng Kung University) presents a fully integrated closed-loop seizure-control SoC that embeds seizure detection, adaptive neural stimulation, and wireless power transmission. The chip occupies less than 14mm2 and dissipates 2.8mW
- In Paper 16.2, imec (with KU Leuven) presents a CMOS neural probe that consists of a shank (100μm wide, 10mm long, 50μm thick) with 455 active electrodes and a body (2.9×3.3mm2) with 52 readout channels including a 25Mb/s digital interface. An input-referred noise of 3.2μVrms and a total power consumption of 925μW are achieved.
- In Paper 16.3, Nanyang Technological University (with Institute of Microelectronics and National University of Singapore) presents a power-efficient neural-recording architecture with two-level supply voltage and dynamic range folding. The implemented 100-channel recording IC includes analog front-ends with 3.2μVrms input noise, ADCs with 8.2b ENOB at 200kS/s, and power-management circuits. The whole recording chain consumes less than 1μW/channel.
- In Paper 16.4, imec (with University of Amsterdam) presents a complete 24-channel wireless neural recording system enabled by a custom IC showing less than 3.5μVrms noise (AP/LFP band) and >70dB CMRR. By transmitting only the action potential (AP) data, power consumption is scaled based on neural activity. By detecting an AP event prior to digitization, the ASIC can power-gate all subsequent stages and yet transmit the entire AP shape to facilitate classification.
- In Paper 16.5, UCLA presents an SoC for retinal prostheses capable of receiving 100mW power at a voltage conversion efficiency of 83% and a 2Mb/s data rate at a BER less than 10-7. The 1024-channel stimulator array supports ±10V output compliance voltage and is expandable to 4096 channels by chip clustering.
- In Paper 16.6, CalTech (with the Doheny Eye Institute and the University of Southern California) presents an epiretinal prosthesis that doubles the number of channels of previous designs to 512 and reduces the pixel size by 66% to 0.0169mm2. It uses a new digital self-calibration technique to match biphasic stimulation currents.
- In Paper 16.7, Sensors for Medicine and Science (with Zentrum Mikroelectronik) presents a remotely powered, dual-channel micro-fluorimeter for use in long-term, implantable biosensor applications. The wireless sensor system is powered through a 13.56MHz carrier and uses NFC for transdermal communication. The system achieves a resolution of less 0.1K and 10pA for the temperature and current sensors, respectively.
- In Paper 16.8, CalTech presents a fully integrated CMOS magnetic spectrometer that can detect, quantify, and characterize magnetic materials within a 1.1-to-3.3GHz frequency range. The sensor consumes <2mW, requires no external biasing magnetic fields, and can be powered and operated completely from a USB interface.

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- In Paper 16.9, imec (with Olympus) presents a 20μW intra-cardiac signal-processing IC for accurate R-peak extraction for VF analysis and bio-impedance sensing. A 2ms group delay, 2.3μW programmable QRS band power feature extractor is implemented. A 16-level digitally synthesized pseudo-sinusoidal current generator ensures to extract bio-impedance in the range of 0.1Ω-4.4kΩ with 35mΩ resolution and higher than 97% accuracy.

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Session 16 Highlights: Biomedical Circuits & Systems

[16.1] A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic SoC for Real-Time Epileptic Seizure Control

[16.7] A Near Field Communication (NFC) Enabled Wireless Fluorimeter for Fully Implantable Biosensing Applications

Paper [16.1] Authors: *W. M. Chen et al.*
Paper [16.1] Affiliation: *National Chiao Tung University, Hsinchu, Taiwan*
Paper [16.7] Authors: *A. DeHennis, M. Mailand, D. Grice, S. Getzlaff, and A. Colvin*
Paper [16.7] Affiliation: *Sensors for Medicine and Science, Germantown, MD, and Zentrum Mikroelektronik, Dresden, Germany*
Subcommittee Chair: *Roland Thewes, TU Berlin, IMMD*

CONTEXT AND STATE OF THE ART

- Seizure-triggered, feedback electrical stimulation has been proven to be a promising therapy delivery to effectively suppress pathological brain activities. However, devices with accurate detection and effective stimulation for real-time seizure control are still unavailable.
- Continuous measurement of glucose levels may increase the therapy efficiency for diabetic patients. However, current solutions are all invasive and suffer from short lifetime in the case of continuous monitors.

TECHNICAL HIGHLIGHTS

- **A fully integrated closed-loop epileptic seizure control system-on-chip with seizure detection and adaptive neural stimulation is presented. The chip is powered and configured wirelessly enabling fully implantable seizure detection.**
- **A remotely powered, dual channel, micro-fluorimeter is presented for use in long-term implantable biosensor applications. The IC is packaged with a flip-chip-mounted LED, and a ferrite antenna for a fully implantable glucose-monitoring system that uses less than 1mJ per measurement.**

APPLICATIONS AND ECONOMIC IMPACT

- Epilepsy is one of the most common neurological disorders, affecting more than 50 million people worldwide and costing more than $15B in the US alone. The presented integrated circuit implements a means to detect the onset of epileptic activity and to suppress a seizure electrically in a closed-loop configuration. The device is demonstrated on rodents, showing effective suppression of epileptic seizures.
- The cost of diabetes in the US exceeds more than $170B. The glucose-monitoring system is an important step towards closed-loop systems for improved diabetes treatment.

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Session 17 Overview: High-Performance DRAM Interfaces

MEMORY SUBCOMMITTEE

Session Chair: *Yasuhiro Takai, Elpida Memory, Sagamihara, Japan*
Session Co-Chair: *James Sung, Etron, Hsinchu, Taiwan*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR*

Increasing demand in high-performance computing in both data server and consumer electronics are the key drivers to power the growth of the semiconductor industry. DRAMs in today's computing systems need to be operated at higher speed in data transmission with lower power consumption. DRAM interfaces are becoming the key focus area for future scaling. In this session, we will have four papers that address novel transceiver design and advanced clocking schemes to achieve higher data rate and lower power while meeting reliability requirements.

- In Paper 17.1, Rambus discloses a 6.4Gb/s near-grounded single-ended low-common mode transceiver for a dual-rank memory interface systems with better than 9.1mW/Gb/s controller power efficiency.
- In Paper 17.2, Pohang University of Science and Technology reveals up to 27% transceiver power reduction in a single-ended point-to-point DRAM interface by increasing the termination resistance to 4×Zo at both ends of TX and RX.
- In Paper 17.3, IBM Zurich Research presents a 5.7mW/Gb/s power-consumption efficiency 24-to-240Ω 1.6Gb/s thin-oxide DDR transmitter with a 4b resolution 1.9-to-7.6V/ns clock-feathering slew-rate control in 22nm CMOS.
- In Paper 17.4, Korea University describes an adaptive-bandwidth PLL for over 10Gb/s/pin and 0.78UI data eye opening for a 1.5V graphics DRAM interface in 65nm CMOS.

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Session 17 Highlights : High-Performance DRAM Interfaces

[17.1] A 6.4-Gb/s Near-Ground Single-Ended Transceiver for Dual-Rank DIMM Memory Interface Systems

Authors: *K. Kaviani, M. Bucher, B. Su, B. Daly, B. Stonecypher, W. Detloff, T. Stone, R. Kollipara, Y. Lu, C. Madden, J. Eble and L. Luo*
Affiliation: *Rambus., Sunnyvale, CA*
Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR*

CONTEXT AND STATE OF THE ART

- 3.2Gb/s/pin DDR4 was introduced at ISSCC 2012 as the leading DRAM interface for main memory, and its DIMM systems are expected to be used as main memories for both PC and server applications. However, the future systems are demanding even higher DRAM bandwidth for higher performance.

TECHNICAL HIGHLIGHTS

- **This paper describes a single-ended transceiver design with highest reported data rate at 6.4Gb/s/pin for high-density dual-rank DIMM modules for commercial applications.**
- Besides the highest data rate for DIMM memory interface, this design also achieves exceptional power efficiency at 9.1mW/Gb/s, which is essential for future applications.

APPLICATIONS AND ECONOMIC IMPACT

- This design has demonstrated the potential to be used in various VLSI systems, including data center servers, networking, and low-power handheld devices. The design should enable significant boost in performance due to higher data rate while keeping the overall DRAM power consumption at minimum.

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Session 18 Overview : Advanced Embedded SRAM

MEMORY SUBCOMMITTEE

Session Chair: *Michael Clinton, Texas Instruments, Dallas, TX*
Session Co-Chair: *Atsushi Kawasumi, Toshiba, Kawasaki, Japan*

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR*

SRAM scaling continues with the introduction of a 20nm SRAM using the smallest bit cell reported to date. In addition to scaling, power dissipation continues to be a challenge for SRAM designers. Three of the other papers in this session describe different approaches that significantly reduce active and static power. One design exploits an application-specific solution, the second simultaneously reduces active and static power, and the third uses a fine-granularity-power-gating scheme. While scaling and power reduction are important, one of the most significant aspects of SRAM is performance. The final paper reports on the fastest L1 cache performance ever achieved.

- In Paper 18.1, TSMC describes the first 20nm SRAM with the smallest bit cell of 0.081μm2 demonstrated to date and achieves 200mV lower VMIN by utilizing innovative read and write assist techniques.
- In Paper 18.2, researchers from MIT describe an SRAM operating at 0.6V that further reduces energy/access by 1.9× by exploiting application-specific techniques to reduce bitline switching activity. They also employ statistically-gated sense amplifiers.
- In Paper 18.3, Toshiba describes a 28nm SRAM with a 0.12μm2 bit cell that utilizes a BL power calculator to reduce active power by 27% and a digitally controllable scheme to control the cell retention voltage resulting in 85% lower standby power consumption.
- In Paper 18.4, IBM describes a 22nm SOI SRAM operating over a wide voltage range of 0.7V to 1.1V and employs a fine granularity power gating feature which reduces bit cell leakage by 37% and also reduces peripheral circuit leakage by 40%.
- In Paper 18.5, IBM describes a 32nm L1 Cache SRAM that achieves 7GHz operation by using a 3-level bitline hierarchy and makes extensive use of dynamic circuit design techniques.

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Session 18 Highlights *: Advanced Embedded SRAM*

[18.1] A 20nm 112Mb SRAM in High-κ Metal-Gate with Assist Circuitry for Low-Leakage and Low-VMIN Applications

Paper Authors: *J. Chang, Y. Chen, H. Cheng, W. Chan, H. Liao, Q. Li, S. Chang, S. Natarajan*
Paper Affiliation: *TSMC, Hsinchu, Taiwan*
Subcommittee Chair: *K. Zhang, Intel, Hillsboro, OR*

CONTEXT AND STATE OF THE ART

- The first 20nm 6T SRAM demonstration
- First demonstration of a large memory array using planar technology at 20nm in a fully functional 112Mb design

TECHNICAL HIGHLIGHTS

- **Smallest reported 6T-SRAM bit cell area of 0.081μm2**
- Read assist using a timed WL underdrive and write assist using negative bitline drive enable a VMIN reduction of 200mV
- A four-state power-management scheme reduces retention leakage by over 65%

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrates planar transistor scaling to the 20nm node
- This technology and the highlighted circuit techniques enable very dense SRAM arrays with different levels of leakage power reduction capability for use in a wide range of consumer products.

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Session 19 Overview: Wireless transceivers for smart devices

WIRELESS SUBCOMMITTEE

Session Chair: Sven Mattisson, *Ericsson, Lund Sweden*
Session Co-Chair: Koji Takinami, *Panasonic, Yokohama, Japan*

Subcommittee Chair: David Su, *Qualcomm Atheros, San Jose, CA, Wireless Subcommittee*

Smart devices like mobile phones and tablets feature multiple wireless communication links. To meet the increasing demands for higher data rates, better power efficiency, and lower cost, one can see an accelerating trend to integrate multi-band functionality in an SoC, exploiting digital techniques and advanced CMOS processes. This session has three TX papers covering digital WLAN and Bluetooth transmitters, two papers with high-performance LTE TX modulators, and one paper with an LTE receiver supporting non-contiguous carrier aggregation. On the SoC side, papers on a universal GNSS receiver and a WLAN transceiver supporting MIMO are presented.

- In Paper 19.1, Texas Instruments describes a fully integrated WLAN SoC, supporting 2x2 MIMO at 2.4G and 1x2 MISO at 5GHz. The transceiver integrates PAs for both bands and a T/R switch for 2.4GHz band with 3.83mm2 in 45nm CMOS, achieving the saturated output power of +29dBm at 2.4GHz and +26dBm at 5GHz, respectively.
- In Paper 19.2, University of California Berkeley and ST-Ericsson present a digitally-modulated transmitter for 2.4GHz WLAN implemented in 65nm CMOS. Using a dynamic load modulation scheme with an integrated phase modulator, the transmitter improves PA average efficiency by 20%, achieving 24.5% drain efficiency and 19.3% system efficiency while providing +16.8dBm output power with -28dB EVM for 802.11g.
- In paper 19.3, Mediatek, University of Southern California and University of California, Berkeley, present an all-digital transmitter featuring a current-mode Class-D digital PA that achieves compact die area and high bandwidth capability. The 40nm CMOS digital TX demonstrates 18.8 dBm output power with -25 dB EVM in 802.11g 54Mbps mode and 15.7 dBm output power with -33 dB EVM for a 80MHz BW, 256-QAM OFDM signal at 2.4GHz.
- In paper 19.4, Mediatek presents a 0.25mm2 GPS radio in 40nm CMOS supporting simultaneous GPS/Galileo-Glonass and GPS/Galileo-Beidou dual reception with 2.1dB NF, -165dBm tracking sensitivity, and -8dBm out-of-band IIP3 while consuming 20mW.
- In Paper 19.5, Ericsson presents the first single-chip receiver supporting non-contiguous intra-band and inter-band carrier aggregation, capable of receiving up to three 20MHz LTE carriers simultaneously. It occupies 14.8mm2 in 65nm CMOS and consumes 155mW and 435mW when receiving one and three carriers, respectively.
- In paper 19.6, IMEC and Renesas present a 40nm CMOS modulator that meets C-IM3 requirements for LTE using 25% duty cycle voltage-sampling mixers and a harmonic-rejection baseband. It achieves -65dBc C-IM3 at 3dBm RMS output power for LTE bands from 0.8 to 3GHz, -160dBc/Hz RX-band Noise, 2.2% EVM and -41dBc ACLR.
- In paper 19.7, Marvell and University of Pavia present an LTE /3G transmitter using a class A/B power mixer in 55nm CMOS, which consumes 56mA and 19mA at 4dBm and -10dBm LTE20 modulated signal, respectively. Up to 0dBm LTE20, 50dBc ACLR1, 56dBc ACLR2 and 1.4 % EVM are achieved with -154 dBc/Hz RX noise for LTE10 at 31 MHz offset .
- In paper 19.8, Mediatek and Delft University of Technology present an all-digital polar Bluetooth transmitter with 13.5 dBm peak power occupying 0.27 mm2 in 40nm CMOS. The transmitter demonstrates 5% EVM at 10dBm 8DPSK and bits-to-RF efficiency of 21.4%.

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Session 19 Highlights : Wireless transceivers for smart devices

[19.3] A 24.7dBm all-digital RF transmitter for multi-mode broadband applications in 40nm CMOS

[19.5] A Receiver for LTE Rel-11 and Beyond Supporting Non-Contiguous Carrier Aggregation

Paper [19.3] Authors: ***C. Lu[1], H. Wang[1], CH. Peng[2], A. Goel[3], S. Son[1], P. Liang[2], A. Niknejad[4], HC. Hwang[2], and G. Chien[1]***
Paper [19.3] Affiliation: ***[1]Mediatek Inc., San Jose, CA, [2]Mediatek Inc., Hsinchu Science Park, Taiwan, [3]University of Southern California, Los Angeles, CA, [4]University of California, Berkeley, CA***
Paper [19.5] Authors: ***L. Sundström, M. Anderson, R. Strandberg, S. Ek, J. Svensson, F. Mu, T. Olsson, I. ud Din, L. Wilhelmsson, D. Eckerbert, and S. Mattisson***
Paper [19.5] Affiliation: Ericsson, Lund, Sweden
Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless Subcommittee

CONTEXT AND STATE OF THE ART

- PA efficiency is a major challenge for high-order modulation schemes needed for high data rates
- Next generation WLAN needs to support 256-QAM up to 80MHz
- Conventional receivers use a single carrier at a time only, which limits the available signal bandwidth
- LTE supports non-contiguous carrier aggregation enabling higher data rates

TECHNICAL HIGHLIGHTS

- **All-digital transmitter supporting 256-QAM OFDM**
- In paper 19.3, Mediatek, University of Southern California and University of California, Berkeley, present an all-digital transmitter featuring a current-mode class-D digital PA that achieves compact die area and high bandwidth capability. The 40nm CMOS digital TX demonstrates 18.8 dBm output power with -25 dB EVM in 802.11g 54Mbps mode and 15.7 dBm output power with -33 dB EVM for a 80MHz BW, 256-QAM OFDM signal at 2.4GHz.
- **First reported LTE receiver supporting non-contiguous carrier aggregation**
- In Paper 19.5, Ericsson presents the first single-chip receiver supporting non-contiguous intra-band and inter-band carrier aggregation, capable of receiving up to three 20MHz LTE carriers simultaneously. It occupies 14.8mm2 in 65nm CMOS and consumes 155mW and 435mW when receiving one and three carriers, respectively.

APPLICATIONS AND ECONOMIC IMPACT

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- Digital transmitters enable multi-mode radios, with reduced power consumption as CMOS technology scales, for smart devices at a lower cost
- Frequency aggregation will enable scaling to higher data rates in existing operator networks resulting in more efficient capacity.

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Session 20 Overview : Frequency Generation

RF SUBCOMMITTEE

Session Chair: *Marc Tiebout, Infineon Technologies, Villach, Austria*
Session Co-Chair: *Jing-Hong Conan Zhan, MediaTek, HsinChu, Taiwan.*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France, RF Committee*

VCO and PLL performance is critical for almost all RF applications including receivers, transmitters, imagers, and radar systems. This session starts with the presentation of the latest advances in VCO design with three papers on low phase noise, high tuning range and low-power operation. The next four PLL designs presented include the first 60GHz ADPLL, a low-power 1GHz digital PLL and a wideband 50-to-930MHz analog design for DTV applications.

- In paper 20.1, Lund University presents a VCO operating in Class-D to reduce the power consumption without compromising phase noise. A 2.5-to-3.3GHz VCO designed in a standard 65nm CMOS operates at a power supply between 0.35V and 0.6V, with a figure of merit of 188 to 190dBc/Hz across power supply and tuning range.
- In paper 20.2, Delft University of Technology presents an oscillator operating in Class-F by enforcing a pseudo-square voltage waveform around the tank, by increasing the third-harmonic component of the fundamental through a second resonance. The 65nm CMOS prototype exhibits an average phase noise of -136dBC/Hz at 3MHz offset over the 5.87-to-7.56GHz tuning range.
- In paper 20.3, the University of Pavia and STMicroelectronics present a 40GHz LC VCO where wide frequency tuning is achieved by splitting the inductor with a series MOS switch. A 32nm CMOS prototype shows a 31.6% frequency tuning, and phase noise at 10MHz carrier offset ranging from -115dBc/Hz to -118dBc/Hz with 9.8mW power dissipation.
- In paper 20.4, Delft University of Technology and USTC, Heifei, China unveil the first fractional-N ADPLL at 60GHz, in 65nm CMOS. The ADPLL achieves -72dBc/Hz in-band phase noise, -90dBc/Hz phase noise at 1MHz offset, and the 100MHz reference spur is lower than -74dBc.
- In paper 20.5, Nanyang Technological University and Micron introduce a 57.9-to-68.3GHz, 24.6mW, 65nm CMOS PLL that occupies 0.19mm2. The PLL adopts an injection-coupled quadrature VCO and a self-correcting charge pump with -91.0dBc/Hz phase noise at 1MHz offset.
- In paper 20.6, Infineon Technologies presents a digital PLL that uses a 5-b bang-bang phase detector to relax bandwidth limitation. A phase-interpolator-based fractional-N divider without background calibration is also introduced. The 130nm CMOS PLL occupies 0.25mm2 and consumes 7.4mW.
- In paper 20.7, Ratio Microelectronics and Fudan University show a 50-to-930 MHz fractional-N synthesizer in 0.18 μm CMOS for multistandard DTV tuners. The synthesizer adopts a linearized PFD / CP for noise folding mitigation, and achieves -75dBc reference spur and 0.25° integrated rms phase error (100 Hz to 40 MHz).

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Session 20 Highlights : Frequency Generation

[20.1] A 2.5-to-3.3GHz CMOS Class-D VCO

Paper Authors: *L. Fanori and P. Andreani.*
Paper Affiliation: *Lund University, Lund, Sweden.*
Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France, RFCommittee.*

CONTEXT AND STATE OF THE ART

- Although voltage-controlled oscillators (VCOs) have been around for more than a hundred years, performance, especially in terms of power consumption and low phase noise operation is still improving.
- A Class-C VCO was introduced at ISSCC 2008 by Lund University.

TECHNICAL HIGHLIGHTS

- **The world's first Class-D CMOS VCO drastically reduces the power consumption without compromising phase noise.**
- In paper 20.1, Lund University presents a VCO operating in Class-D to reduce the power consumption without compromising phase noise. A 2.5-to-3.3GHz VCO designed in standard 65nm CMOS operates at a power supply between 0.35V and 0.6V, with a figure of merit of 188 to 190dBc/Hz across power supply and tuning range.

APPLICATIONS AND ECONOMIC IMPACT

- Almost all RF applications including receivers, transmitters, imagers, and radar systems require a VCO in the frequency generation portion of the circuit, and benefit from lower power consumption.
- A VCO consumes a considerable portion of the total power consumption in any mobile phone frequency synthesizer. A low-power, low-phase-noise VCO will improve the operating time of a mobile phone.

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Session 21 Overview : Power Converters

ANALOG SUBCOMMITTEE

Session Chair: *Wing-Hung Ki, HKUST, Hong Kong, China*
Session Co-Chair: *Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands*

Subcommittee Chair: *Bill Redman-White, University of Southampton, UK, Subcommittee Analog*

Efficient power conversion extends the operating time of mobile devices and reduces heat generation in high-power applications. This session covers a wide variety of power converters ranging from fully integrated inductive and switched-capacitor converters for SoC applications, to supply voltage modulators for envelope tracking RF power amplifiers and high-power LED drivers that can be connected directly to the mains. New circuit techniques and technology options are introduced to enhance efficiency and increase power density.

- Paper 21.1 by HKUST presents a 100MHz buck converter in 0.13μm CMOS using package bondwire inductance and an additional flying capacitor to reduce total capacitor area by 10 times for fully integrated implementation. The converter delivers 1.2A and achieves efficiency higher than 80% for load current up to 800mA.
- Paper 21.2 by MediaTek presents an envelope-tracking modulator in 0.15μm CMOS with 3.3V I/O devices for HSUPA transmitters that provides a power reduction of 24% relative to a fixed supply solution at 26dBm PA output power.
- Paper 21.3 by UC San Diego and Brown University presents a stacked-FET supply modulator in 0.18μm CMOS using deadband multi-level switching for envelope tracking RF PA applications. It achieves an efficiency of 83% with a 20MHz LTE signal at 29dBm from a 6V supply.
- Paper 21.4 by the Massachusetts Institute of Technology and Texas Instruments presents a burst-mode controller chip in 0.35μm CMOS with 3.3V/15V high-voltage devices for a quasi-resonant inverted buck converter driving a GaN power transistor. The 11MHz converter drives a 22W LED load and achieves a peak efficiency of 90.6%.
- Paper 21.5 by the University of Michigan presents a switched-capacitor (SC) DC-DC converter in 0.18μm CMOS with 31mV output voltage resolution and 0.4-to-4.0V voltage range. The converter cascades 4:1 and five 2:1 SC stages achieving a peak efficiency of 72% and output variation < 81mVpp for load currents from 0-to-0.3mA.
- Paper 21.6 by the University of California at Berkeley presents a fully integrated switched-capacitor voltage regulator that is implemented in a 65nm bulk LP CMOS process. The converter achieves >73% efficiency at 0.19W/mm2 and maintains <76mV voltage droop under a full load step of 0.253A/mm2 in 50ps.
- Paper 21.7 by the Massachusetts Institute of Technology presents a multi-phase switched capacitor DC-DC converter with a peak efficiency of 93% using on-chip ferroelectric capacitors. The system supports an output voltage of 0.4V to 1.1V from 1.5V input while delivering load current of 20μA to 1mA.
- Paper 21.8 by Dankook University presents a soft self-commutating method for non-isolated multiple-string LED drivers. The 6-string LED driver IC operates directly from 110V AC with 92.2% efficiency, 0.996 PF and 8.6% THD under 22W input power conditions, and requires only one external resistor to set the LED current.

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Session 21 Highlights : Power Converters

[21.4] 90.6% Efficient 11MHz 22W LED Driver using GaN FETs and Burst-Mode Controller with 0.96 power factor

[21.6] A Sub-ns Response Fully-Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm² at 73% Efficiency

Paper [21.4] Authors: *S. Bandyopadhyay[1], B. Neidorff[2], D. Freeman[3], A. Chandrakasan[1]*
Paper [21.4] Affiliation: *[1]Massachusetts Institute of Technology, Cambridge, Massachusetts, [2]Texas Instruments, Manchester, New Hampshire, [3]Texas Instruments, Dallas, Texas*
Paper [21.6] Authors: *H.-P. Le, J. Crossley, S. R. Sanders, and E. Alon*
Paper [21.6] Affiliation: *University of California, Berkeley,California*
Subcommittee Chair: *Bill Redman-White, Southampton University, UK,*

CONTEXT AND STATE OF THE ART

- Recent DC-DC converters that power LEDs for lighting applications utilizing silicon transistors operate at switching frequencies <1MHz necessitating large off-chip inductors. [21.4]
- State-of-the-art efficiencies are 85% at 20W or 88% at 7W [21.4]
- Recent high-performance integrated DC-DC converters provide ~1V to microprocessor cores from a supply voltage of only ~2V, whereas Lithium-ion batteries in mobile devices produce voltages of 3V - 4V. [21.6]
- When modern microprocessors comes out of standby, a large load step is introduced which stresses the associated DC-DC converters. [21.6]

TECHNICAL HIGHLIGHTS

- **Highest efficiency of 90.6% reported for LED drivers at 22W. [21.4]**
- This power converter employs GaN devices switched at 11MHz permitting it to use smaller sized external components than previous designs. [21.4]
- **Sub-ns transient response time for a switched-capacitor CMOS DC-DC converter is the fastest ever reported for a switch-mode power supply. [21.6]**
- The converter also boasts a ~1.5X higher conversion ratio compared with other state-of-the-art designs making it compatible with lithium-ion batteries. [21.6]

APPLICATIONS AND ECONOMIC IMPACT

- Improving the energy-efficiency and reducing the size of LED drivers will increase the penetration of LEDs into a variety of lighting applications. [21.4]
- Improving the transient response of integrated DC-DC converters and making them capable of direct Li-ion battery attachment will obviate the need for discrete power-management ICs, reducing the cost and size of computing equipment. [21.6]

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Session 22 Overview : Sensors & Displays

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Co-Chair: *Aaron Partridge, SiTime, Sunnyvale California*
Session Co-Chair: *Young-Sun Na, LG Electronics, Seoul Korea*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin Germany, IMMD*

This session presents recent achievements in the areas sensors and displays. A noise-insensitive accelerometer extends a differential signaling path through both the MEMS sensor and circuit to reject external interference. An AC biasing approach is described for MEMS microphones to reduce die area, and micropower techniques are developed in heart rate and battery current sensors. Two noise-insensitive multi-touch capacitive sensing approaches are highlighted that reject external interference. New developments in thermal infrared and ultrasonic imaging are highlighted with the most recent results in these fields.

- In Paper 22.1, Robert Bosch presents a dual-mass accelerometer with fully differential signal path through the interface IC together with a pseudo-noise chopping technique that improves immunity to electromagnetic interference. The dual-axis front-end occupies 1.1mm2 in 0.18μm CMOS and consumes 730μA from a 1.9V supply. The system achieves 380μg/√Hz noise floor and 84.5dB dynamic range.
- In Paper 22.2, NXP Semiconductors (with Delft University of Technology) shows how AC biasing for MEMS microphones solves fundamental limitations of DC-biased systems. The combination of ASIC and MEMS shows an SNR of 58dBA at 94dBSPL and consumes 500μA at 5V while occupying 0.25mm2 in 0.16μm CMOS.
- In Paper 22.3, Masdar Institute of Science and Technology presents a non-uniform quantizer and a logarithmic digital-to-resistance converter that achieve low-power operation in a heart rate sensor IC. The IC measures photodiode currents from 4nA to 3.2μA, and heart-rate frequencies from 30 to 300 bpm are supported. The high sensitivity of the IC is demonstrated by measurements in which ambient light is sufficient for operation.
- In Paper 22.4, Delft University of Technology (with Infineon Technologies) presents a micropower current-sensing IC that includes a calibrated shunt resistor, a $\Delta\Sigma$ ADC, and a dynamic bandgap reference to measure battery current. The IC employs dynamic error correction, digital temperature compensation, and a single room-temperature trim. Over the industrial temperature range and 0-to-1A current, measurement offset is 10μA and gain error is ±0.03% 3σ.
- In Paper 22.5, KAIST (with Zinitix) presents a new code-division multiple capacitive touch-sensing IC that simultaneously drives all TX lines. The system achieves a 55dB SNR for a finger and 35dB SNR for 1mm round-tip metal pillar, with 240Hz frame scan rate in a 5-inch touch screen smart phone.
- In Paper 22.6, KAIST (with SiliconWorks) presents a filtered-delta-integration scheme incorporated with a charge-interpolation technique that reduces noise interference in capacitive touch-screen panels. A controller for 10.1-inch touch-screen panels demonstrates 39dB SNR at 120Hz scan frequency with multi-touch performances.
- IN Paper 22.7, KAIST presents a 10b column driver IC for active-matrix LCDs that includes a mismatch-free switched-capacitor interpolation scheme. A 7b R-DAC combined with 3b switched-capacitor DAC provides uniform channel performance and small size. The maximum DNL, INL, and inter-channel DVO are measured to be 0.25 LSB, 0.43 LSB, and 5.6mV.
- In Paper 22.8, CEA-LETI-MINATEC presents an IR bolometer and 0.18μm CMOS circuit with enhanced differential architecture that measure thermal infrared images without a thermo-elecric cooler. The 640×480 pixel 17μm-pitch sensor array and circuit features a noise equivalent temperature difference (NETD) below 50mK over a 60°C range with a 4V power supply and delivers lag-free images at 60 fps.
- In Paper 22.9, Stanford University (with Texas Instruments and North Carolina State University) presents a real-time 3-D ultrasound imaging system that utilizes a 32×32 2D CMUT array with front-end driver ICs. Integration of

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the CMUT and the ICs with a PCB interposer using flip-chip technology allows for a compact device, better noise performance, improved image quality, and reduced number of cable connections to the back-end system.

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Session 22 Highlights : Sensors & Displays

[22.1] A Fully Differential Charge-Balanced Accelerometer for Electronic Stability Control

[22.5] A 55dB SNR with 240Hz Frame Scan Rate Mutual Capacitor 30×24 Touch Screen Panel Read-Out IC using Code-Division Multiple Sensing Technique

Paper [22.1] Authors: *V. Petkov, G. Balachandran, Jochen Beintner*
Paper [22.1] Affiliation: *Robert Bosch Research and Technology Center, Palo Alto, CA, Robert Bosch GmbH, Reutlingen Germany*
Paper [22.5] Authors: *H.C. Shin, S.H. Ko, H.J. Jang, I.H. Yun, K.R. Lee*
Paper [22.5] Affiliation: *KAIST, Daejeon, Korea, Zinitix, Daejeon, Korea*
Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin Germany, IMMD*

CONTEXT AND STATE OF THE ART

- Accelerometers and touch sensors must operate in increasingly noisy environments. For example, automotive safety sensors are moving from dedicated modules to components within the electronic control systems mounted under-hood. This increases the environmental noise but must not interfere with the measurements.

TECHNICAL HIGHLIGHTS

- **Noise immunity is improved by adopting differential signaling and pseudo-noise chopping in the case of the accelerometer.**
- **Code-division multiple sensing is used to drive all transmission lines simultaneously on the touch screen sensor to increase its robustness.**

APPLICATIONS AND ECONOMIC IMPACT

- Robustness of the sensors allows for more compact low-cost modules that will make the cars of the emerging economies safe to drive.
- As touch-screen displays for mobile devices become increasingly thin, they are exposed to increased interference from the display and switched-mode chargers. The described techniques orthogonalize the sense signals from the interferers.

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Session 23 Overview : Short-Reach Links, XCVR Techniques, & PLLs

WIRELINE SUBCOMMITTEE

Session Chair: *Gerrit W. den Besten, NXP Semiconductors, The Netherlands*
Session Co-Chair: *Koichi Yamaguchi, Renesas Electronics, Japan*

Subcommittee Chair: *Daniel Friedman, IBM T.J. Watson, Yorktown Heights, NY*

Advances in high-speed short-reach interfaces are essential for on-chip, chip-to-chip, and board-to-board links, in order to satisfy demands for continuously increasing data transfer capacity. Different I/O techniques are required for different applications, but common critical factors are low power consumption and small area. This session includes several papers focused on short-reach link innovations, new approaches to realizing key link components, and additionally two papers describing new PLL techniques.

- In Paper 23.1, IBM describes a charge-recycling stacked I/O for on-chip interconnects in 45-nm CMOS SOI, providing energy efficiencies of 0.08-to-0.13pJ/b for on-chip interconnects between 1-to-6.5mm and data rates from 5-to-10Gb/s.
- In Paper 23.2, Intel shows a scalable 64-lane chip-to-chip I/O with 1Tb/s aggregate bandwidth. Per-lane data rates of 2-16 Gb/s and power efficiencies of 0.8-to-2.6pJ/bit are demonstrated in 32nm CMOS, with a total demonstrated bus-level power consumption of 2.6W.
- In Paper 23.3, NVidia describes a new ground-referenced single-ended 20Gb/s serial link for short-haul die-to-die communications over high density interconnect on a laminated package. This link is fabricated in 28nm CMOS, operates from a 0.9V supply and has power efficiency of 0.54pJ/b.
- In Paper 23.4, Renesas presents a contactless interface between modules using a coupler-in-package, achieving a BER<10-12 over a 5mm distance. Implemented in 0.18μm CMOS, the differential 5.5Gb/s TX+RX consumes 104+94 mW and the common-mode 50Mb/s TX+RX consumes 9+5.4 mW.
- In Paper 23.5, IBM presents a pipelined half-rate 8-tap NRZ/PAM-4 Tomlinson-Harashima precoder with 6b resolution in 22nm SOI CMOS. Using this design, 8Gb/s PAM-4 data is transmitted over a 34cm PCB channel at a power consumption efficiency of 1.5pJ/bit and a 5× ISI-reduction at 4.0Gb/s NRZ signaling.
- In Paper 23.6, Samsung describes a low-power receiver using an ILO with dual feedback loop and quadrature injection scheme, which reduces jitter-transfer bandwidth by 4× and phase error from 18° to 3°. Fabricated in 0.13μm CMOS, it achieves an 8Gb/s data rate at an efficiency of 0.65pJ/bit.
- In Paper 23.7, Stanford presents a quadrature clock generation and phase interpolation technique using parametric capacitance modulation. Applied in a dual-loop 28Gb/s CDR in 28nm CMOS, the block achieves 1.5° phase resolution, consumes 3.1mW at 13.5GHz, and exhibits a BER<10-12 from 23.2 to 27Gb/s.
- In Paper 23.8, National Taiwan University shows a divider-less sub-harmonically injection-locked 2.4GHz phase-locked loop in a 65nm CMOS process. The phase noise is -126 dBc/Hz at a 1MHz offset, while the integrated jitter is 188fsrms. It consumes 5.2 mW from a 1.2V supply, and has a FOM of -247 dB.
- In Paper 23.9, MediaTek describes a 1.9GHz fractional-N PLL employing a noise shaping segmentation technique which suppresses fractional spurs by 26dB within the 2MHz PLL bandwidth. Die area of the 40nm CMOS implementation is 0.055mm2.

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Session 23 Highlights : Short-Reach Links, XCVR Techniques, & PLLs

[23.2] A Scalable 0.128-to-1Tb/s 0.8-to-2.6pJ/bit 64-Lane Parallel I/O in 32nm CMOS

[23.3] A 0.54pJ/bit 20Gb/s Ground-Referenced Single-Ended Short-Haul Serial Link in 28nm CMOS for Advanced Packaging Applications

Paper 23.2 Authors: *Mozhgan Mansuri, James Jaussi, Joseph Kennedy, Tzu-Chien Hsueh, Sudip Shekhar, Ganesh Balamurugan, Frank O'Mahony, Clark Roberts, Randy Mooney, Bryan Casper*
Paper 23.2 Affiliation: *Intel, Hillsboro, OR*

Paper 23.3 Authors: *John W. Poulton, William J. Dally, Xi Chen, John G. Eyles, Thomas H. Greer III, Stephen G.Tell, C. Thomas Gray*
Paper 23.3 Affiliation: *Nvidia Corp., Durham, NC*

Subcommittee Chair: *Daniel Friedman, IBM T.J. Watson, Yorktown Heights, NY*

CONTEXT AND STATE OF THE ART

- Laminated packages, silicon interposer substrates, and special-purpose package-to-package interconnect will enable systems with greatly improved computational density, memory capacity and bandwidth. To get full advantage of these technologies, high speed signaling techniques are being developed, which exploit massively parallel signaling as opposed to the more traditional signaling over long channel lengths.
- These advanced packaging options demand dense local chip-to-chip interconnect at very high density and low power. However, this target can be achieved only if the challenges of parallel signaling, like power scalability to data rates, tolerance to simultaneous switching noise, and matching between transmitter and receiver reference voltages, are addressed and solved.

TECHNICAL HIGHLIGHTS

- **16Gb/s 64-ch differential package-to-package serial link with 2.6pJ/bit**
- In Paper 23.2, Intel shows a scalable 64-lane chip-to-chip I/O with 1Tb/s aggregate bandwidth. Per-lane data rates of 2-to-16 Gb/s and power efficiencies of 0.8-to-2.6pJ/bit are demonstrated in 32nm CMOS, with a total demonstrated bus-level power consumption of 2.6W.
- **20Gb/s multi-channel single-ended in-package serial link with 0.54pJ/bit**
- In Paper 23.3, NVidia describes a new ground-referenced single-ended 20Gb/s serial link for short-haul die-to-die communications over high density interconnect on a laminated package. This link is fabricated in 28nm CMOS, operates from a 0.9V supply and has power efficiency of 0.54pJ/bit.

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APPLICATIONS AND ECONOMIC IMPACT

- High-density, high-speed chip-to-chip communications are becoming critical for the long-term development of high performance application processors and memory controllers.
- The successful implementation of high density parallel links will allow the continued expansion of the performance expected from complex systems and enable cost advantages by enabling the mixing of different technologies in the context of a range of dense packaging solutions.

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Session 24 Overview : Energy-Aware Digital Design

ENERGY EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: *Wim Dehaene, KU Leuven, Leuven, Belgium*
Session Co-Chair: *Masaya Sumita, Panasonic, Moriguchi, Japan*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital*

Energy efficiency and low-power design are paramount for the next generation of systems-on-chip. To make this a reality, ground-breaking implementation techniques are required for continued improvement. The papers in this session describe several of these innovative circuit concepts. Examples include time-domain mathematical computation, various body-biasing techniques, and resonant clocking. These techniques are applied to real world applications such as LDPC decoders, biomedical processors and FIR filters.

- In Paper 24.1, Toshiba discloses an alternative method of computation for LDPC decoders utilizing a digital-to-time converter (DTC) and time-to-digital converters (TDC) to enable time-domain computational processing. The paper describes how mathematical operations are selectively moved to the time domain, reducing area and energy, to achieve 10.4pJ/b and 6.1Gb/s/mm2.
- In Paper 24.2, the University of Michigan presents the first nonbinary 1.15Gb/s fully-parallel LDPC decoder in 65nm technology. Each processing node applies dynamic clock gating upon detecting algorithm convergence, achieving low energy consumption of 1.1nJ/b at 675mV and 400MHz while delivering 656Mbps throughput.
- In Paper 24.3, STMicroelectronics and CEA-LETI-MINATEC compare their flip well wide-range body-biasing technique on an 802.11n low-density parity-check (LDPC) decoder in a 28nm ultra-thin body and BOX (UTBB) fully-depleted SOI technology, as compared to a conventional 28nm CMOS bulk process. The decoder is shown to have a 46% delay improvement at 0.7V at constant leakage, or a 63% delay improvement at 0.7V at a cost of higher leakage as compared to bulk CMOS.
- In Paper 24.4, National Chung Cheng University utilizes a series-stacked power gate switch to achieve a low-leakage standby mode and for generation of a state-retention voltage rail. This technique is demonstrated on a 5MHz 32b RISC core running at 0.3V, and achieves an energy efficiency of 0.29 fJ/cycle/gate in 0.13μm CMOS.
- In Paper 24.5, ARM describes an in-situ fault-detection technique utilizing a Razor latch for error detection and deferred resolution by the use of time borrowing between successive pipeline stages. This technique is combined with an approximate-error-correction (AEC) algorithm and applied to an FIR accelerator in 65nm CMOS, with a peak throughput of 1.0GS/s, to achieve 37% improved energy efficiency at 1.2V.
- In Paper 24.6, imec and Samsung employ an in-situ performance method with supply-voltage control through an on-die DC-DC converter and bias control adjustment on a sub-threshold reconfigurable biomedical signal processing SoC in 40nm LP CMOS. Combined with fine-grained power gating, this leads to a 30 pJ/cycle operation at 0.4V, and achieves 9MOPS.
- In Paper 24.7, Texas Instruments describes a Cortex-based SoC with zero standby leakage with less than 400ns wake-up latency, achieved by distributing non-volatile storage elements within the core logic in a fine-grained manner using a single 1.5V 0.13μm FRAM technology.
- In Paper 24.8, Kobe University shows a wide-I/O TSV data bus of 4096b and demonstrates 100Gb/s source-synchronous bidirectional data transfer in a 3D stacked interface using an active silicon interposer. The wide nature of the interface allows power consumption to be reduced to 0.56mW/Gb/s.
- In Paper 24.9, the University of Tokyo presents a wide frequency range 0-to-1GHz resonant clocking system. The technique is demonstrated on a 370mV 32b adder array in 40nm CMOS, and demonstrates a 36% power reduction as compared to a non-resonant clock strategy.

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Session 24 Highlights : Energy-Aware Digital Design

[24.7] An 8MHz 75µA/MHz Zero-Leakage Non-Volatile Logic-Based Cortex-M0 MCU SoC Exhibiting 100% Digital State Retention at VDD=0V with <400ns Wakeup and Sleep Transitions

Paper 24.7 Authors: S. Bartling, S. Khanna, M. Clinton, S. Summerfelt, J. Rodriguez, H. McAdams
Paper 24.7 Affiliation: Texas Instruments, Dallas, TX

Subcommittee Chair: Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital

CONTEXT AND STATE OF THE ART

- Nonvolatile memory has been embedded with processors for a long time, mainly to store program code. Storing the processor's state is also possible but it comes at large energy overhead and significant wake-up time.

TECHNICAL HIGHLIGHTS

- **TI demonstrates a processor with NVM having a wake-up time of 358ns and 3.6% area overhead:**
- In Paper 24.7, Texas Instruments describes a Cortex-based SoC with zero-standby leakage with less than 400ns wake-up latency, achieved by distributing non-volatile storage elements within the core logic in a fine-grained manner using a single 1.5V 130nm FRAM technology.

APPLICATIONS AND ECONOMIC IMPACT

- This technology is essential for energy-harvesting applications and handheld devices with limited cooling. Potential usage is in sensor nodes and wearable electronics.
- Processors with 0V retention are a key enabler for e-health, smart RFID and all other applications requiring ultra-low energy consumption.

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Session 25 Overview : Energy Efficient Wireless

WIRELESS SUBCOMMITTEE

Session Chair: *Shouhei Kousai, Toshiba, Kawasaki, Japan*
Session Co-Chair: *Gangadhar Burra, Texas Instruments Inc., Dallas, TX*

Subcommittee Chair: *David Su, Qualcomm-Atheros, San Jose, CA, Wireless*

Energy efficient transceivers for multistandard short range communication and body-area-network systems are emerging. This session covers several techniques that address this area, primarily low-power radios compatible with several standards such as BTLE, Zigbee, and WBAN as well as those that offer extremely low power connectivity, heavily duty cycled and fast wake-up times.

- In Paper 25.1, Texas Instruments presents a 3.4mm2 45nm CMOS NFC radio addressing wide dynamic range requirements by utilizing an automatic field-monitor tag-control scheme. The proposed architecture achieves a high dynamic range while supporting multiple data rates with 0.15A/m RX sensitivity and 4mA current consumption.
- In Paper 25.2, University of Michigan and Cavium describe a fully integrated 9.8GHz Crystal-less UWB transceiver in 180nm CMOS. This solution includes an integrated antenna, RF front-end and baseband processor. It uses bit-level duty-cycling to allow a 30kb/s data rate while consuming 291uW in transmit mode and 306uW in receive mode.
- In Paper 25.3, Columbia University presents a 4.35GHz 65nm CMOS UWB receiver in 65nm CMOS. By utilizing a fully synchronized and self-duty-cycled scheme, the receiver achieves an energy efficiency of 375pJ/bit for a sensitivity of -76.5dBm at a rate of 2Mbps.
- In Paper 25.4, IMEC and Eindhoven University of Technology present a 2.4GHz radio compliant with three wireless personal/body area network standards (Bluetooth LE, Zigbee, IEEE 802.15.6). The sliding-IF RX and polar TX transceiver implemented in 90nm CMOS achieves an energy efficiency of 1.9nJ/bit for a -96dBm sensitivity.
- In Paper 25.5, University of Macau and Insituto Superior Tecnico, Lisbon,present a 2.4GHz Zigbee receiver which unifies a Balun-LNA-I/Q-Mixer with a hybrid filter in one stacked cell. The receiver achieves 8.5dB NF while consuming 1.7mW at an area of 0.22mm2 in 65nm CMOS.
- In Paper 25.6, Institute of Microelectronics A*STAR, Nanyang Technological University and National University of Singapore, present a 2.2mW multi-channel multi-modulation 400MHz transmitter in 65nm CMOS. The transmitter is based on a synthesizer utilizing a phase-interpolated DLL and a hybrid FIR injection locking, and achieves an energy efficiency of 110pJ/b at 20Mb/s QPSK.
- In Paper 25.7, KAIST presents an IEEE 802.15.6-compliant WBAN transceiver in a 0.13um CMOS process. By employing a digital bandpass filter, transmission spectral mask requirements are satisfied while achieving a power consumption of 5.5mW at 1.2V.
- In Paper 25.8, NXP presents a fully integrated UHF ISM-band transceiver supporting BPSK DSSS modulated signals at a chip rate of 600Kchips/s implemented in 14nm CMOS. By using a wide RX bandwidth and high dynamic range, the transceiver simultaneously receives up to 3 ASK/FSK channels in an 800kHz frequency band while consuming 18mA.
- In Paper 25.9, University of Washington and Panasonic introduce a 2.4GHz receiver with transformer coupling to reduce headroom requirement, and demonstrates operation at 300 mV supply voltage. Fabricated in 65nm CMOS, it shows -94dBm sensitivity with only 1.6mW power consumption.
- In Paper 25.10, Princeton University illustrates the first fully integrated radio using low temperature thin-film transistors, achieving a communication range of over 12 meters using a large antenna.

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Session 25 Highlights : Energy Efficient Wireless

[25.7] A 5.5mW IEEE 802.15.6 Wireless Body Area Network Standard Transceiver for Multi-Channel Electro-Acupuncture Application

Paper Authors: H. Lee, K. Lee, S. Hong, K. Song, T. Roh, J, Bae, and H. Yoo
Paper Affiliation: KAIST, Daejeon, Korea
Subcommittee Chair: David Su, Qualcomm Atheros, San Jose CA, Wireless

CONTEXT AND STATE OF THE ART

- An IEEE standard of 802.15.6 for Wireless Body Area Network (WBAN) has been recently established for short-range, highly reliable, and low-power communication around the human body.

TECHNICAL HIGHLIGHTS

- **The world's first 802.15.6 wireless body area network (WBAN) transceiver with electro-acupuncture application**
- A transceiver compliant with the new 802.15.6 WBAN standard is implemented and demonstrated with a multi-channel electro-acupuncture application
- A digital band-pass filter is proposed to meet the stringent spectrum mask.

APPLICATIONS AND ECONOMIC IMPACT

- Sensors for medical and health-care purposes will find wide applicability in telemedicine and personal fitness.
- Ultra low cost and low power wireless medical sensor nodes offer cost and comfort benefits to consumers and opens new markets in the area of wearable devices.

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Session 26 Overview : High-Speed Data Converters

DATA CONVERTERS SUBCOMMITTEE

Session Chair: Boris Murmann, Stanford University, Stanford, CA
Session Co-Chair: Tetsuya Iizuka, University of Tokyo, Tokyo, Japan

Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

Technology scaling and advances in design are enabling complex systems that thrive on high-performance data converters. Such systems cover applications such as Gigabit Ethernet, radar, wireless transceivers, high-speed instrumentation, set-top boxes, and more. Related to the demands of these applications, this session will highlight the latest achievements at sampling rates up to 10.3GS/s and 6-to-14 bits of resolution. The collection of data converters selected for this session exhibit unprecedented combinations of speed, resolution and power efficiency.

- In Paper 26.1, Broadcom presents a 10.3GS/s, 6b flash ADC in 40nm CMOS, with an FOM of 0.7pJ/conv-step. Four-way interleaving, along with dynamic reconfiguration of the comparator order, enables a DSP-based receiver for 10G Ethernet standards.
- In Paper 26.2, NXP introduces a 3.6GS/s 11b 4×16 time-interleaved SAR ADC implemented in 65nm CMOS. An on-chip calibration of gain and offset enables the digitization of 2.5GHz inputs with a THD better than –55dB.
- In Paper 26.3, Agilent presents an 8× time-interleaved 14b pipelined ADC running at 2.5GS/s for highly reliable measurement equipment applications. The chip exhibits 78dB SFDR over a 1GHz bandwidth and is demonstrated in a 0.13μm SiGe BiCMOS technology with better than 10^{-17} metastability rate.
- In Paper 26.4, IBM (with EPFL) describes a single-channel 8b, 1.2GS/s asynchronous SAR ADC for high-speed data link applications in 32nm SOI technology. Using two alternating comparators with a redundant capacitive DAC, the design consumes only 3.1mW from a 1V supply, yielding an energy efficiency of 34fJ/conv-step.
- In Paper 26.5, KAIST (with Samsung) introduce a 9b 900MS/s 2-channel time-interleaved SAR ADC. This design utilizes both 2b and 1b/cycle conversions and achieves 8.6 ENOB in 45nm CMOS with an energy efficiency of 40fJ/conv-step.
- In Paper 26.6, Analog Devices demonstrates a 14b 80MS/s asynchronous SAR ADC in 65nm CMOS. The circuit features a 2-channel time-interleaved architecture with random shuffling among 3 DACs to relaxes residual mismatches, thereby yielding 73.6dB SNDR.
- In Paper 26.7, National Cheng-Kung University presents a 12b 1.6GS/s current-steering DAC in 40nm CMOS. By combining dynamic element-matching and return-to-zero signaling, this DAC demonstrates >70dB SFDR over the entire first Nyquist zone with 40mW power dissipation.

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[26.4] A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 3.2nm Digital SOI CMOS

Paper Authors: L. Kull, T. Toifl, M. Schmatz, P. Francese, C. Menolfi, M. Braendli, M. Kosssel, T. Morf, T. Andersen, Y. Leblebici
Paper Affiliation: IBM Research, Zurich, Switzerland
Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

CONTEXT AND STATE OF THE ART

- SAR ADCs are energy-efficient, but the sampling rates have been limited to several hundreds of MS/s or less due to serial bit decisions.
- High-speed ADC architectures such as flash and pipeline ADCs are less energy-efficient due to the complexity or power-hungry opamps.

TECHNICAL HIGHLIGHTS

- **The fastest-ever single-channel 8b SAR ADC - runs at 1.2GS/s.**
- The combination of 32nm digital SOI implementation, along with alternation between two comparators to save reset time, enables high-speed operation. With 34fJ/conv-step, it also achieves the best energy efficiency at among all comparable GS/s ADCs to date.

APPLICATIONS AND ECONOMIC IMPACT

- Next-generation high-speed data links require low-power, low-cost ADCs with sampling rates of 10GS/s or higher. Based on a single-channel SAR architecture, this 8b ADC consumes only 3.1mW at 1.2GS/s and occupies a mere 0.0015mm2 in area. Only 8-channel time-interleaving is required for 10GS/s.
- Low power consumption, tiny die area, and compatibility with scaled digital CMOS will permit many channels of time-interleaving on a single die for even greater sampling rates.

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Session 27 Overview : Image Sensors

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Chair: *Shoji Kawahito, Shizuoka University, Hamamatsu Japan*
Session Co-Chair: *Robert Johansson, OmniVision Technologies, Oslo Norway*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin Germany, IMMD*

Image sensors continue to evolve and are used in an ever-wider variety of applications. This session highlights sensors that are intended to be used in distributed wireless network nodes, medical imaging, and 3D imaging suitable for both machine vision and the consumer market. Recent advancements in mass production of 3D stacked image sensors are also presented.

- In Paper 27.1, the University of Michigan reports a 256×256 CMOS imager with integrated feature-extraction capability, to identify objects of interest. The on-chip feature extraction reduces the amount of data that has to be transferred by 96.5%. The chip operates at 0.22μW/frame in motion-sensing mode and at 3.4μW/frame for feature extraction.
- In Paper 27.2, the University of Michigan proposes a 128×128 CMOS imager with in-pixel motion detection. Spatial aggregation of pixels and temporal averaging are implemented to minimize blindspots and increase sensitivity to slow motion. The 130nm test chip consumes 467nW while performing motion detection. Full-frame images with 38.5dB dynamic range are captured at 6.4fps while consuming 16μW.
- In Paper 27.3, Olympus presents a 704×512 rolling-shutter, distortion-free, 3D stacked image sensor with in-pixel storage nodes. The two semiconductor substrates, one with a backside-illuminated photodiode array and one with a storage-node array, are connected with interconnects spaced 8μm apart. The interconnection yield is over 99.9%. A parasitic light sensitivity of -160dB is achieved.
- In Paper 27.4, Sony presents an 8Mpixel back-illuminated 3D stacked image sensor. The top substrate consists of an image sensor, implemented using a 90nm CIS process, and the bottom substrate of a logic chip implemented using a 65nm logic process. The substrate interconnect is made with TSVs at the edges of the substrates. The logic chip comprises of an equivalent of 2400k gates. The imager also supports interlaced HDR and RGBW color filter pattern. The HDR mode extends the dynamic range by 24dB.
- In Paper 27.5, Fondazione Bruno Kessler (with STMicroelectronics and the University of Edinburgh) reports an 8×16 pixel array based on CMOS miniature silicon photomultiplier (MiniSiPM) detectors for PET/MRI applications. The pixel size is 610×570um2 and contains 4 digital MiniSiPMs, with a total of 720 SPADs. Energy and time are handled in-pixel by two 7b counters, two 12b 64ps TDCs, accumulator, and FIFOs. The fill factor is 42.9%. An overall system timing resolution of 263ps FWHM is achieved.
- In Paper 27.6, Toyota Central R&D Labs introduces a CMOS SoC that performs time-correlated single-photon counting and complete DSP for a 100m-range time-of-flight sensor. A relative precision of 0.3% and 0.13% at 10fps and 5fps, respectively, are achieved over the full range and an ambient light level of 70klux.
- In Paper 27.7, Fondazione Bruno Kessler reports a range image sensor based on gain-modulated avalanche photodiodes operated in the linear region. The pixel has a 30×x30μm2 size with a fill-factor of 25.7% and a demodulation contrast exceeding 80% at 200MHz modulation frequency. A 3D camera using an LED illumination unit modulated at 25MHz is demonstrated, showing a best precision of 1.9cm and a frame rate up to 200fps.
- In Paper 27.8, Panasonic reports a 2.1Mpixel stereo 3D CMOS image sensor with on-chip lenticular lenses and buried sub-wavelength optics. The pixel pitch is 2.75μm, and a crosstalk of 6.3% is achieved.
- In Paper 27.9, Toshiba presents a 1.4Mpixel CMOS image sensor in a 0.13μm 2P4M CMOS technology. The CDS circuitry uses 1.5V PMOSCAPS with body terminal control to reduce area and power consumption. Furthermore, a 10b pipeline SAR-ADC with an implementation scheme resulting in an 80% reduction of switching power, and 50%

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reduction of the CDAC area. The read noise and power consumption are 187.5μVrms and 51mW, respectively, at 17fps

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Session 27 Highlights : Image Sensors

[27.5] An 8×16-pixel 92kSPAD Time-Resolved Sensor with On-Pixel 64ps 12b TDC and 100MS/s Real-Time Energy Histogramming in 0.13mm CIS Technology for PET/MRI Applications

[27.8] A 3D Vision 2.1M Pixels Image Sensor for Single-Lens Camera Systems

Paper [27.5] Authors: *L. Braga, L. Gasparini, L. Grant, R. Henderson, N. Massari, M. Perenzoni, D. Stoppa, R. Walker*
Paper [27.5] Affiliation: *Fondazione Bruno Kessler, Trento, Italy, STMicroelectronics, Edinburgh, UK, and University of Edinburgh, Edinburgh, UK*
Paper [27.8] Authors: *S. Koyama, K. Onozawa, K. Tanaka, Y. Kato*
Paper [27.8] Affiliation: *Panasonic, Nagaokakyo, Japan*

Subcommittee Chair: *Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee*

CONTEXT AND STATE OF THE ART

- Positron Emission Tomography (PET) scanners compatible with Magnetic Resonance Imaging (MRI) open the way to new frontiers in the field of cancer diagnostics. In order to cope with high magnetic fields, a solid-state solution must be used instead of the traditional photomultiplier tubes (PMT).
- Stereoscopic vision systems currently rely on bulky optics to capture the scene from two different points of view or using multiple cameras.

TECHNICAL HIGHLIGHTS

- **An 8×16 pixel sensor with 92160 SPADs (192×480) offers a real-time output of the total detected energy up to 100Msamples/s. A timing resolution of 263ps FWHM is achieved.**
- **A 2.1M 3D vision image sensor with 2.75×2.75mm2 pixels provides right-eye and left-eye images at 30fps. Buried sub-wavelength micro lenses successfully suppress the crosstalk between right-eye and left-eye pixels to 6%.**

APPLICATIONS AND ECONOMIC IMPACT

- CMOS SiPMs will replace PMTs, allowing higher spatial and energy resolution, better time resolution, and lower cost. This opens the way to low-cost and high performance diagnostic PET systems for pre-clinical application, and also future clinical applications.
- The single-lens single-chip stereoscopic image sensor realizes a compact passive 3D vision camera module, which is applicable to mobile consumer devices and advanced endoscopes.

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ISSCC 2013
TRENDS

CONDITIONS OF PUBLICATION

PREAMBLE

- The Trends document serves to capture the trends within each technology track covered by the scope of ISSCC 2013 in February in San Francisco
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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 60th appearance of ISSCC, on February 17th to the 21th, 2013, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2013, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 17-21, 2013, at the San Francisco Marriott Marquis Hotel.

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As of November 9, 2012, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

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Analog Subcommittee – 2013 Trends

Subcommittee Chair: Bill Redman-White, NXP/Southhampton University, UK

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy must fundamentally be performed with analog systems. As a result, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants, and increased efficiency in wireless power transmission is enabling faster charging over longer distances. There is also an explosion of technologies that permit energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from energy sources at 10's of millivolts, to provide autonomy for remote sensors or to supplement conventional battery supplies in mobile devices. To achieve this, extremely low power must be consumed by the attendant analog circuits so that some energy is left over to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low power systems. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will permit devices to be powered indefinitely from sustainable sources, opening the door to ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like the bridges in our roads, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, digital circuits such as microprocessors drive the market; so semiconductor technology has been optimized relentlessly over the last 40 years to reduce the size, cost, and power consumption of digital circuits. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle has decreased and the variation observed in their analog performance has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in our most modern digital semiconductor technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are captured by movement towards the top-right in the plot below.

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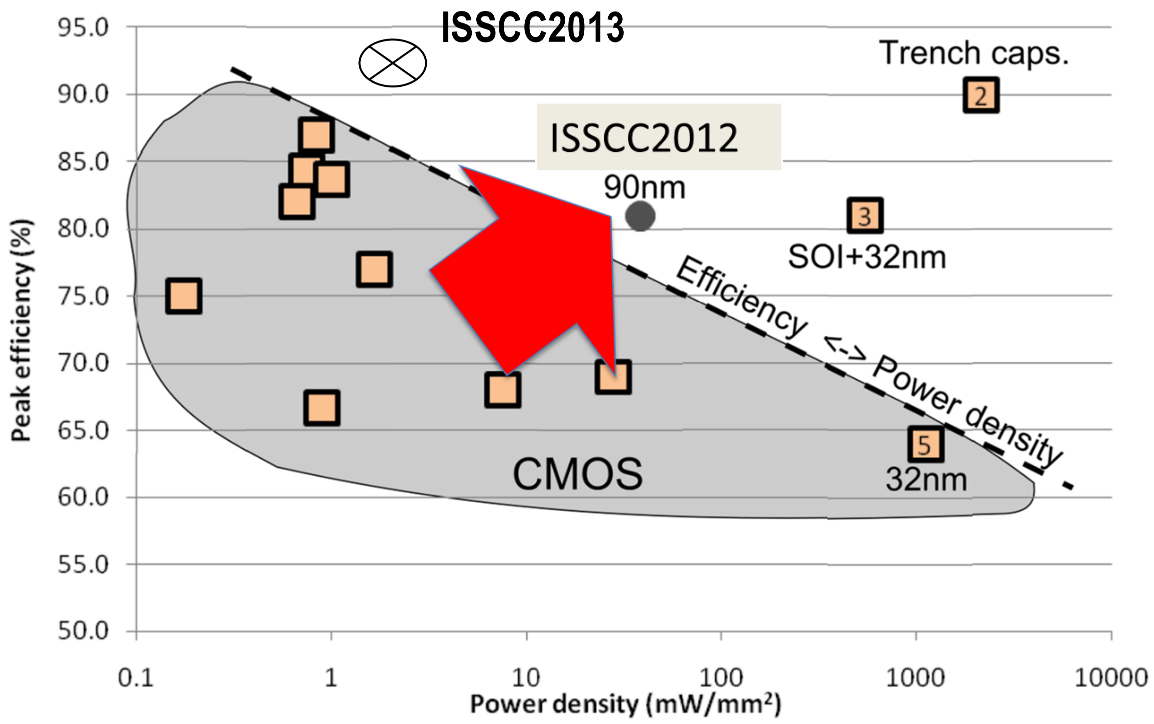

[Session 5: Audio and Power Converters, courtesy paper 5.4 ISSCC 2012]

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Data Converters – 2013 Trends

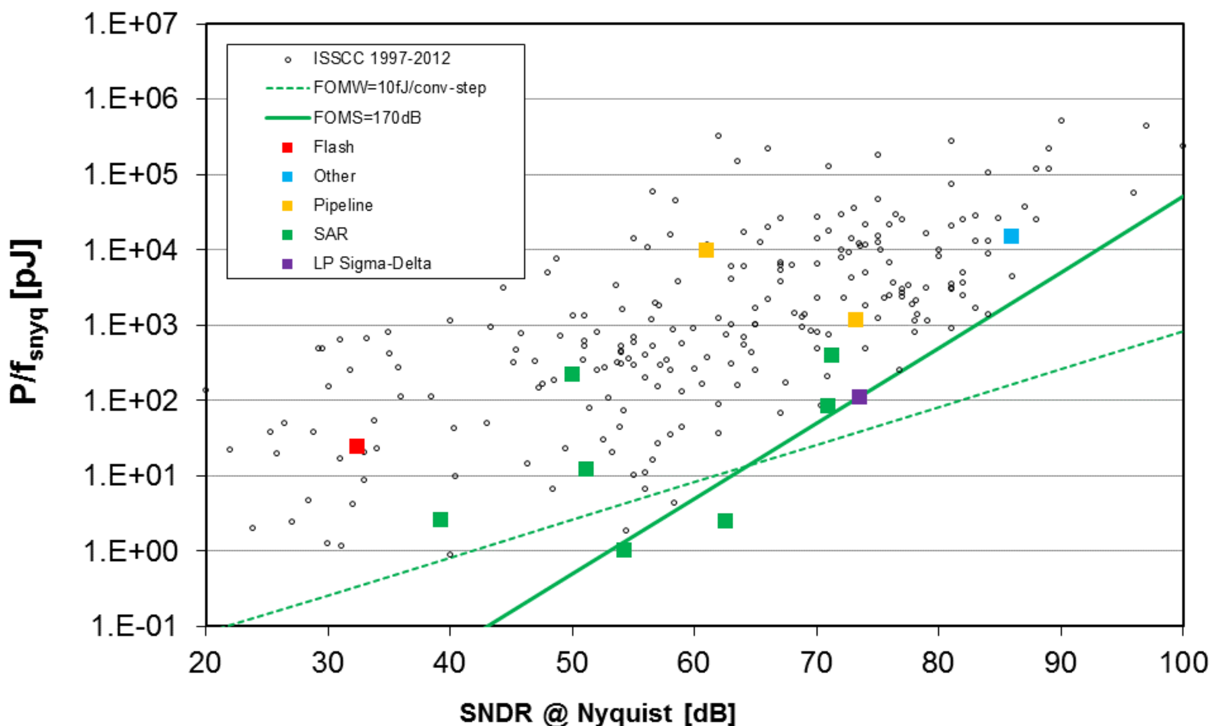
Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

Data converters serve as key building blocks in almost all known applications that bridge the analog physical world with the digital circuits that drive the functionality in modern integrated circuits. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be key drivers for innovation, as evidenced by the data converters presented at ISSCC 2013.

The first figure below shows energy efficiency expressed as power dissipated relative to the effective Nyquist sample rate (P/f_{snyq}) and as a function of the ADC's signal-to-noise ratio (SNDR). For low- to medium-resolution converters, energy is primarily expended to quantize the signal; the efficiency of this operation can be measured as the energy consumed per conversion step (the so-called Walden Figure of merit). The dotted trend line represents a benchmark of 10 fJ/conv-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of the signal-to-noise ratio shown by the solid line. Contributions for 2013 are indicated by the colored dots representing various converter architectures with contributions from previous years denoted by the smaller dots. (Note here that a lower P/f_{snyq} metric represents a more efficient circuit.) Several new SAR-based converters at various SNDR design points continue to push the limits of energy efficiency and push into previously unchartered territory.

The second figure shows energy per conversion step vs. the effective sample rate. This figure elucidates the difficulties of high-speed operation for a given technology. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the spectrum of conversion rates.

The final chart shows achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2013, we see many examples that set new records in this metric utilizing several different converter architectures.



Power efficiency versus SNDR, highlighting ISSCC 2013 results

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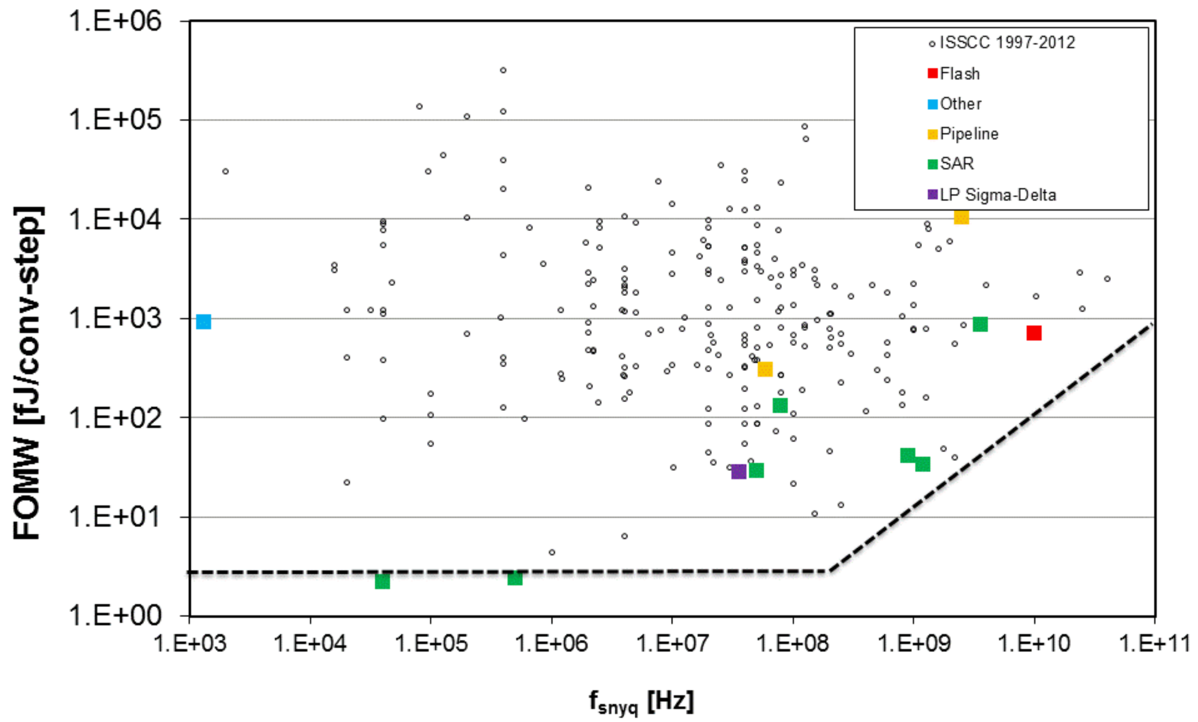
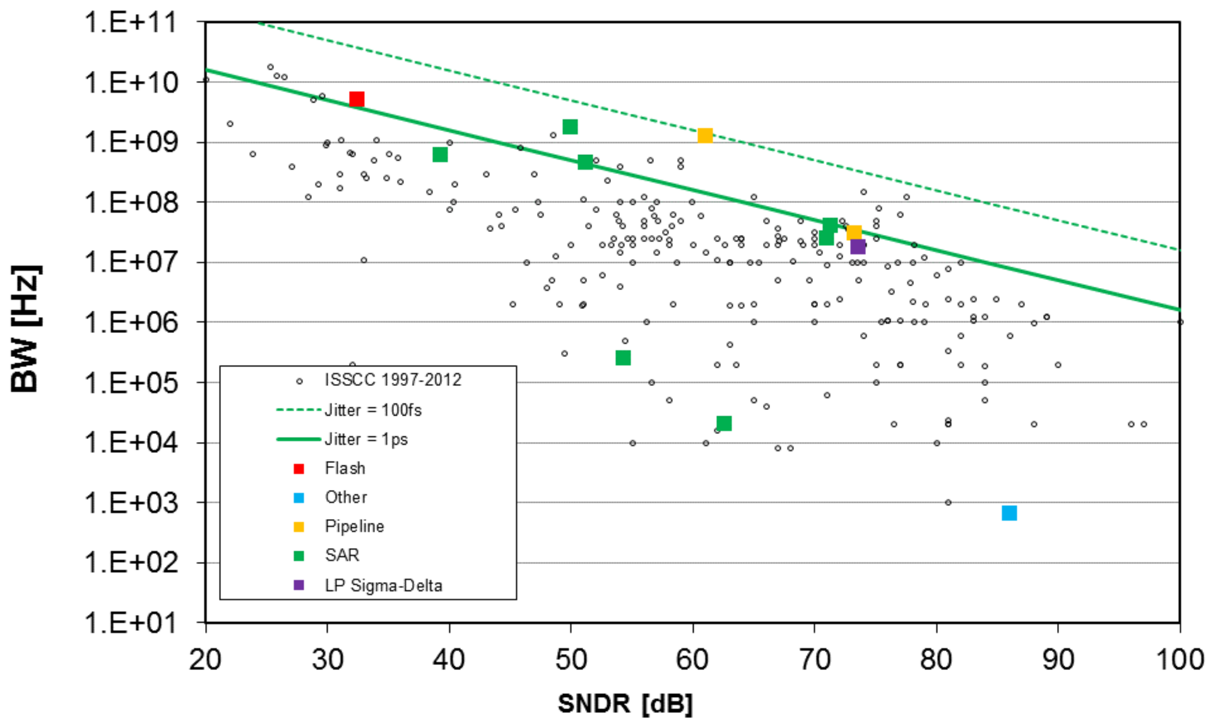


FoM (energy per conversion step) versus Nyquist-bandwidth for various converters



Bandwidth versus SNDR.

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Energy Efficient Digital – 2013 Trends

Subcommittee Chair: Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital

Demand for ubiquitous mobile functionality to achieve enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive innovation in technologies that will deliver to these objectives in an energy and cost-efficient manner. While the performance of embedded processors has increased to meet the rising demands of general-purpose computations, dedicated multimedia accelerators provide dramatic improvements in performance and energy efficiency of specific applications. Energy harvesting is another area of growing importance, leading to technologies that leverage non-volatile logic-based SoC's for applications that do not have a constant power source or handheld devices with very limited battery capacity.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as reducing the area required to implement specific functions. Processors unveiled at ISSCC 2013 are built on a variety of technology nodes, with best-in-class results accomplished along the axes of integration, performance/watt and functional integration, as well as a few industry-first implementations. These are demonstrated in various process nodes ranging from 0.13μm down to 28nm bulk, and SOI CMOS technologies.

Emerging medical applications require a significant reduction in the standby power over state-of-the-art commercial processors. This drives the exploration of new leakage-reduction techniques in both logic and on-chip memories, targeting orders of magnitude reduction in leakage currents. Fast wake-up time requirements drive the need for saving and restoring the processor state.

Figure 1 illustrates the main trends in feature phones and smart phones relevant to energy-efficient digital circuits. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300 MHz in the early 2000s, there has been sudden spurt towards 1 GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and recent smart phones incorporate dual and even quad-core processors, running up to 2GHz frequencies. Battery capacity, mostly driven by the required form factor, as well as thermal limits imply a power budget of roughly 3W for a smartphone. From this budget, also the power amplifier (for cellular communication) and the displays have to be powered. The available power budget for everything digital is in the range of 2W (peak) to 1W (sustained). As a result, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth). For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, and computational imaging, to name a few. For all digital circuits, the limited power budget leads to more fine-grained clock gating, various forms of (adaptive) voltage-frequency scaling, a variety of body-bias schemes, and elaborate power management strategies.

Figure 2 shows the evolution of bitrates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links consistently show a 10× increase every five years, with no sign of abating. With essentially constant power and thermal budgets, energy efficiency has become a central theme in designing the digital circuits for the involved signal processing. Historically, CMOS feature sizes halve every five years. For a brief period in the 1990s, CMOS scaling (a.k.a. Dennard scaling) provided a 2^3 (α^{-3}) increase in energy efficiency per five years, almost matching the required 10×. During the past decade, however, CMOS scaling offers a roughly 3× improvement in energy efficiency every five years. The resulting ever-widening gap has led to alternative approaches to improve energy efficiency, namely, new standards, smarter algorithms, more efficient digital signal processors, highly-optimized accelerators, smarter hardware-software partitioning, as well as the power management techniques mentioned above.

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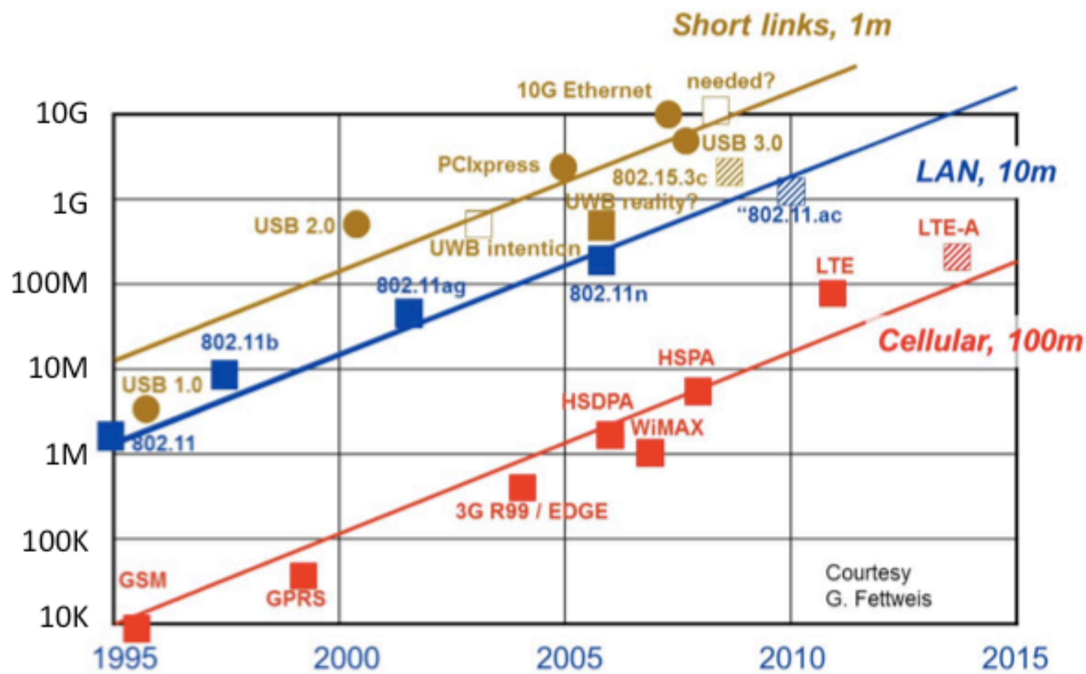
Category	Stages (2004 → 2013)						
Graphics	2D, 3D	OpenGL (ES1.1)	OpenGL/VG/MAX (ES2.0)	AR (Augmented Reality)			
Display	16b QVGA	VGA	Dual 24b WVGA @ 60fps	Dual 24b Stereo SXGA @ 60fps			
Camera	1-2M	3M	5~8M	10M	16M	20M	Dual camera
Image/Video	JPEG, MPEG-4	H.264/AVC (VGA)	H.264/AVC (D1)	H.264/AVC (Full HD)	H.264/MVC H.264/SVC		
Audio	MP3	AAC	AAC Plus	WMA Dolby 5.1	Dolby TrueHD/Digital+		
Accelerator	DSP	FPU	SIMD Multi-core	Many-core			
downlink [Mb/s]	EGPRS 0.4	UMTS 0.4- 2	HSPA 1.8 - 7	HSPA+ 7 - 42	LTE 100		
CPU [MIPS]	-300	300-500	500-800	800-2400	2400-6000		

2004	2005	2006	2007	2008	2009	2010	2011	2012	2013

Application processor trends in smart phones.



Wireless and wired data rates over time.

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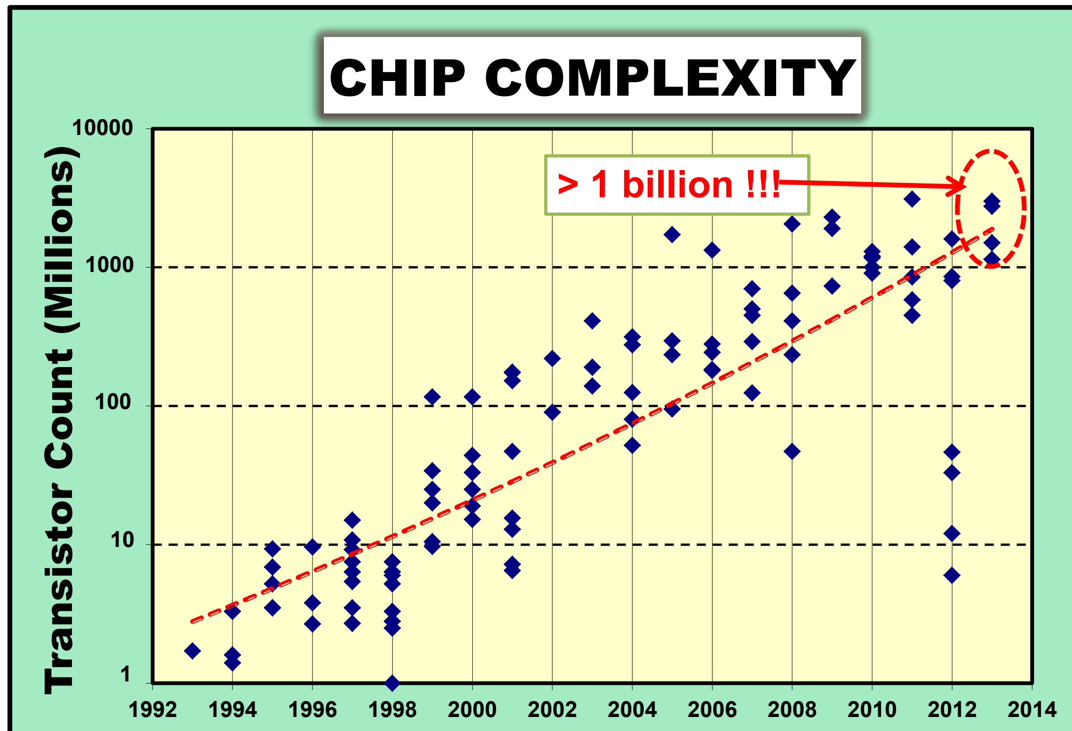
High-Performance Digital – 2013 Trends

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

The relentless march of process technology brings more integration and performance. IBM's System z processor leads the charge at ISSCC 2013 clocking in at 5.7GHz and with 2.75B transistors.

The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration mark was achieved some years ago, we now commonly see processors with beyond 2B transistors on a die.



Leveraging sophisticated strategies to lower leakage and manage voltage, variability and aging, has bolstered the continuing reduction in total power dissipation. This is helping rein in the increase in energy demands from PCs, servers, and similar systems. As power reduction becomes mandatory in every application, the trend towards maintaining near-constant clock frequencies also continues as shown below in frequency trends plot. This will yield solutions with less cost and cooling demands, resulting in greener products in the future.

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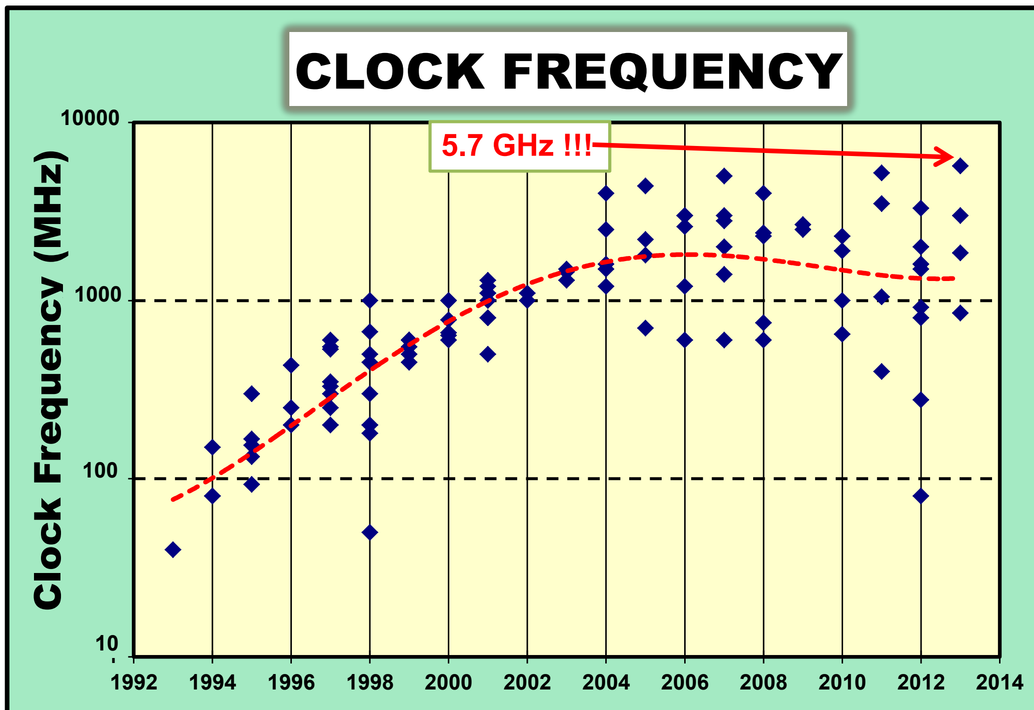
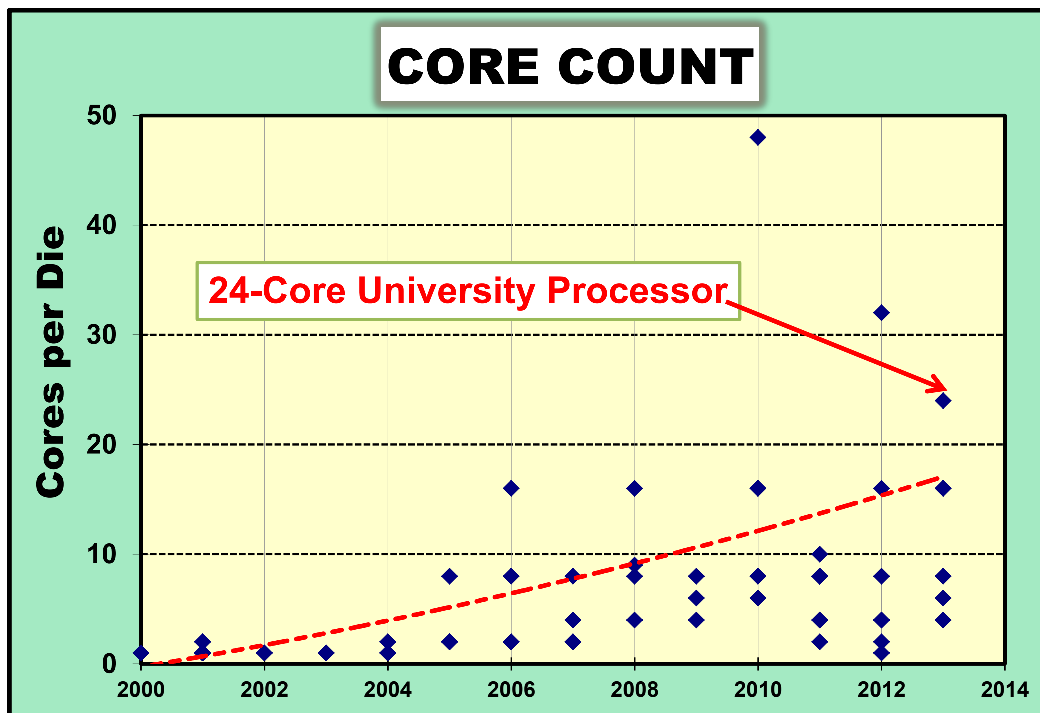


Processors are choosing to trade off performance by lowering supply voltage. The performance loss of reduced voltage and clock frequency is compensated by further increased parallelism. Processors with more than 8 cores are now commonplace. This year at ISSCC 2013, a 24-core processor from Fudan University will be presented as noted in the core-count trend chart below.



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In addition to the trend to integrate more cores on a single chip, multiple die within a single package are appearing. In ISSCC 2013, IBM will present a multi-chip module with six CPUs and two embedded DRAM cache chips. As well, dedicated co-processing units for graphics and communications are now commonly integrated on these complex systems-on-chip. Design of these SoCs requires broad collaboration across multiple disciplines including circuits, architecture, graphics,

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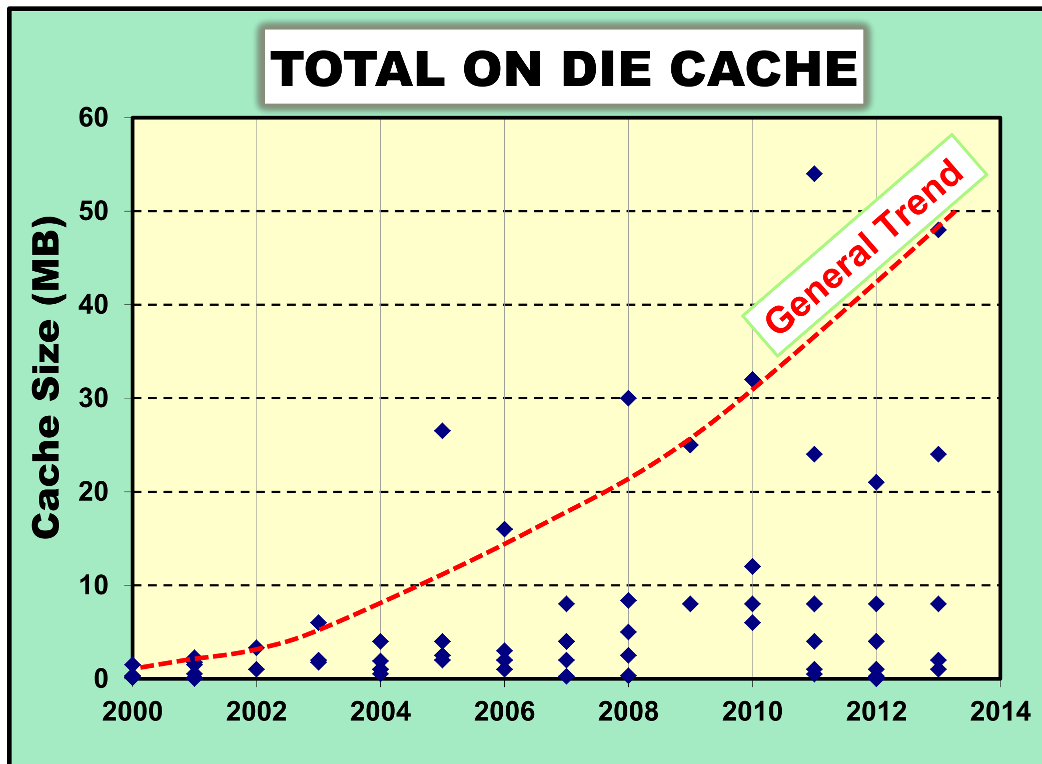
process technology, package, system design, energy efficiency and software. New performance and power-efficient computing techniques continue to be introduced at targeted, critical applications such as floating point and SIMD.

As technology continues to scale to finer dimensions, large caches are being integrated into microprocessor die. The chart below shows the general trend of large cache integration.



Methods to communicate within-die as well as cross-die are becoming increasingly important. This is being driven by two trends: (1) 3D integration continues to grow in interest and (2) intra-die communications become more challenging with process scaling due increases in delay per unit interconnect length. Work on bringing package-level inter-chip transport onto the die has been gaining in popularity and we see this trend continuing.

Another trend evident at ISSCC 2013 is the continued emergence of all-digital phase-locked loops and delay-locked loops to better exploit nanometer feature size scaling and reduce power and area costs. Due to the application of highly innovative architectural and circuit design techniques, the features of these "all-digital" PLLs and DLLs have improved significantly over the recent past. The diagram below shows the jitter performance vs. energy cost for PLLs and MDLLs.

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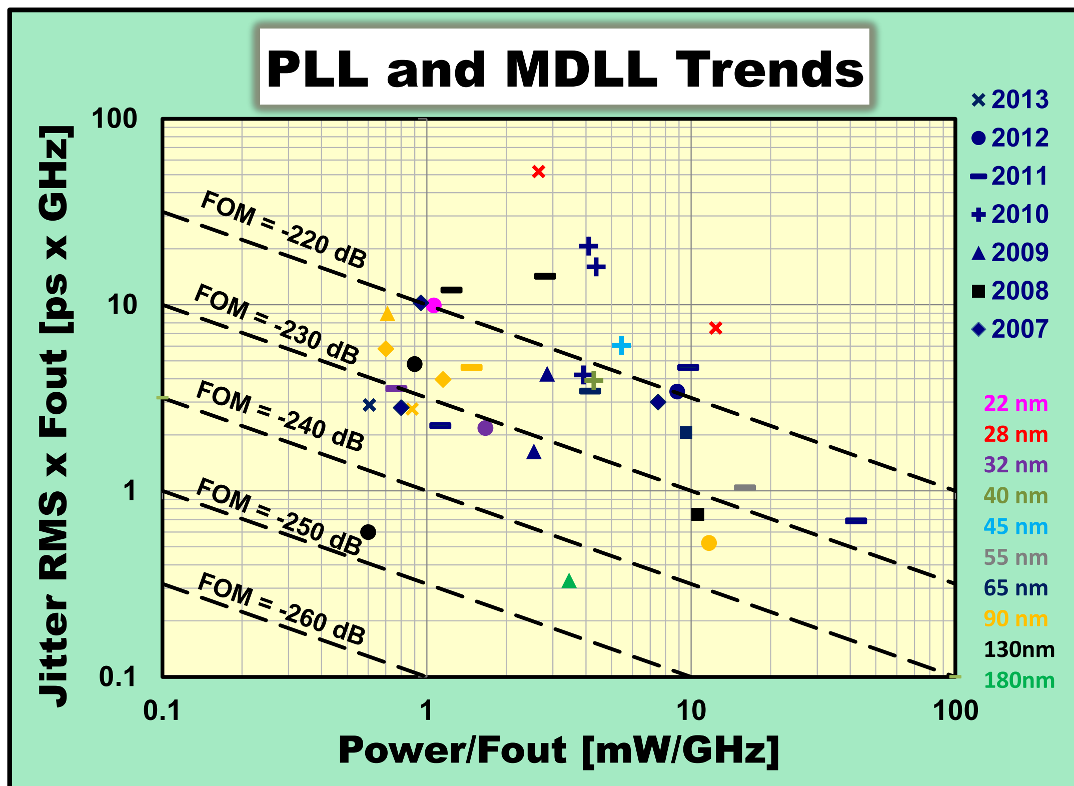

Overall, digital processors continue to grow in complexity, while more circuits are implemented using digital techniques to cope with variability and ease scaling to finer geometries.

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IMAGERS, MEMS, MEDICAL & DISPLAYS – 2013 Trends

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany

IMAGERS

Since 2010 there has been growth beyond expectations in the adoption of mobile devices, e.g., smart phones and tablets, which has called for larger volumes of CMOS image sensor chips to be produced. The resolution and miniaturization races are ongoing, and performance metrics are also becoming more stringent. In addition to the conventional pixel shrinkage, a "more than Moore" trend is increasingly evident. Resolutions of over 20Mpixels are commercially available for mobile devices employing enhanced small-size pixels. Thanks to the innovative readout and ADC architectures embedded at the column and chip levels, data rates approaching 50Gb/s and a noise floor below single electron have been demonstrated. In addition to the conventional applications, ultra-low-power vision sensors, 3D, high-speed, and multispectral imaging are the front-running emerging technologies.

Back-side Illumination (BSI) is now the mainstream technology for high-volume, high-performance mobile applications, 1.12μm BSI pixels are available, and the industry is potentially moving towards 0.9μm pixel pitch and below. Additional innovative technologies outside of the traditional scaling include advanced 3D stacking of a specialized image sensor layer on top of deep-submicron digital CMOS (65nm 1P7M) using through silicon vias (TSVs) and micro-bumps. The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts is a trend throughout the image sensor industry toward higher levels of integration to reduce system costs.

Ultra-low-power vision sensors are being reported in which more programmability and computation is performed at the pixel level in order to extract scene information such as object features and motion.

Lightfield/plenoptic commercial cameras, which have been available since 2010, are now gaining popularity and are being marketed for 3D imaging and/or all-in-focus 2D imaging. On-chip stereoscopic vision has been demonstrated through digital micro lenses (DML), paving the way to next-generation passive 3D imaging for mobile and entertainment applications, e.g. through gesture control user interfaces.

Significant R&D effort is being spent on active 3D imaging time-of-flight (TOF) applications to support requirements from autonomous driving, gaming, and industrial applications, addressing open challenges like background light immunity, higher spatial resolution, and longer distance range. Deep-submicron CMOS single-photon avalanche diodes (SPADs) have been developed by several groups using different technology nodes. They are now capable of meeting the requirements for high resolution, high timing accuracy by employing highly parallel time-to-digital-converters (TDCs) and small pixel pitch with better fill factor.

Ultra-high-speed image sensors for scientific imaging applications with up to 20Mfps acquisition speed have been demonstrated.

Multispectral imaging is gaining a lot of interest from the image sensor community: several research groups have demonstrated fully CMOS room-temperature THz image sensors, and a hybrid sensor capable of simultaneous visible, IR, and THz detection has been reported.

The share of CCDs continues to shrink in machine vision, compact DSC and security applications. Only for high-end digital cameras for astronomy and medical imaging do CCDs still maintain a significant market share.

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Sensors & MEMS

MEMS inertial sensors are finding widespread use in consumer applications to provide enhanced user interfaces, localization, and image stabilization. Accelerometers and gyroscopes are being combined with 3D magnetic-field sensors to form nine-degree-of-freedom devices, and pressure sensors will eventually add a 10th degree. The power consumption of such devices is becoming sufficiently low for the sensor to be on all the time, enhancing indoor navigation. There have been further advances in heterogeneous integration of MEMS with interface circuits in supporting increased performance, larger sensor arrays, reduced noise sensitivity, reduced size, and lower costs.

To address the stringent requirements of automotive, industrial, mobile, and scientific application, MEMS inertial sensors, pressure sensors and microphones are becoming more robust against electromagnetic interference (EMI), packaging parasitics, process voltage temperature (PVT) variations, humidity, and vibration.

Sensor interfaces achieve increasingly high resolution and dynamic range while maintaining or improving power or energy efficiency. This is achieved through techniques such as zooming, non-uniform quantization, and compensation for baseline values.

New calibration approaches, such as voltage calibration, are being adopted for BJT-based temperature sensors to reduce cost. In addition to thermal management applications (prevention of overheating in microprocessors and SoCs), temperature sensors are also increasingly co-integrated with other sensors (e.g. humidity, pressure, and current sensors) and MEMS resonators for cross-sensitivity compensation. Alternative temperature-sensing concepts find their way into applications with specific requirements not easily addressed by BJTs: thermal diffusivity-based sensing for high-temperature applications; thermistor-based and Q-based concepts for *in-situ* temperature sensing of MEMS devices and for ultra-low-voltage operation.

MEMS oscillators continue to improve; phase noise is now low enough for demanding RF applications, 12kHz-to-20MHz integrated jitter is now below 0.5ps, and frequency accuracy is now better than 0.5ppm. Consumer applications are adopting new low-power and low-cost oscillators.

Biomedical

There have been continuous achievements in the area of ICs for neural and biopotential interfacing technologies. Spatial resolution of neural monitoring devices is being reduced utilizing the benefits of CMOS technology. IC providers are increasing their component offerings towards miniaturization of portable medical devices.

Telemedicine and remote-monitoring applications are expanding with support from IC manufacturing companies. The applications of such systems are not limited to services targeted for elderly or chronically ill patients; for example there are several technologies developed to enhance the way clinical trials are conducted by monitoring patient adherence and by improving data collection. Low power WiFi, and Bluetooth-low-energy is emerging as a standard wireless connection between portable communication services and wearable technology.

Smart biomolecular sensing is another major trend that marries solid-state and biochemical worlds together with the ultimate goal of enabling a more predictive and preventative medicine. With the help of the accuracy and parallelism enabled by CMOS technology, time, cost, and error rate of DNA sequencing may be significantly improved. Direct electronic readout may relax the need for complex biochemical assays. Similar trends are becoming increasingly evident in the space of proteomics and sample preparation.

Even for medical imaging, there is a trend from hospital imaging toward point-of-care and portable devices. A key example is in the space of portable high-resolution ultrasounds in which larger scientific imaging setups are being integrated onto the sensor by process technology (e.g. integrated spectral filters, CMUT). Another example is in the space of molecular imaging. The advent of silicon photomultipliers (SiPM) providing a solid-state alternative to PMTs enable the realization of PET scanners compatible with MRI, opening the way to new frontiers in the field of cancer diagnostics. More recently,

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SiPMs realized within deep-submicron CMOS technologies have allowed the integration at pixel- and chip-level of extra features, e.g. multiple timestamp extraction, allowing in perspective a dramatic reduction of the system cost.

Displays

The desire to put much higher-resolution and higher-definition displays into mobile applications is one of the display-technology trends, and it is now opening a Full HD smartphone era. 440ppi high-definition displays are expected, even for 5-inch display sizes. Low-temperature polysilicon (LTPS) technology seems to have more merits over a-Si TFT technology. But a-Si TFT and oxide TFT technologies supported by compensating driver systems are being prepared to compete with it. Very-large-size LCD TVs over 84 inches, and UD (3840×2160) resolution are now the leading entertainment systems. 55-inch AMOLED TVs with Full HD resolution are also opening new opportunities in consumer applications.

As touch-screen displays for mobile devices become increasingly thin, capacitive touch sensors move closer to the display. The resulting in-cell touch displays come with reduced signal levels due to increased parasitics, and increased interference from the display and switched-mode chargers. Noise immunity is improved by adopting noise filtering and new signal-modulation approaches.

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MEMORY – 2013 Trends

Subcomittee Chair: Kevin Zhang, Intel, OR

We continue to see progressive scaling in embedded SRAM, DRAM, and floating-gate based Flash for very broad applications. However, due to the major scaling challenges in all mainstream memory technologies, we see a continued increase in the use of smart algorithms and error-correction techniques to compensate for increased device variability. In further response to these challenges, we see logic processes adopting FinFET devices along with read- and write-assist circuits in SRAMs. Emerging memory technologies are making steady progress towards product introductions, including PCRAM and ReRAM, while STT-MRAM is beginning to become a strong candidate for both standalone and embedded applications.

SRAM

Embedded SRAM continues to be a critical technology enabler for a wide range of applications from high performance computing to mobile applications. The key challenges for SRAM include V_{CCMIN}, leakage and dynamic power reduction while relentlessly following Moore's law to shrink the area by 2× for every technology generation. As the transistor feature size marches toward sub-30nm, device variation has made it very difficult to shrink the bit cell size at the 2× rate while maintaining or lowering V_{CCMIN} between generations. Starting at 45nm, the introduction of high-k metal-gate technology reduces the V_t mismatch and enables further device scaling by significantly reducing the equivalent oxide thickness. Starting at 22nm and beyond, new transistors such as FinFETs and fully-depleted SOI are key to enabling the continuous scaling of bit cell area and low voltage performance. Design solutions such as read/write assist circuitry have been used to improve SRAM V_{CCMIN} performance starting at 32nm. New SRAM bit cells with more than 6 transistors have also been proposed to minimize operating voltage. For example, 8T register file cells have been reported in recent products requiring low V_{CCMIN}. Dual-rail SRAM design emerges as an effective solution to enable dynamic voltage-frequency scaling (DVFS) by decoupling logic supply rails from SRAM arrays and thus allowing much wider operating window. It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope at the next technology node. Sleep transistors, fine-grain clock gating and clock-less SRAM designs have been proposed to reduce leakage and dynamic power. Redundancy and ECC protection are also keys to ensure yield and reliability when embedded SRAM products go to production. Figure 1 shows the SRAM bit cell scaling trend on the left axis and the SRAM V_{DD} scaling trend on the right axis, using data from major semiconductor manufacturers.

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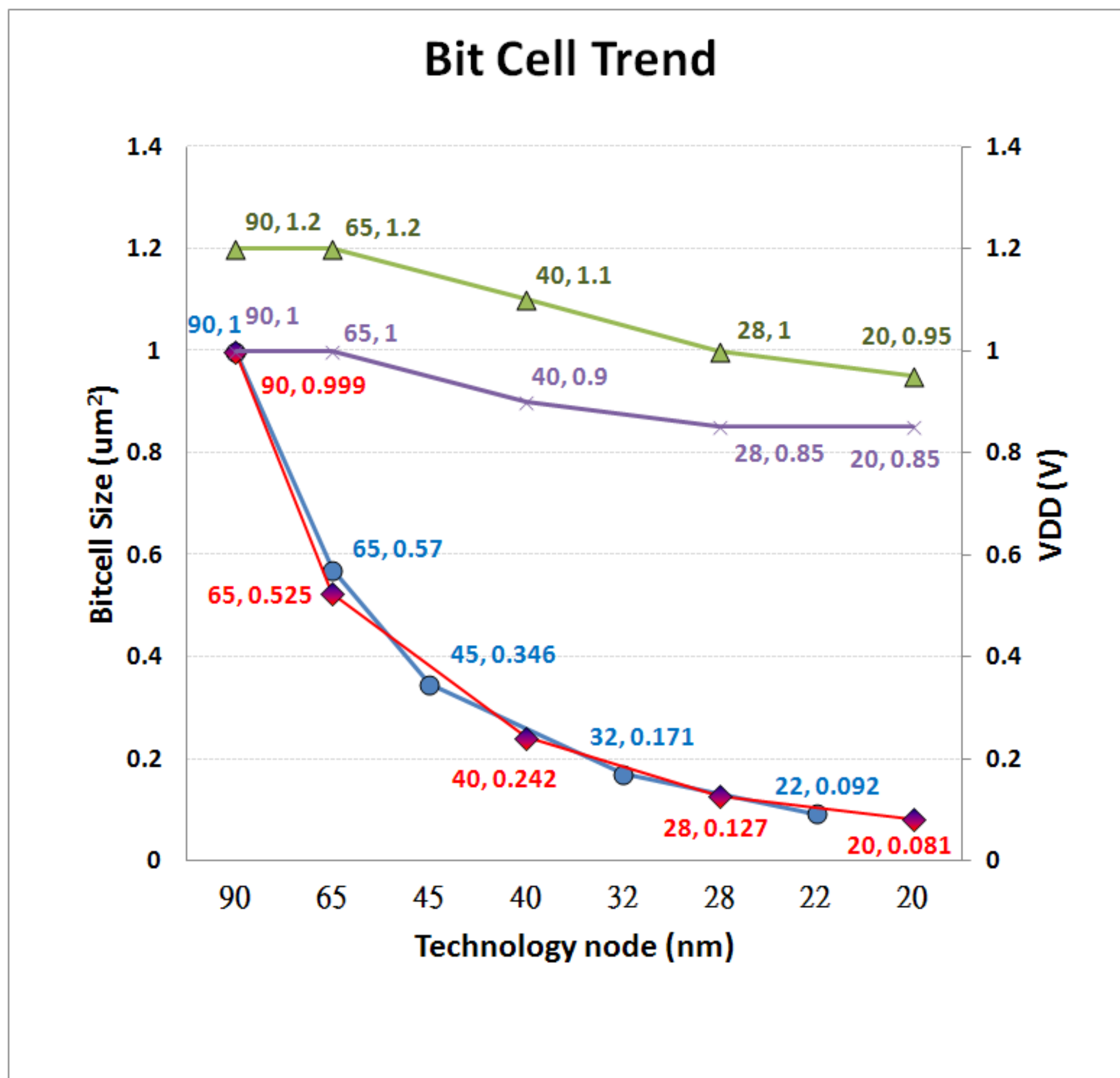

Figure 1: Bit cell and V_{DD} scaling trend of SRAM from major semiconductor manufacturers.

HIGH-SPEED I/O for DRAM

In order to reduce the bandwidth gap between main memory and processor frequencies, external data rates continue to increase as conventional high-speed wired interface schemes such as DDR(x) and GDDR(x) for DRAM evolve (Figure 2). Currently GDDR5 and DDR4 memory I/Os operate around 7Gb/s/pin and 3Gb/s/pin, respectively. To achieve higher speed data transfer rate, signal integrity techniques such as crosstalk, noise and skew cancellation, and speed enhancement techniques such as equalizer and pre-emphasis have been developed. These advanced techniques have pushed I/O speeds towards 10Gb/s/pin. Lower power consumption for data center and mobile applications is also pursued. A near-ground signaling method, termination impedance optimization, decision feedback equalizer, and clock-feathering slew rate control technologies have been demonstrated to reduce the power dissipation of memory interfaces significantly, while achieving high bandwidth.

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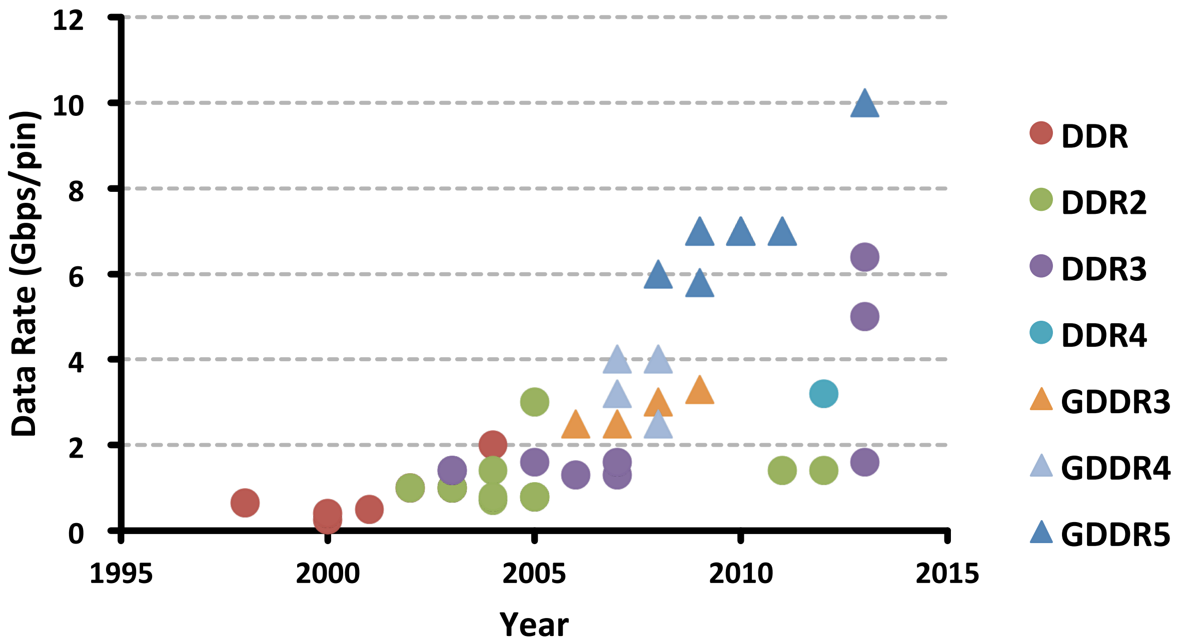

Figure 2: DRAM data rate/pin trends

NONVOLATILE MEMORIES

In the past decade significant focus has been put on the emerging memories field to find a possible alternative to floating gate nonvolatile memory (NVM). The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer RAM (STT-MRAM), and resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit for both read and write operations. Some commercial applications, such as cellular phones, have recently started to use PRAM, demonstrating that reliability and cost competitiveness in emerging memories is becoming a reality. Fast write speed and low read-access time are being achieved in many of these emerging memories. At ISSCC 2013, a 32Gb ReRAM cross-point array is demonstrated in 24nm technology. Figures 3 and 4 provide a summary on the scaling trends for both bandwidth and density in emerging memories.

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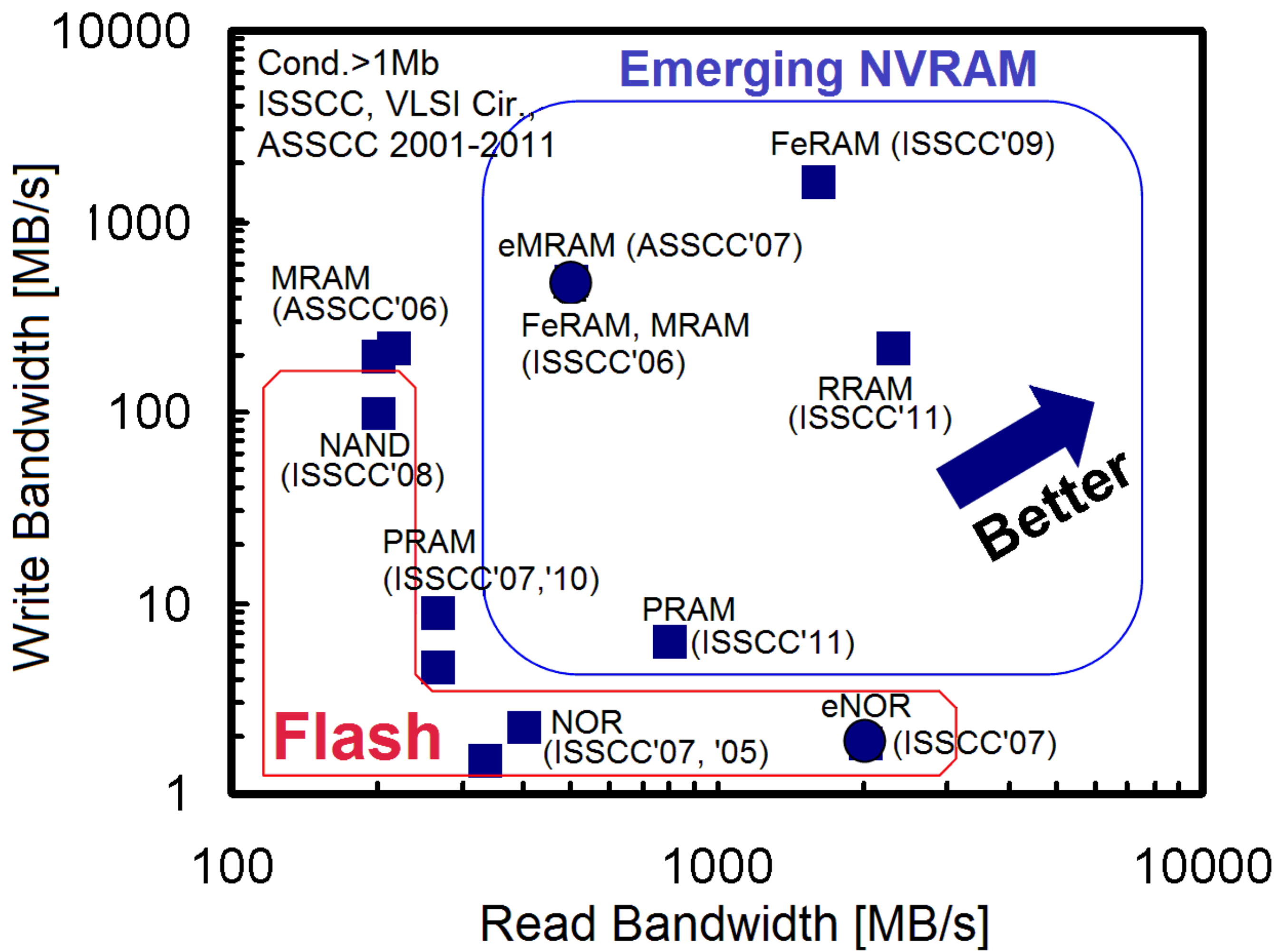

Figure 3: Read- and write-bandwidth comparison of nonvolatile memories.

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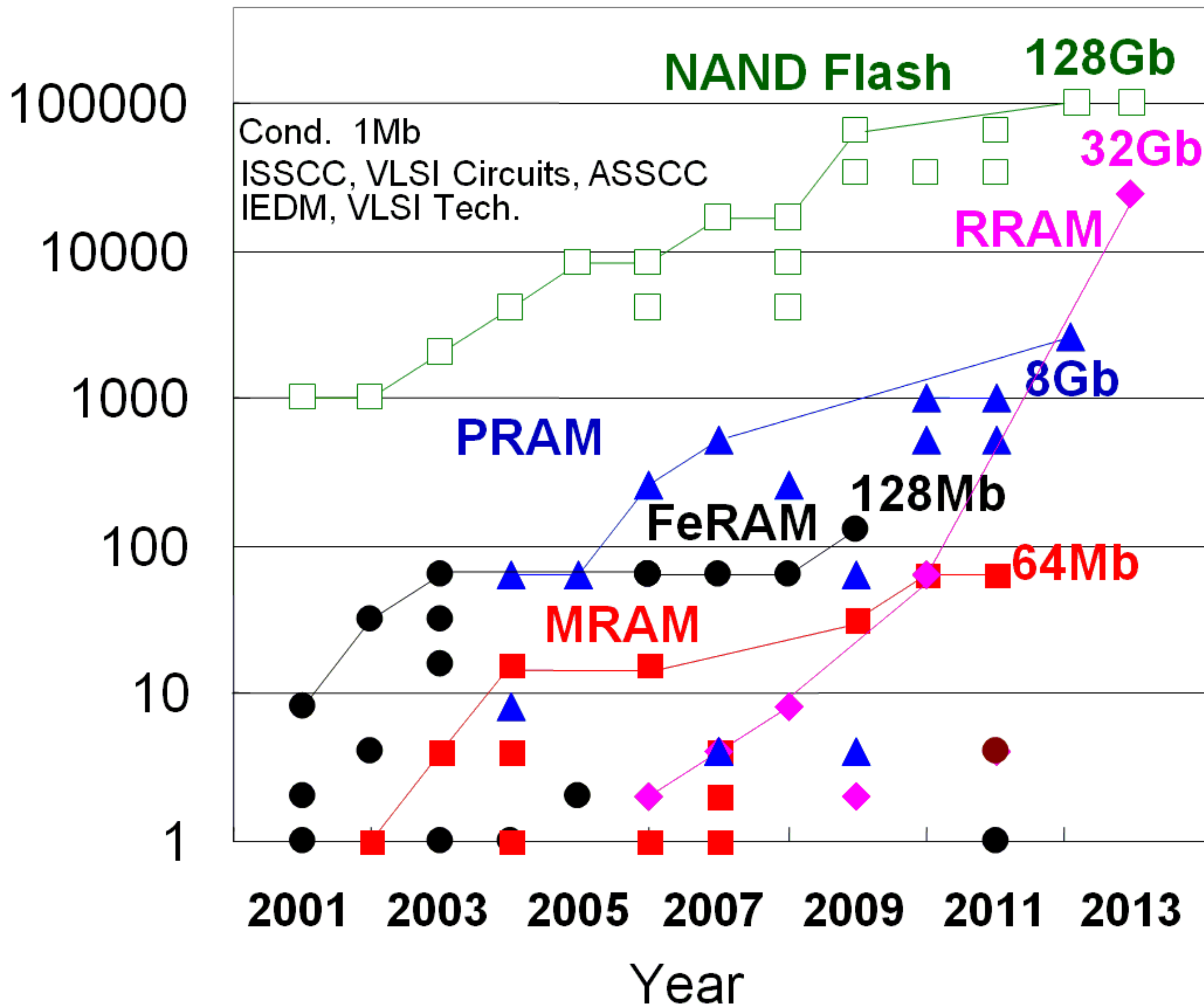

Figure 4: Memory capacity trend of emerging nonvolatile memories.

NAND FLASH MEMORY

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). Multiple bits per cell has proven to be effective in increasing the density. Figure 5 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 18 years. With scaling, device variability and error rates increase, requiring system designers to develop sophisticated control algorithms to offset this trend. Some of these are implemented outside the NAND silicon in the system memory controller, especially ECC and data management methods, for improved overall reliability. Possible future scenarios include 3D stacked NAND vertical gates as a solution to further increase the NAND density.

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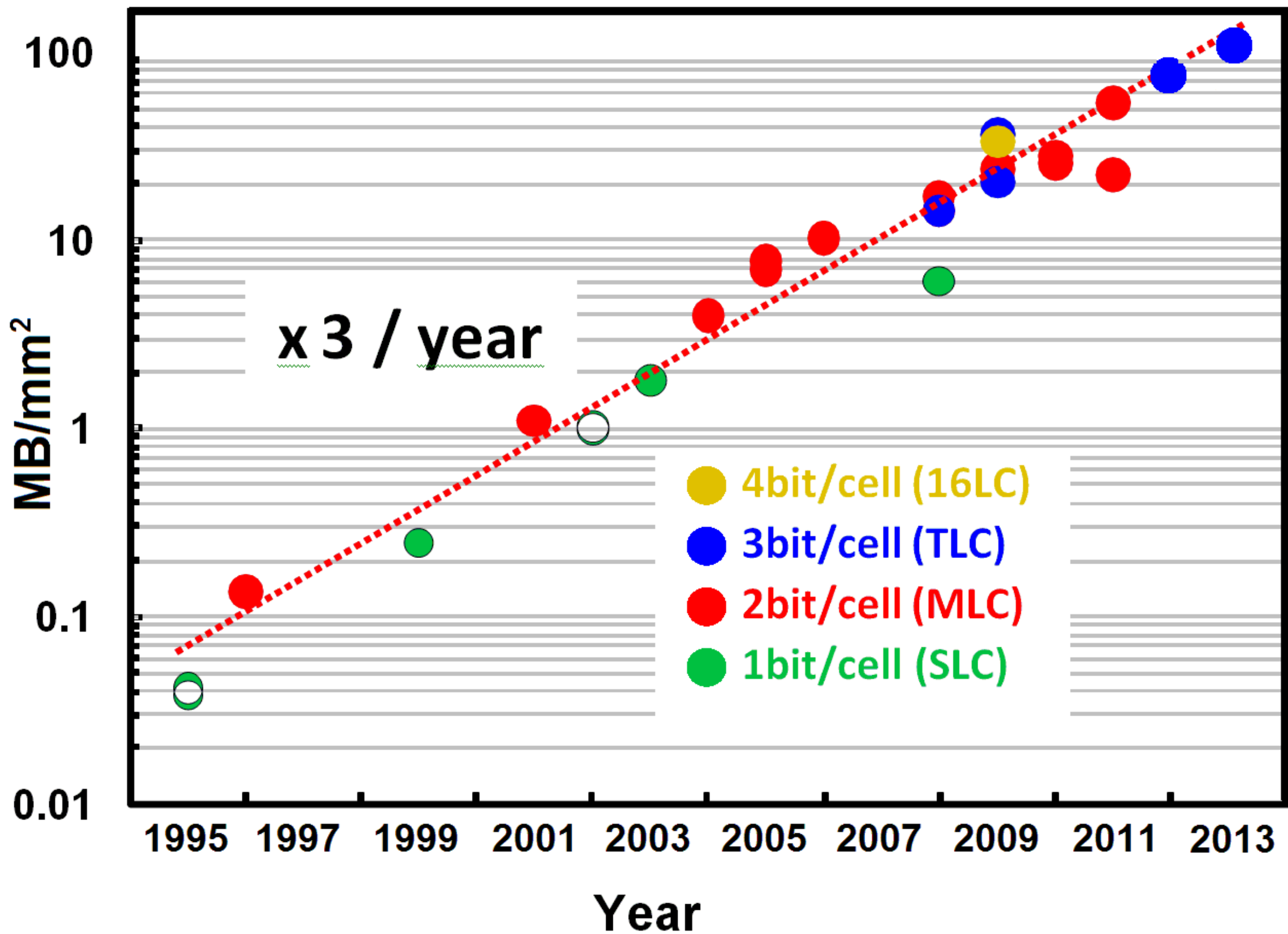

Figure 5: NAND Flash memory trends.

Some current state-of-the-art papers from ISSCC 2013 include:

- [12.1] A 130.7mm² 2-Layer 32Gb ReRAM Memory Device in 24nm Technology
- [12.5] A 128Gb 3b/cell NAND Flash Design Using 20nm Planar Cell Technology
- [18.2] An SRAM Using Output Prediction to Reduce BL-Switching Activity and Statistically-Gated SA for up to 1.9× Reduction in Energy/Access
- [17.1] A 6.4Gb/s Near-Ground Single-Ended Transceiver for Dual-Rank DIMM Memory Interface Systems
- A 45nm 6b/cell Charge-Trapping Flash Memory Using LDPC-Based ECC and Drift-Immune Soft-Sensing Engine

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RF – 2013 Trends

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF

Introduction
This year has shown increased innovation, integration, and technical maturity across RF frequency bands. This document outlines emerging RF trends that will be covered at ISSCC 2013.

ISSCC 2013 authors will present an ongoing drive toward **increasing levels of integration**. This trend can be seen in all areas of RF design from mm-Wave, to cellular, to imaging, to wireless sensors. In mm-Wave designs, higher system complexity (front-end, synthesizer, and baseband) is increasingly being integrated onto a single die. In cellular, the push for integration has led to a strong trend of architectures allowing better linearity and co-existence of these multiple bands and standards. In a related trend, there has been much research the last few years into various ways to remove costly and bulky SAW filters and duplexers. Some of these research areas include highly linear blocker-tolerant receivers, mixer-first receivers, feedback blocker cancellation, feed-forward blocker cancellation, N-path filters, and electrical balance of hybrid transformers. Strong work continues in the effort to integrate CMOS PAs while delivering viable power/efficiency performance. Finally, a clear trend this year was a significant number of chips demonstrated in 65nm CMOS compared to other technology nodes. This observation was noted across all frequency ranges and circuit topologies. The chips presented at ISSCC 2013 confirm that RF devices will continue to see larger levels of integration at the chip- and package-level for years to come.

Over the past decade, the papers submitted to ISSCC have indicated clear trends in the **continuing push to higher frequencies of operation in CMOS and BiCMOS**. This trend has continued this year for oscillators, mm-Wave amplifiers, and PAs. An emerging trend is the increasing complexity of systems operating in the 60-to-200GHz range. The push to ever-higher frequencies is being pursued by both industry and academia for various applications. An important application is high-data-rate communication. With the low-GHz frequency spectrum already overcrowded, researchers are continuing to target frequencies above 60GHz. Two other applications for products operating in these frequency bands are imaging and radar. These frequencies are desirable for such products due to their high spatial resolution and enablement of small antenna dimensions, allowing efficient beam-forming arrays. Another continuing trend is the integration of mm-Wave antennas into silicon substrates.

The combination of these two trends (that is, increased integration and the push to higher frequencies) has enabled a new class of fully-integrated **application-driven systems**. With the availability of many RF and mm-Wave building blocks in CMOS and BiCMOS, fully integrated solutions for specific emerging domains are appearing, both in the RF and the mm-Wave frequency range. These systems are built on a foundation of circuit-block innovations that have been developed over the past few years. Single-chip radars in RF and mm-Wave frequencies with improved resolution, improved efficiency, showing increasing levels of integration are being demonstrated. Similarly, new systems are being developed for ultra-wideband radar and mm-Wave wireless sensing. Demonstrations in the biomedical field are clearly moving from simple electrical measurements towards real medical measurements in realistic environments using systems-in-package (SiP).

We now discuss these two trends supported with data from chips to be presented at ISSCC 2013.

Complexity and maturity in the mm-Wave and sub-mm-Wave ranges

The high cutoff frequency of bipolar transistors and highly downscaled MOS transistors enables the realization of circuits and systems operating in the mm-Wave range. In the last few years, high-data-rate communication in the 60GHz band and car radar around 77GHz have garnered much attention. While the integration level in these domains is already quite high, we see an improvement of the performance of the building blocks (e.g. output power of PAs, spectral purity and tuning

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range of VCOs).

The 100GHz barrier for the operating frequency of silicon circuits has been broken a few years ago. Whereas initially elementary building blocks like a VCO and an amplifier operating above 100GHz have been realized, we now witness the trend of increasing complexity in circuits operating above 100GHz. Meanwhile, the electrical performances at the building block level improve: the output power of mm-Wave and sub-mm-Wave sources and PAs increases (Figure 1, Figure 2) and VCOs can operate at ever-increasing frequencies with a higher tuning range.

Co-existence and efficiency for cellular applications

RX and TX linearization: in the past few years there has been increasing interest in techniques to improve the linearity of transmitters and receivers. Improved linearity in the receivers will ease the requirements on the RF filtering of out-of-band blockers that can be accomplished, for instance, by placing a programmable notch filter in the RF path. TX linearity improvements will benefit performance parameters such as error-vector magnitude (EVM), ACLR and spectral purity.

Efficiency: PA efficiency improvements demonstrated this year will directly impact the battery life in portable applications. These efficiency improvement techniques include analog and digital pre-distortion, dynamic biasing and envelope tracking.

Digitally-assisted RF: the trend towards digitally-assisted RF continues and is increasingly applied to mm-Wave chips. More digitally assisted calibration techniques are being demonstrated in order to improve the overall performance of the transceiver by reducing the impact of analog impairments at the system level. These techniques include: spur cancelation/reduction, IIP2 improvements, and digital pre-distortion.

VCOs: there is a continuing trend toward improvements in phase-noise figure-of-merit (FOM) and power consumption due to circuit techniques like Class-C and Class-D VCOs. Figure 3 shows trends in VCO FOM performance of some of the most significant VCOs published over the past decade. This year's ISSCC shows clear contributions to this field.

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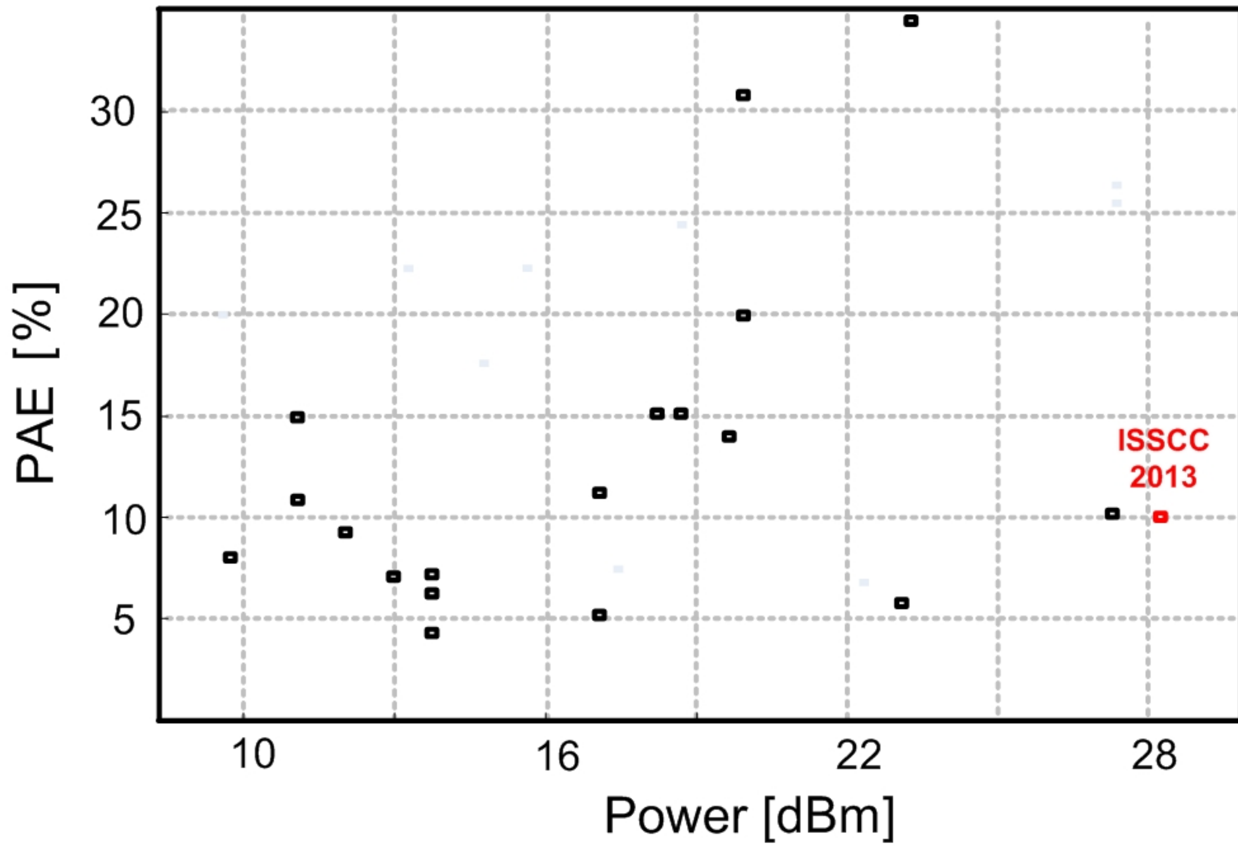

Figure 1: PAE (%) vs. output power for recent submicron mm-Wave CMOS PAs.

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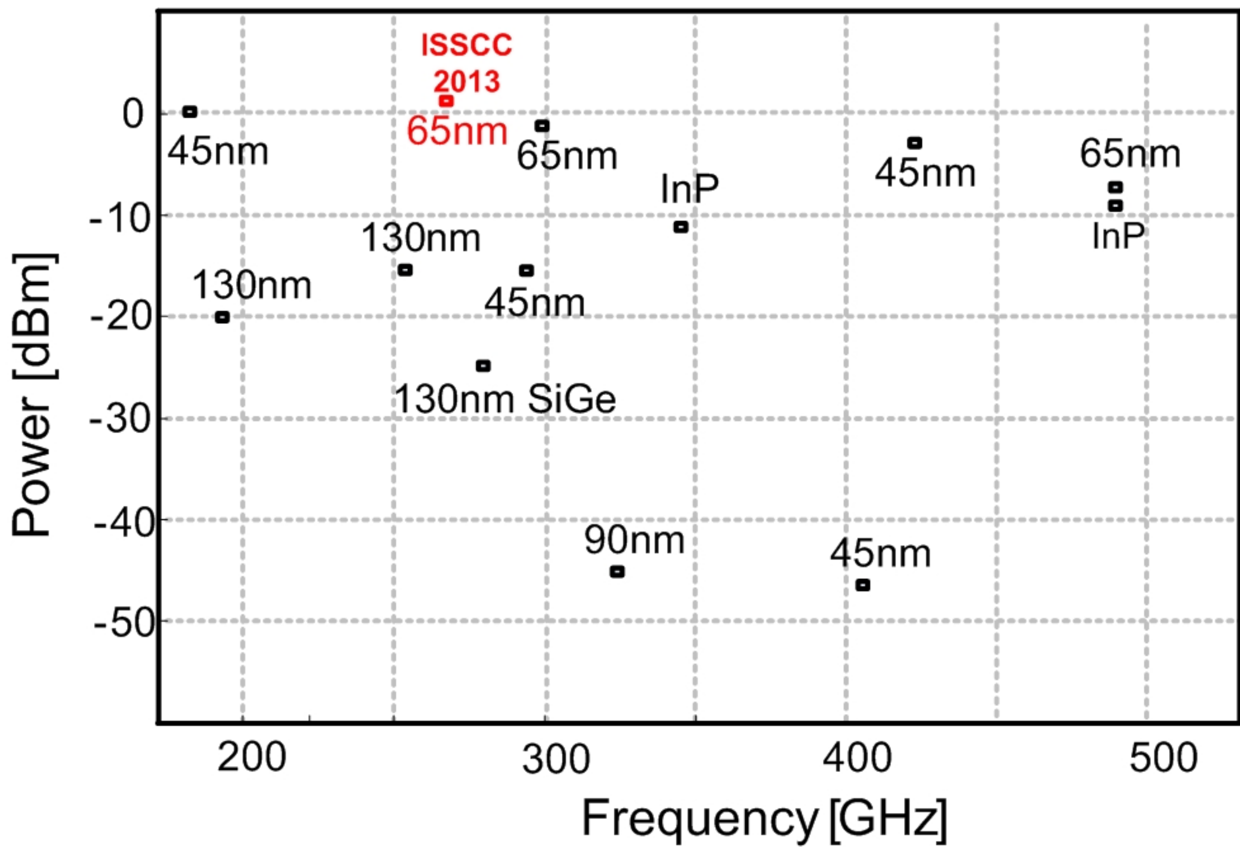

Figure 2: Output power versus frequency for mm-wave and sub-mm-wave sources.

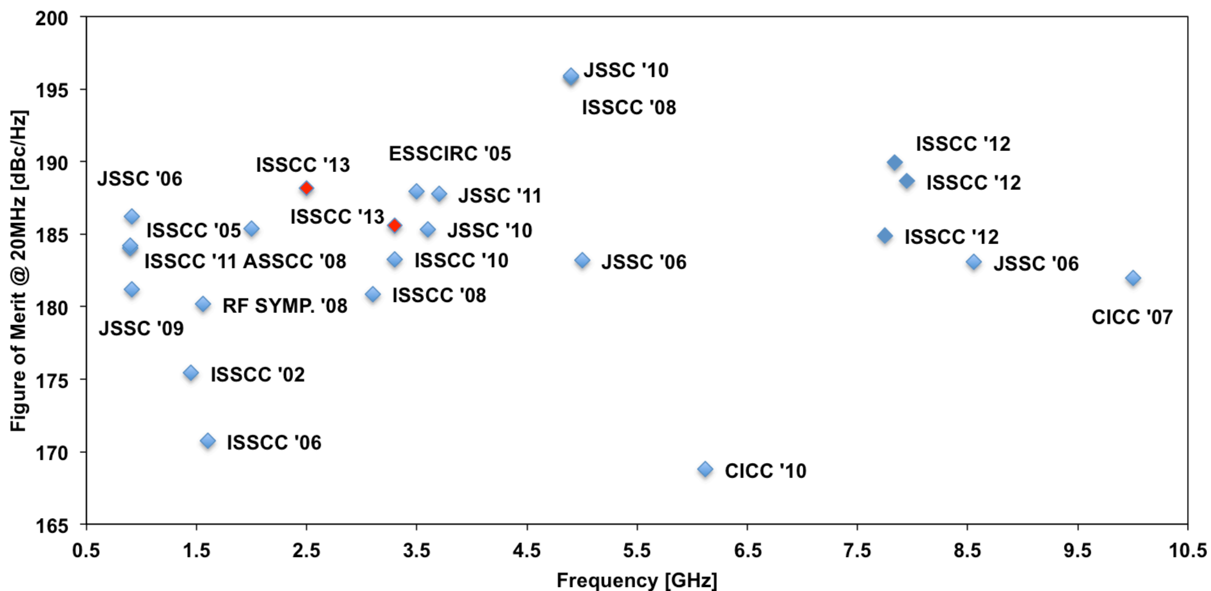

Figure 3: Phase-noise FOM at 20MHz offset frequency versus oscillation frequency.

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Technology Directions – 2013 Trends

Subcommittee Chair: Hoi-Jun Yoo, KAIST, South Korea, Technology Directions

Large-Area Flexible Electronics

Technology directions in the field of large-area and low-temperature electronics focuses on lowering the cost-per-unit-area, instead of increasing the number of functions-per-unit-area that is accomplished in crystalline Si technology according to the well-known Moore's law.

A clear breakthrough in research for large area electronics in the last decade has been the development of thin-film-transistor (TFT) processes with an extremely low temperature budget of (<150°C) enabling manufacturing of flexible and inexpensive substrates like plastic films and paper.

The materials used for these developments have for a long time been carbon-based organic molecules like pentacene with properties of p-type semiconductors. More recently, air-stable organic n-type semiconductors and amorphous metal oxides, which are also n-type semiconductors, have emerged. The most popular metal oxide semiconductor is amorphous Indium Gallium Zinc Oxide (IGZO), but variants exist (Zinc Oxide, Zinc Tin Oxide, and so on). The mobility of n- and p-type organic semiconductors has reached values exceeding 10 cm^2Vs, which is already at par or exceeding the performance of amorphous silicon. Amorphous metal oxide transistors have typical charge carrier mobility of 10 to 20 cm^2/Vs. Operational stability of all semiconductor materials has greatly improved, and should be sufficient to enable commercial applications, especially in combination with large-area compatible barrier layers to seal the transistor stack.

In the state-of-the-art p-type only, n-type only and complementary technologies are available. For the latter, all-organic implementations have been shown, but also hybrid solutions, featuring the integration of p-type organic with n-type oxide TFTs. Most TFTs are still manufactured with technologies from display-lines, using subtractive methods based on lithography. However there is a clear emphasis on the development of technologies that could provide higher production throughput, based on different technologies borrowed from the graphic printing world like screen and inkjet printing. The feature sizes and spread of characteristics of printed TFT technologies are still larger than those made by lithography, but there is clear progress in the field.

The prime application for these TFT families are backplanes for active-matrix displays, including in particular flexible displays. Organic TFTs are well-suited for electronic paper-type displays, whereas oxide TFTs are targeting OLED displays. Furthermore, these thin-film transistors on foil are well-suited for integration with temperature or chemical sensors, pressure-sensitive foils, photodiode arrays, antennas, sheets capable of distributing RF power to appliances, energy scavenging devices, and so on, which will lead to hybrid integrated systems on foil. Early demonstrations include smart labels, smart shop shelves, smart medical patches, etc. They are enabled by a continuous progress in the complexity of analog TFT circuits targeting the interface with sensors and actuators, to modulate, amplify and convert analog signals as well as progress in digital TFT circuits and non-volatile memory to process and store information.

In line with this trend, ISSCC 2013 features three papers representing the latest state-of-the-art of organic thin-film transistor circuits. A front-end amplifier array for EMG measurement is demonstrated for the first time with organic electronics in paper 6.4. Transistor mismatch and power consumption of the amplifier are reduced by 92% and 56%, respectively, by selecting and connecting the transistors trough a post-inkjet printing. Papers 6.5 and 6.6 present advances in analog-to-digital converters for sensing applications. Papers 6.5 demonstrates the first ADC that integrates on the same chips resistors and printed n and p-type transistors. The ADC achieves an SNDR of 19.6dB, SNR of 25.7dB and BW of 2Hz. In Papers 6.6, an ADC made only with p-type transistors is presented that has the highest linearity without calibration and that is 14 times smaller than previous works using the same technology.

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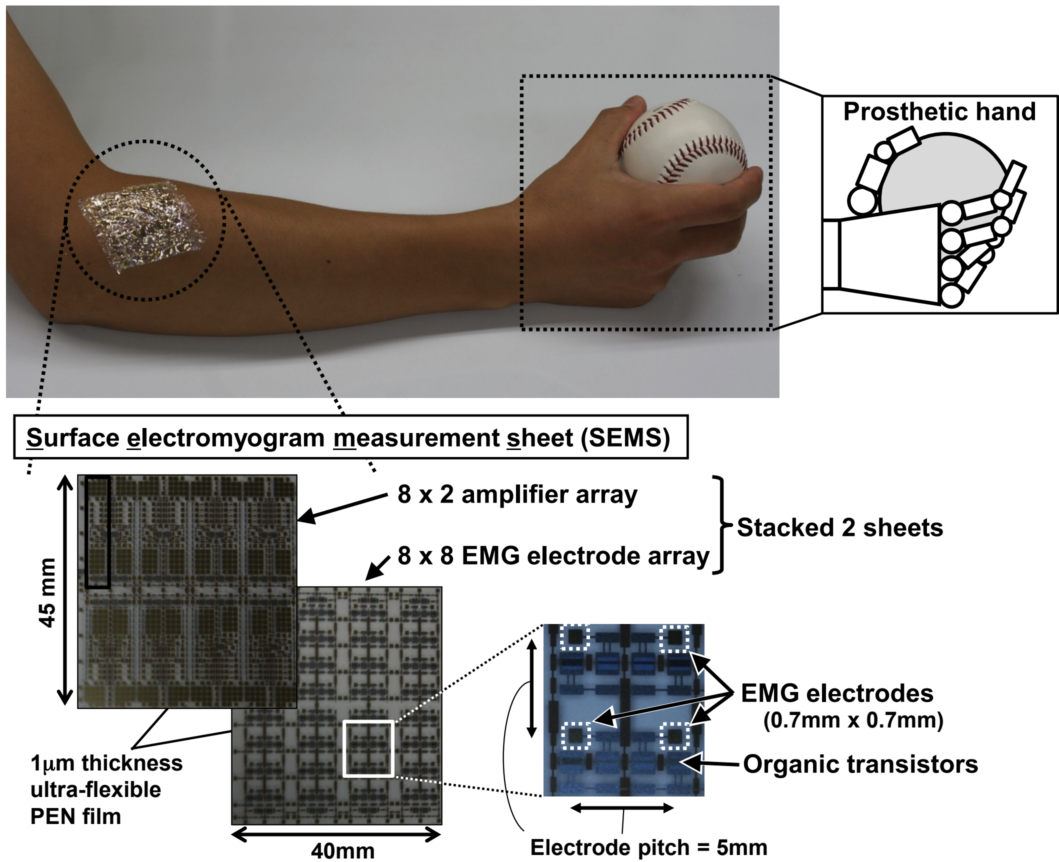

Emerging Integrated Non-Volatile Memories and Processors

With continuing technology scaling, enabling advances in computation along with energy efficiency will become even more important. A new trend is towards integration of non-volatile memory with logic for ultra-fast power-down/power-up while keeping the state of the computation has been appearing at ISSCC 2013. These technologies will impact future mobile platforms and industrial applications, making mobile computing truly ubiquitous.

ISSCC 2013 features Paper 11.1 by MIT that presents a D-Flip-Flop with ferroelectric capacitor non-volatile storage, enabling logic pipelines to be suspended and power-cycled without losing the state. It demonstrates a save-restore energy budget of just 3.4 pJ/bit. Paper 11.2 by Tohoku University describes an MTJ-based logic-in-memory solution for parallel motion vector prediction accelerator implemented with cycle-based power gating, demonstrating 4X reduction in leakage power and 2X reduction in active power.

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Wireless – 2013 Trends

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA. (Wireless)

Data rates for modern wireless standards are increasing rapidly and this is evident from the trend of cellular standards (shown in Figure 1). The data rate has increased 100X over the last decade and another 10X is projected in the next five years. This trend is partly contributed by using more complex modulations (e.g. using OFDM – Orthogonal Frequency Division Multiplexing - for better spectral efficiency) at the cost of digital signal processing (DSP). In addition, the expansion of channel bandwidth is also an effective way to achieve the data rate increase. This is seen in the wireless connectivity chart (e.g. 802.11) shown in Figure 2. The channel bandwidths for the WLAN standards increase from the traditional 20MHz (802.11g) all the way to 2.16GHz (802.11ad). Because the available spectrum is limited in the low GHz range, for >1GHz channel bandwidth, the carrier frequency is moving from 2.4/5GHz (802.11a/b/g/n/ac) to 60GHz (802.11ad) in the mm-Wave range. With the available spectrum in the 60GHz range, data rates up to 6.76Gb/s can be achieved. Design at mm-Wave frequencies comes with significant challenges, with academic research oriented to the reduction of the power, while industry focuses on product-quality robustness and standards compliance. A new generation of chipsets, compliant with WiGig and 802.11ad, is ready for production.

Since spectrum is scarce, new carrier aggregation techniques are being developed that can combine available channels in a flexible way, *e.g.* combining non-contiguous channels, or even channels at different frequency bands.
The new 802.11af standard aims to utilize "*TV white space*", unused legacy analog TV frequency bands below 1GHz. This will first be implemented using a database of available channels per geographical location, but eventually high-sensitivity spectrum sensing will be used to confirm the availability of the spectrum. The possibility of opening up this large amount of spectrum generates radio challenges, e.g. highly linear transceivers that can cover a very wide frequency range and various channel bandwidths. As a consequence of high-linearity and wideband design requirements, distortion cancellation and tunable RF channel-selection techniques are very critical. Most transceivers in this category are adopting digital calibration and analog-feedback techniques to increase the linearity performance for a flexible and tunable front-end to cover a wide range of frequencies.

As wireless technology becomes cheaper, it can be deployed in many devices, including sensors for monitoring environmental conditions. Wireless Sensor Networks (WSNs) require ultra-low-power radio to increase battery life and minimize the battery size, or better yet, eliminate the battery altogether by using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. A "wake-up radio" that monitors the channel and alerts the "main" radio when communication is requested becomes one of the main building blocks of the WSN node. Once the radio is awake, power efficiency becomes the main target for both high- and low-data-rate communication. Another approach is to duty-cycle the radio operation, i.e. only use the radio for short communication bursts, which requires fast turn-on techniques. Such WSNs will enable electronics for sustainability.

Similar to the evolution in cellular, ultra-low-power radios are now becoming multistandard, covering for example Zigbee, BTLE, and IEEE 802.15.6. Multistandard implementation implies radio-block sharing, and standards management, including modulation, frequency, bandwidth, power output, sensitivity …, while maintaining the low power consumption, which is one of the key success factors of such devices. Another main concern is the price. These multistandard radios must have small silicon area circuits in low cost packaging.

NFC (Near Field Communication) is becoming more and more popular. This new secure data wireless transmission mode is now embedded in smart phones and will become a de-facto requirement in the next years.

Digital architectures implementing radio functions are very efficient in deep-nm CMOS. In the past years Digital-PLLs were developed in the radio front-ends. Now, new digital approaches are being deployed in transmitters, targeting more flexibility

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of the RF front-end that leverages CMOS scaling for reduced power dissipation and area, simplifying integration in large SOCs, and empowering the next generation of wireless communications.

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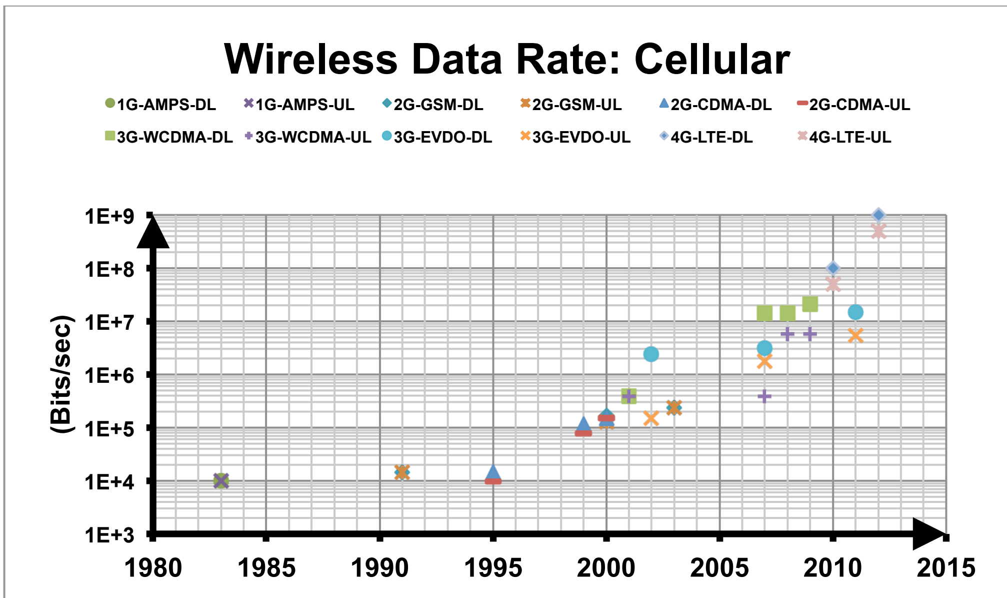

Figure 1: Data Rate Trend of Cellular Standards

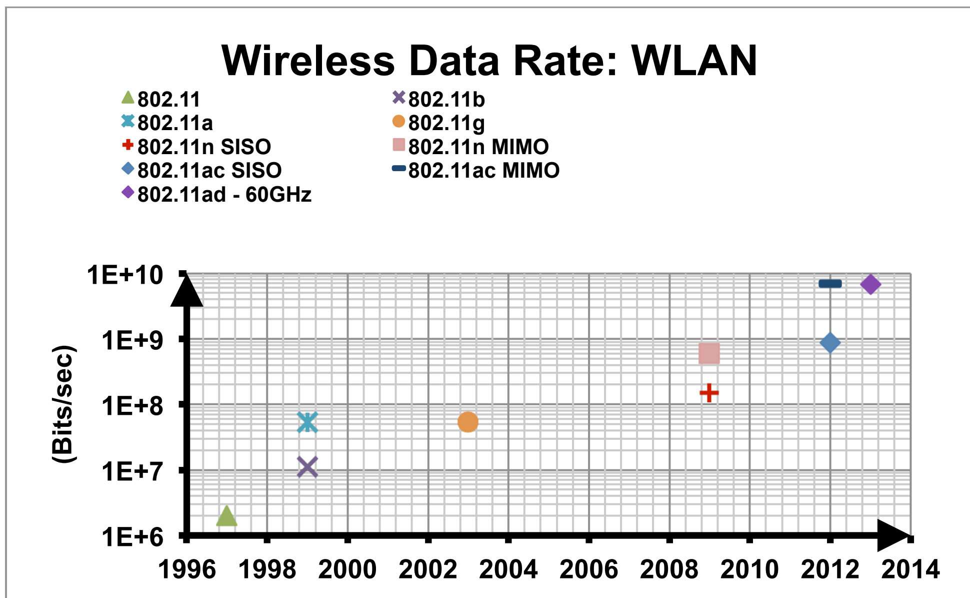

Figure 2: Data Rate Trend of Wireless Connectivity Standards (802.11x)

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Wireline – 2013 Trends

Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2-to-3× every 2 years. Demand for bandwidth is driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth is enabled by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems.

Power Consumption and Energy Efficiency

Power consumption for I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. However, there is a strong correlation between the energy efficiency and the distortions introduced by the channel. Figure 3 plots the energy efficiency (expressed in mW/Gbps, which is equivalent to pJ/b) as a function of Nyquist loss for recently reported transceivers. These transceivers cover a wide variety of standards and process nodes. Based on these data points, the scaling factor between link power and signaling loss is approximately unity, meaning that required link power approximately doubles with every additional 6dB of channel loss. As a result, simply increasing per-pin data rates with existing circuit architectures and channels while scaling transistors is not a viable path given fixed system power limits. To address this issue, recent link research has focused on reducing power through both circuit and channel innovation. There have been a number of recent advances that reduce power through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. Based on the relationship between channel loss and energy efficiency, power can also be reduced by changing the interconnect itself to either reduce the total loss or increase the interconnect density. Examples of this from ISSCC include stacked die TSVs and proximity interconnect, silicon interposers, on-package I/O, and low-loss flexible interconnect. Presentations at ISSCC 2013 move the state-of-the-art well below 1pJ/b for short-range links. A 20Gb/s chip-to-chip transceiver consuming just 540fJ/b employs single-ended ground-referenced signaling across high-density package interconnects [23.3]. Another demonstrates 1Tb/s aggregate bandwidth across low-loss flexible cabling consuming 2.6pJ/b [23.2].

Electrical

Some types of channels, especially those related to medium-distance electrical I/O like server backplanes, have to support high data rates along with high loss. Others, like DDR, must contend with increasing amounts of crosstalk in addition to channel loss. For these links, the key to scaling has been improvements in clock jitter and equalization. There are several recent examples of transceivers able to signal across 30 to 35dB of loss at Nyquist at data rates up to 28Gb/s. These transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. In some cases, equalization is being done in the digital domain after first converting the data signal using a 5-to-6b ADC. Although the energy efficiency for these systems tends to be lower than in conventional equalization approaches, they enable more complex and flexible equalization techniques as well as equalization power that may scale more gracefully. A number of CDR circuit techniques have also been developed for these high-loss transceivers, including

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digital CDRs that employ baud-rate sampling, oversampling, and even blind sampling techniques. Papers at this year's conference represent the fastest link components reported to date, including a 66Gb/s 3-tap DFE consuming just 46mW without loop unrolling [2.2] and a 48Gb/s 88mW TX [2.6], both in standard 65nm CMOS. They also demonstrate significant advances in fully-integrated high-speed transceivers, including a 39.8-to-44.6Gb/s chipset in 40nm CMOS [2.3] and several 32Gb/s TX and RX equalizers compensating up to 40dB of channel loss [2.5, 2.7].

Optical

As the bandwidth demand for traditionally electrical wireline interconnects has accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnects. Relative to electrical interconnects, optics provides lower loss and potentially higher density through techniques like wavelength-division multiplexing. Optical components – including VCSELs, Mach-Zehnder Interferometers (MZI), optical ring modulators, and photodetectors – are simultaneously being developed for higher performance, lower power, and higher degrees of integration with standard CMOS processes. Circuit design techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. ISSCC 2013 includes several examples of 25Gb/s optical transceivers, including an RX that consumes only 4.9pJ/b. The conference highlights significant advances in Si photonic integration, including a 20Gb/s driver and associated silicon photonic MZI [7.7] and a 2.5Gb/s driver and ring modulator designed and fabricated in a standard CMOS process [7.5].

Concluding Remark

Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2013.

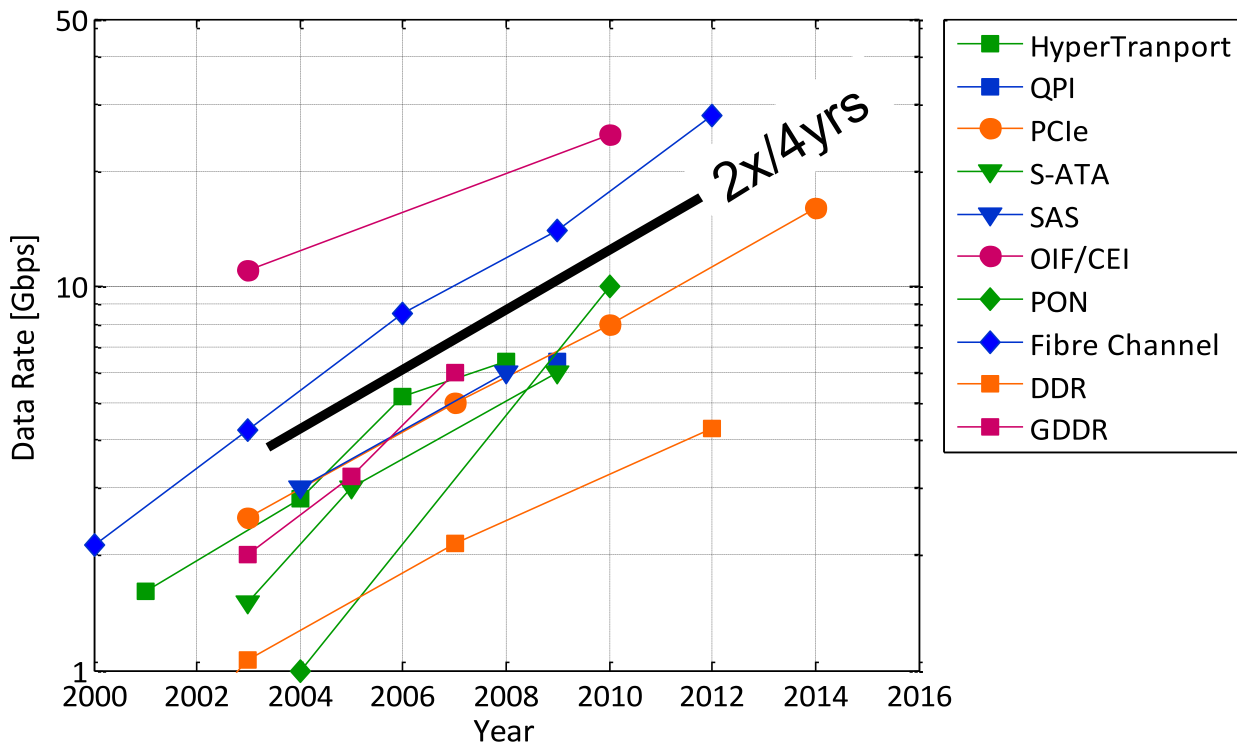

Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

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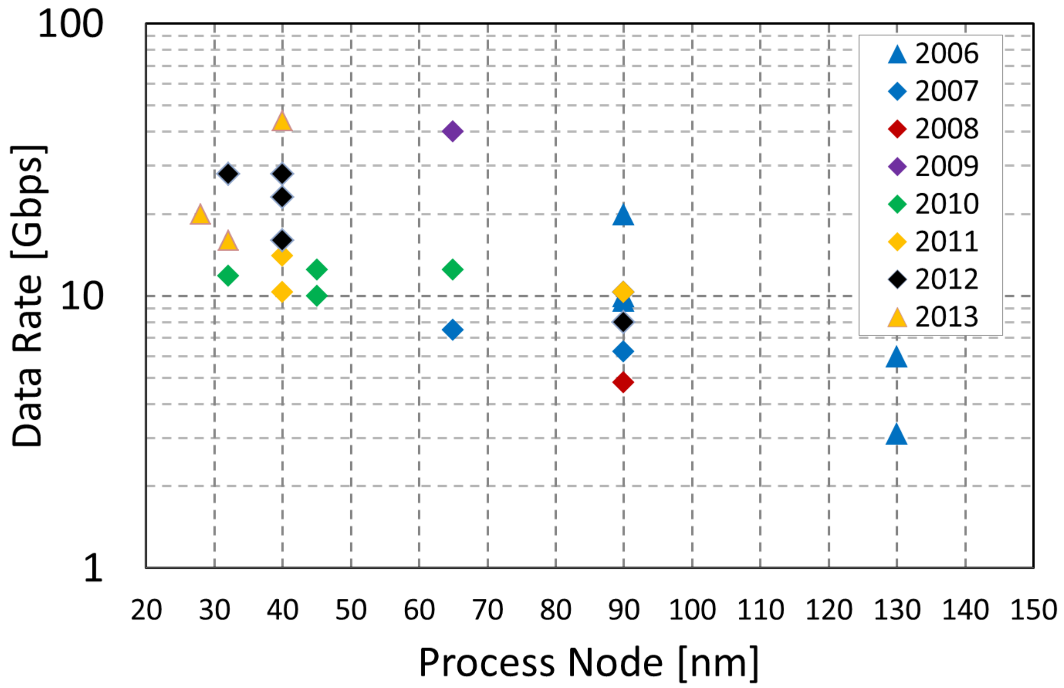

Figure 2. Data Rate vs. Process Node and Year.

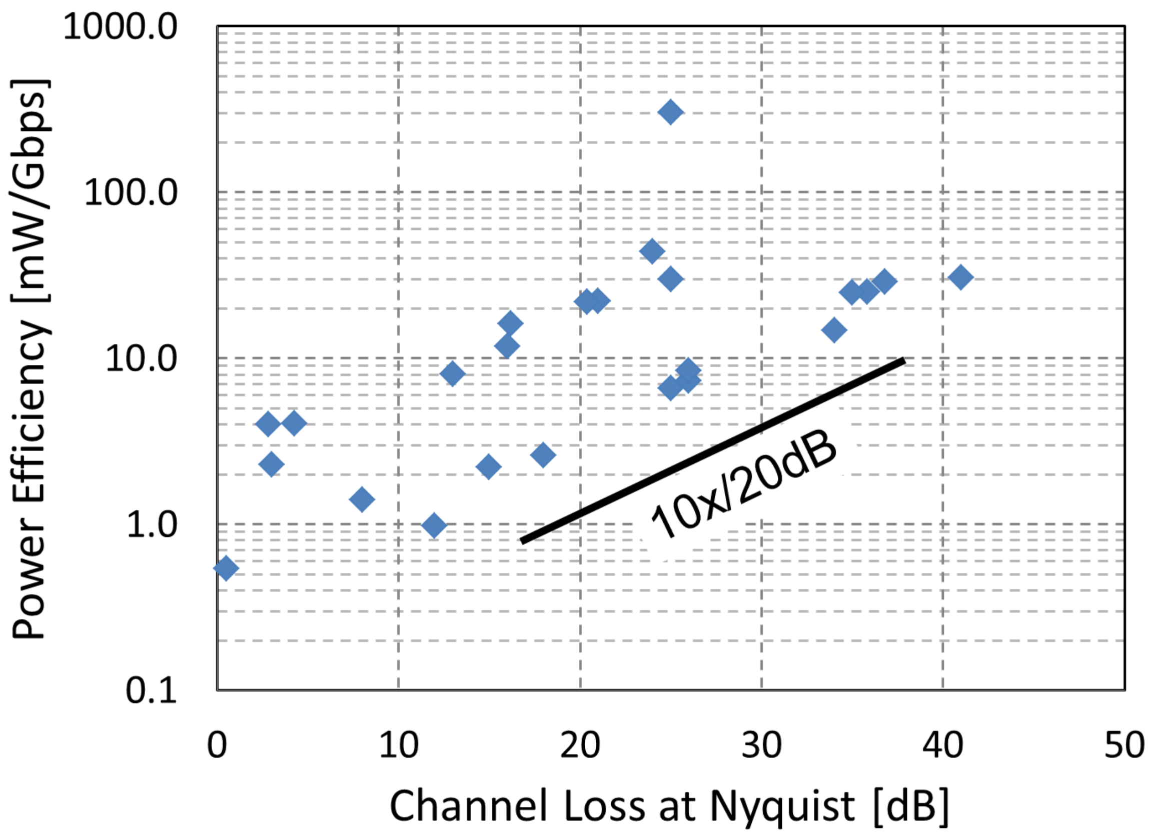

Figure 3. Transceiver Power Efficiency vs. Channel Loss.

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CONTACT INFORMATION

TECHNICAL EXPERTS

ANALOG Subcommittee Chair: Bill Redman-White Southampton University Office: +44-2380-593617 wrw@ecs.soton.ac.uk Press Designates: Tony Chan Carusone, University of Toronto Tsung-Hsien Lin, National Taiwan University Michiel Steyaert, KU Leuven	MEMORY Subcommittee Chair: Kevin Zhang Intel Office:503-613-9144 kevin.zhang@intel.com Press Designates: Colin Bill, Global Founderies Tadaaki Yamauchi, Renesas Electronics Daniele Vimercati, Micron Technology
DATA CONVERTERS Subcommittee Chair: Boris Murmann Stanford University Office: 650-725-7042 murmann@stanford.edu Press Designates: Takahiro Miki, Renesas Electronics Lucien Breems, NXP Semiconductors Harry Lee, Massachusetts Institute of Technology	RF Subcommittee Chair: Andreia Cathelin STMicroelectronics Office:+33-4387-2175 andreia.cathelin@st.com Press Designates: Taizo Yamawaki, Renesas Mobile Corp. Piet Wambecq, imec Brian Otis, University of Washington
ENERGY-EFFICIENT DIGITAL Subcommittee Chair: Stephen Kosonocky Advanced Micro Devices Office: 970-226-8152 Stephen.kosonocky@amd.com Press Designates: Vasantha Erraguntla, Intel Victor Zyuban, IBM T.J. Watson Kees Van Berkel, ST-Ericsson	TECHNOLOGY DIRECTIONS Subcommittee Chair: Hoi-Jun Yoo KAIST Office: +82-42-350-3468 hjyoo@kaist.ac.kr Press Designates: Shinichiro Mutoh, NTT Eric Colinet, CEA-LETI Ali Keshavarsi, Cypress
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GENERAL CONTACTS

Program Chair, ISSCC 2013
Bram Nauta
University of Twente
Office: +31-53-489-2655
b.nauta@utwente.nl

Program Vice-chair, ISSCC 2013
Trudy Stetzler
Texas Instruments
Office: 281-274-3736
t-stetzler1@ti.com

Press-relations Liaison
Kenneth C. Smith
University of Toronto
Office: 416-418-3034
lcfujino@cs.com

Press Coordinator
Alice Wang
MediaTek
Office: 214-810-2347
aliwang@gmail.com

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Editor-in-Chief: Alice Wang

Editor-at-Large: Kenneth C (KC) Smith

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