2012

PRESS KIT

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The material presented here is preliminary.
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ISSCC
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2012
Conference Overview

CONFERENCE THEME

The ISSCC 2012 Conference theme is:

“Silicon Systems for Sustainability”

What can we do for Earth’s sustainability? Sustainability must be the paramount theme for the future of human society! Electronics will play a primary role: more robust and sustainable silicon systems will emphasize re-usability, re-organization, re-configurability, self-repair, and self-organization.

Currently, environmentally-supportive sustainable systems are exemplified by silicon technology used in electric-automotive and smart power-grid systems. Potentially, silicon technology and its applications will provide solutions for the realization of smarter recycling sustainable global systems. To fulfill this goal, system-level approaches, as well as technology and circuit advancements will play important roles!

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PAPER STATISTICS

OVERALL:

- **4** papers invited
- **628** papers submitted to ISSCC 2012
- **202** papers accepted
    - **68** papers from North America, including
        - **33** Industry papers
        - **35** University papers
        - **0** Institution/Lab papers
    - **73** papers from the Far East, including
        - **32** Industry papers
        - **37** University papers
        - **4** Institution/Lab papers
    - **61** papers from Europe, including
        - **14** Industry papers
        - **33** University papers
        - **14** Institution/Lab papers
- **28** Sessions, over 3 days

INTERNATIONAL SCOPE:	2012	2011	2010	2009	2008
Americas:	34%	38 %	41 %	38 %	43 %
Far East:	36%	33 %	31 %	35 %	28 %
Europe:	30%	29 %	28 %	27 %	29%

WIDE COVERAGE:	2012	2011	2010	2009	2008
Analog:	13%	10 %	9 %	11 %	9 %
Data Converters:	8%	8 %	7 %	7 %	10 %
Energy-Efficient Digital:	7%	6 %	6 %	6 %	5 %
High-Performance Digital:	10%	7 %	10%	4 %	7 %
IMMD:	13%	14 %	12 %	12 %	11 %
Memory:	10 %	10 %	11 %	9 %	12 %
PLL:	--	--	6 %	--	--
RF:	10%	12 %	8 %	11 %	11%
Technology Directions:	9%	10 %	12 %	13 %	12%
Wireless:	9%	11 %	11 %	13 %	11%
Wireline:	10%	11 %	8 %	14 %	11%

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PLENARY SESSION

Paper 1.1:
Flash Memory - The Great Disruptor!

Eli Harari
Co-Founder and Former CEO and Chairman (retired), SanDisk Corporation, Milpitas, CA

This presentation will discuss:

- The two-decade advance of Flash-memory chip technology through 17 technology nodes, in each of which the number of bits-per-chip doubled, outpacing Moore's Law.
- As 20nm NAND Multi-Level Cell (MLC) enters volume production, Flash has become the technology driver for the semiconductor memory industry.
- The introduction of System-Flash and MLC in the 1990s transformed Flash from primarily a code-store memory to a low-cost data-store medium.
- The arrival of Flash coincided with, and benefitted from, the rising importance of digital consumer electronics, the Internet, and wireless mobile devices.
- The ability of Flash to sustain growth will hinge on new and innovative System-Flash solutions, including advanced SSD (Solid-State Disk) and embedded Flash that will be custom-tailored for specific usage cases.
- Flash will enable new cloud-based business models by enhancing user-experience at both the first level (fast cloud storage) and last level (secure mobile storage) of the mobile network.
- By 2020 NAND and post-NAND 3D Flash will eclipse all other storage media, whether semiconductor, magnetic, or optical, thereby completing a history of technological transformation.

Paper 1.2:
The Role of Semiconductors in the Energy Landscape

Carmelo Papa
Senior Executive VP/GM, STMicroelectronics, Geneva, Switzerland

This presentation will discuss:

- The exponential increase of world energy consumption which makes energy management one of the most urgent topics of this century and a key driver for the semiconductor and electronics component evolution.
- The Kyoto Protocol on Climate Change which targets limitation of global temperature increase to 2°C maximum by 2030.
- Increasing electricity production from renewable and bio-fuel sources, and increasing energy efficiency with a wider adoption of microelectronics.
- Electricity consumption which comes from three major application areas: Power Supply (24%), Lighting (21%), and Motor Control (55%), where semiconductors can play a relevant role through improvements in silicon technologies, innovative IC topologies, and system-design methodologies.
- The replacement during the past 10 years of universal motors by brushless motors using powerful and cost-effective microcontrollers with embedded advanced software algorithms.
- New Class-A+ Home Appliances with average energy efficiency will increase by 30% for a saving of up to 50 TWh by 2020, the equivalent of today's electricity consumption by Portugal and Latvia.
- CFL and LED lighting technologies employing cost effective IC solutions, which provide significantly large power reduction.

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- “More Moore” and “More than Moore” technologies will play an important role in the energy revolution of the Smart Grid, particularly in Power Conversion and Connectivity Systems.
- Power Conversion using finer lithography geometries which will allow miniaturization and integration at the component level, and Connectivity Systems using heterogeneous system integration which will allow the introduction of more functions like micro-batteries, smart sensors, plastic electronics, energy harvesting, etc.
- In summary, the semiconductor-driven revolution will have an enormous impact on sustainability, quality of life, and societal change.

Paper 1.3:
Take the Expressway to Go Greener

Yoichi Yano
Executive VP, Renesas Electronics, Tokyo, Japan

This presentation will discuss:

- Society is going green.
- We see green initiatives are appearing in various industry sectors, such as solar power generation, eco-friendly white goods and consumer electronics, and ”green cars” based on hybrid technology.
- The world demands greener products for a green society to an extent that we have never before experienced.
- The semiconductor technology has led the power-reduction thrust by monitoring, controlling, and managing power consumption.
- In power control the key product is a lesser-known device: the microcontroller (MCU).
- Historically, the microcomputer appeared on the market in the early 1970s, then evolving into two product streams - the Microprocessor (MPU) for personal computers and servers, and the Microcontroller (MCU) for embedded control.
- In 2010, 13 billion MCUs were shipped - 20x more than in 1987, corresponding to 400 pieces shipped EVERY SECOND!
- Now MCUs are “everywhere you imagine”; we see more than one hundred such devices in a modern home.
- MCUs have enjoyed wide acceptance in various embedded applications because of their ease to use, wide variety products availability, and their self-contained nature – everything is integrated on a tiny piece of silicon having a small foot print, using low-power, providing adequate performance, all at low cost.
- The strength of an MCU comes from its programmability using on-chip flash-memory technology.
- While Flash was introduced to MCUs in the early 1990s, wide spread use of Flash technology in low-end MCUs was not until the early 2000s.
- Flash-based MCUs have changed the world because of their programmability in a very small footprint using low-power technology.
- A recently developed MCU operates from a battery source of only one lemon! Tremendous amounts of power are potentially saved by the use of enormous numbers of very-low-power MCUs in a myriad of applications.
- MCUs are slated to evolve further to save even more power in wide spread applications involving “energy harvesting”.
- Alternatively, the automotive industry requires higher real-time performance with much a higher level of functional safety in addition to lower power.
- Such requirements will drive a new generation of Flash MCU on the expressway to going greener!
- MCU is truly the core technology for making everything greener!

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Paper 1.4:
Sustainability in Silicon and Systems Development

David Perlmutter
Executive VP/GM, Intel, Santa Clara, CA

This presentation will discuss:

- Computing solutions will have an even more profound impact on the world.
- A recognition that we have a responsibility to “care for the planet” by developing technology solutions to address major global problems while reducing our own environmental impact is important.
- A global sustainability strategy specifies environmental goals and technology for the environment.
- Designing for energy efficient performance includes efforts “outside the box”, “inside the box”, and “inside the socket”.
- Outside the box efforts include high-voltage distribution & high-temp (above 25C) operation, and data center management software.
- Inside the box strategies include:

  (1) Re-architecting platforms and bus standards to reduce idle power

  (2) Voltage regulator design for high efficiency across an extended range

  (3) OS power management – managing idle states, dynamic voltage frequency scaling

  (4) Optimizing software to enable quiet idle periods.

- Inside the socket techniques are:

  (1) Power gating: cores, caches and blocks, sleep devices

  (2) Clock gating: local fine-grained and coarser regional

  (3) Warm design technology: power-aware techniques to maximize energy-efficiency

  (4) Multi-core design: performance from parallelism, not from escalating frequency

- Key trends in silicon, systems and data center design methodologies that enable ‘always on’ capabilities while ensuring that energy-efficient improvements of Moore’s Law will continue to serve the environment, well into the future.

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TECHNICAL HIGHLIGHTS

ANALOG:

- Highest efficiency power-conversion system for grid-connected photovoltaic (PV) cells [5.5]
- Improved regulation addresses a key challenge for LED lighting [16.3]
- Analog signal processing moves to temporal domain [21.2]
- Highest CMRR instrumentation amplifier [21.9]

DATA CONVERTERS:

- Very high sampling rate RF ΔΣ data converters [8.3, 8.6]
- Revolutionary opamp architecture lowers power [27.2]
- Pipelined coarse/fine opamp extends low-power/high-performance tradeoff [27.3]

ENERGY-EFFICIENT DIGITAL:

- First ever complete 60GHz transceiver in silicon [12.3]
- High-definition video engine for smartphone SoC features support for 14 different video standards [12.6]
- World's first single-chip 8k×4k video resolution Super Hi-Vision (SHV) decoder implementation [12.7]
- Subthreshold 32b processor operates down to 200mV in 65nm CMOS [28.4]
- Bubble Razor – an architecture-independent approach to timing-error detection and correction [28.6]

HIGH-PERFORMANCE DIGITAL:

- Intel introduces the first processor built in 22nm technology using 3D transistors [3.1]
- Oracle's next-generation SPARC SoC runs at 3GHz providing 7× performance improvement [3.3]
- 8.162 PETAFLOPS —the highest floating point performance ever achieved [10.8]
- Samsung presents a tiny all-digital phase-locked loop for mobile applications [14.1]
- The world's first 22nm digital phase-locked loop using Intel's 3D transistors [14.4]

IMAGERS, MEMS, MEDICAL AND DISPLAYS:

- First analog motion artifact suppression technique that does not degrade the performance of an analog front-end [6.5]
- Resonant coupling between a capacitive sensor and a readout circuit [11.4]
- First use of a MEMS-thermistor for high-resolution, high-stability temperature sensing, along with an innovative readout circuit [11.6]
- CMOS image sensor with high-speed burst capture rate of 10Mframes/s and burst readout rate of 1Tpixels/s [22.2]
- Real-time color and 3D imaging over 1-to-7m distances [22.7]

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MEMORY:

- First ever reported 1.2V DDR4 SDRAM [2.1]
- World's smallest embedded SRAM cell (and first 22nm node tri-gate 6T-SRAM demonstration) [13.1]
- Highest-ever density NAND Flash memory (and fastest 3b/cell write performance of 18MB/s) [25.8]

RF:

- A tri-band WCDMA CMOS PA with lowest current ever reported [4.7]
- World's first reported RF feedback loop for power efficiency and linearity enhancement [4.6]
- An integrated Terahertz, 1k-pixel real-time camera in 65-nm CMOS [15.1]
- A 16 pixel image sensor integrates antenna and power detectors while achieving record sensitivity [15.2]
- A reconfigurable DCO breaks power/complexity trade-off for different standards [20.4]

TECHNOLOGY DIRECTIONS:

- A compact electro-acupuncture patch [17.3]
- A miniature wirelessly powered implant with locomotion and remote control [17.6]
- A self-powered wearable lifestyle system that uses organic electronics [18.1]
- The first NEMS resonator co-integrated with a 0.3mm fully depleted SOI technology [18.7]
- An optically reconfigurable sensor node with complete power-management unit, power-on reset, as well as brown-out detection for CPU and memory integrity preservation [23.2]

WIRELESS:

- Dramatic application of tunable RF channel-selection for software radios [9.3]
- The first application of an outphasing power amplifier at 60GHz [9.5]
- First beamforming transmitter with 1° phase resolution [26.3]

WIRELINE:

- 3D I/O drives 6-TSV chains at 5.2Gb/s with 0.50mW/Gb/s [7.7]
- First 28Gb/s transceiver addressing medium reach, 35dB loss, electrical channel in 32nm SOI CMOS [19.1]
- A spectrally-efficient multi-carrier interconnect operating at >20Gb/s at millimeter-wave frequencies in the 50GHz to 90GHz range [19.5]

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ISSCC 2012
SESSION OVERVIEWS
AND HIGHLIGHTS

CONDITIONS OF PUBLICATION

PREAMBLE

- The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2012 in February in San Francisco
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    - That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 59th appearance of ISSCC, on February 19th to the 23th, 2012, in San Francisco.

> This and other related topics will be discussed at length at ISSCC 2012, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 19-23, 2012, at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview : HIGH BANDWIDTH DRAM & PRAM

MEMORY SUBCOMMITTEE

Session Chair: Joo Sun Choi, Samsung, Korea
Session Co-Chair: Daisaburo Takashima, Toshiba, Japan

Subcommittee Chair: Kevin Zhang, Intel, OR, Memory Subcommittee

VLSI applications today require high-volume power-efficient DRAM. Achieving high bandwidth at low voltages remains a significant challenge for DRAM design. In ISSCC 2012, a new DDR4 4Gb DRAM demonstrates a data rate up to 3.2Gb/s/pin for server applications. A new LPDDR3 4Gb DRAM for mobile applications has a data rate up to 1.6Gb/s/pin. DRAM technology has advanced to 23nm and 4Gb density is becoming mainstream. For the emerging memory technology of PRAM (phase-change RAM), an 8Gb chip has been now realized with the minimum feature-size of 20nm. Significant progress is also made in the TSV (through-silicon via) technology along with new I/O circuit design for more power-efficient memory interfaces. The papers in this session present the latest technologies and high-bandwidth circuit techniques to improve the performance and density of both DRAM and PRAM.

- In Paper 2.1, Samsung discloses the first 1.2V DDR4 4Gb SDRAM with a 30nm CMOS technology. A high bandwidth of 3.2Gb/s/pin, which is 2× faster than existing DDR3 DRAM, is realized by stable signal transfer using a dual-error detection scheme, a gain-enhanced buffer, and a PVT-tolerant data-fetch scheme.
- In Paper 2.2, Hynix introduces the first 1.2V 2Gb SDRAM with a 4-bank group. A half-page architecture minimizes the active bank current by 8.4%. A pre-emphasis driver enhances the data eye to be stable up to 4Gb/s/pin. Both CA parity and simultaneous CRC/DBI enable such a reliable data transfer.
- In Paper 2.3, Hynix demonstrates the smallest 23nm 30.9mm2 4Gb DDR3 SDRAM by using an open bitline architecture with 6F2 cell. The hybrid local sense amplifier guarantees robust read operation, and a new dummy-less array architecture minimizes the die area.
- In Paper 2.4, Samsung describes a 1.2V 82mm2 4Gb low-power DDR3 DRAM fabricated with a 30nm process. The CA training and write-leveling technique achieves a data rate of 1.6Gb/s/pin. A temperature-compensated refresh and comprehensive partial array refresh minimizes refresh current by 50mA.
- In Paper 2.5, Samsung demonstrates the first 1.8V 8Gb phase-change memory (PRAM) which is 8× higher capacity than the previous work by developing an advanced 20nm process technology. A 256b parallel write with multiple wordline activation realizes 40MB/s write throughput by using an 800Mb/s/pin LPDDR2 interface.
- In Paper 2.6, Korea U shows a DLL-based I/O timing self-aligner to reduced I/O data conflicts for stacked DRAMs by using a through-silicon via (TSV) interface. This alignment technique realizes the power and performance to 283.2μW and 800Mb/s/pin, respectively, and a leakage controller also suppresses leakage power by 90.5%.
- In Paper 2.7, UCLA presents a dual (Base+RF) band simultaneous bi-directional data transfer of 8Gb/s/pin and 4pJ/pin by using a single transmission line structure. The inductively coupled to terminated transmission through a transformer enables a 5Gb/s BB-band and a 3 Gb/s RF-band with a BER of 10-12.
- In Paper 2.8, Keio U demonstrates a 7Gb/s/link non-contact memory module for multi-drop bus. Equipartitioned energy design for each module drop suppresses reflection. Aggregate data bandwidth of 56Gb/s with 8 channels is demonstrated.

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Session 2 Highlights : HIGH BANDWIDTH DRAM & PRAM

[2.1] A 1.2V 30nm 3.2Gb/s/pin 4Gb DDR4 SDRAM with Dual Error Detection and PVT-Tolerant Data Fetch Scheme

Paper Authors : K. Sohn, T. Na, I. Song, Y. Shim, W. Bae, S. Kang, D. Lee, H. Jung, H. Jeoung, K-W. Lee, J. Park, J. Lee. B. Lee, I. Jun, J. Park, H. Choi, S. Kim, H. Chung, Y. Choi, D-H. Jung, J. Choi, B. Moon, J-H. Choi, B. Kim, S-J. Jang, J. Choi, K. Oh
Paper Affiliation : Samsung Electronics, Hwasung, Korea

Subcommittee Chair : Kevin Zhang, Intel, Hillsboro, OR, Memory Subcommittee

CONTEXT AND STATE OF THE ART

- DDR3 using 50nm technology has been established as the leading DRAM technology in the past year and has entered the mass-production phase. However, new systems are demanding higher DRAM bandwidth along with higher capacity

TECHNICAL HIGHLIGHTS

- **First ever reported 1.2V DDR4 SDRAM:**
- In Paper 2.1, Samsung discloses the first 1.2V DDR4 4Gb SDRAM with a 30nm CMOS technology. A high bandwidth of 3.2Gb/s/pin, which is 2× faster than those of existing DDR3 DRAMs, is realized by stable signal transfer using a dual-error detection scheme, a gain enhanced buffer, and a PVT-tolerant data-fetch scheme.

APPLICATIONS AND ECONOMIC IMPACT

- This design is going to be used for data center servers, networking and low-power handheld devices.
- All the DDR3 DRAMs currently being used are expected to be replaced by DDR4 DRAMs by 2013.

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Session 3 Overview : Processors

HIGH PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: Joshua Friedrich, IBM, Austin, TX
Session Co-Chair: Jinuk Luke Shin, Oracle, Santa Clara, CA

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

The continuous CMOS scaling predicted by Moore's law for density, frequency and power is threatened by the limits of traditional planar 2D transistors. This year's introduction of 3D transistors in an industry processor represents an innovative approach to overcome these trends. Engineering creativity continues to drive circuit techniques for energy-efficient computing, including low-voltage design and advanced clocking methodologies. Processors continue to integrate diverse components and improve micro-architectural performance to balance scaling of performance and power. This session shows a wide range of processors and techniques to address current and future challenges.

- In Paper 3.1, Intel unveils the industry's first 22nm 3D transistors in a next-generation processor containing four IA-32 cores, GPU, memory and PCIe controllers.
- In Paper 3.2, Cavium presents its third-generation 65nm MIPS64 processor, which integrates 32 cores with 4MB L2 cache, hardware accelerators and DDR3 memory controller while operating at 1.6GHz with a TDP of 40W to 65W.
- In Paper 3.3, Oracle shows its next-generation 40nm T4 processor. The T4 features eight 8-threaded, out-of-order SPARC cores, a 4MB L3 cache, a crossbar and SoC components on a 403mm2 die. The chip delivers up to 5× single-thread performance improvement within the same power envelope over its predecessor.
- In Paper 3.4, Intel introduces an x86-standard OS-compliant SoC with a dual-core 1.6GHz Atom® processor supporting a custom interconnect fabric, integrated voltage regulators, clock generator with SSC, PMU and a fully integrated RF WiFi transceiver. The chip is implemented in a 32nm high-k/metal-gate CMOS process.
- In Paper 3.5, Fudan University discloses a 16-core processor design featuring both message passing and shared-memory inter-core communication mechanisms implemented in 65nm CMOS occupying 9mm2, and operating at 800MHz, consuming 320mW at 1.2V.
- In Paper 3.6, Intel's 32nm IA-32 core demonstrates ultra-low voltage operation and a wide supply range of 280mV to 1.2V. The chip occupies 2mm2, and consumes 2mW at 0.28V operating at 3MHz, to 737mW at 1.2V operating at 915MHz, with a 4.7× improvement in energy efficiency.
- In Paper 3.7, AMD shows a resonant clock network with integrated inductors implemented in AMD's 32nm x86-64 processor resulting in a reduction of 24% in clock power and 5-to-10% in total chip power at frequencies above 3.0GHz.
- In Paper 3.8, Intel introduces a reconfigurable SoC clock-generation core to enable digital SSC and clock-skew correction based on an all-digital synthesizable PLL. The design is implemented in a 22nm LP CMOS process, consuming 3mW at 1V, operating at 3.2GHz, in the low-power mode.

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Session 3 Highlights : Processors

[3.1] A 22nm IA Multi-CPU and GPU System-on-Chip

[3.3] The Next-Generation 64b SPARC Core in a T4 SoC Processor

Paper 3.1 Authors: S. Damaraju, V. George, S. Jahagirdar, T. Khondker, R. Milstrey, S. Sarkar, S. Siers, I. Stolero, A. Subbiah
Paper 3.1 Affiliation: Intel, Folsom, CA
Paper 3.3 Authors: J.L. Shin, H. Park, H. Li, A. Smith, Y. Choi, H. Sathianathan, S. Dash, S. Turullols, S. Kim, R. Masleid, G. Konstadinidis, R. Golla, M. Doherty, G. Grohoski, C. McAllister
Paper 3.3 Affiliation: Oracle, Santa Clara, CA

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

CONTEXT AND STATE OF THE ART

- Last year's ISSCC processors featured 32nm planar (2D) transistors, while this year introduces the industry's first microprocessor with 3D transistors in a 22nm process.
- The general industry trend has featured low-thread-count processors at high frequency, or high thread counts at relatively low frequency. This year features a processor with eight 3.0GHz cores for 64 total threads to balance single-thread performance with throughput.

TECHNICAL HIGHLIGHTS

- **Intel introduces the first processor built in 22nm technology using 3D transistors:**
- In Paper 3.1, Intel unveils the industry's first 22nm 3D transistors in a next-generation processor containing four IA-32 cores, GPU, memory and PCIe controllers.
- **Oracle's next-generation SPARC SoC runs at 3GHz providing 7× performance improvement:**
- In Paper 3.3, Oracle's T4 processor features eight out-of-order SPARC cores for a total of 64 threads with 4MB L3 cache, and running at 3.0GHz.

APPLICATIONS AND ECONOMIC IMPACT

- These innovative processors represent a new level of performance, integration, and energy efficiency. By delivering significantly increasing performance and capability, these efficient engines will enable servers to handle the most challenging technical applications and manage needs for the world's growing cloud computing ecosystem.
- The introduction of the 22nm technology node provides increased performance and higher levels of integration by combining an ever-expanding list of features onto a single die. This enables a new generation of energy-efficient low-cost computing systems. In addition, 3D transistors bring unheralded opportunity for the continuation of Moore's law and pave the way for future CMOS scaling.

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Session 4 Overview : RF Techniques

RF SUBCOMMITTEE

Session Chair: Masoud Zargari, Qualcomm-Atheros, Irvine, CA
Session Co-Chair: Songcheol Hong, KAIST, Daejeon, Korea

Subcommittee Chair: Andreia Cathelin, *STMicroelectronics, Crolles, France*, RF Subcommittee

System-on-a-chip (SoC) integration of RF transceivers has become progressively popular in recent years as the SoCs provide increased functionality and lower power while driving down the overall system cost, all due in part to CMOS integration. The papers presented in this session focus on CMOS implementation of several key building blocks of RF transceivers.

- In Paper 4.1, UCLA presents a blocker-tolerant wideband noise-cancelling receiver in 40nm CMOS that uses two down-conversion paths with no voltage gain prior to baseband filtering. A prototype achieves sub-2 dB noise figure from 0.3 to 2.9GHz. In out-of band, IIP3 is measured at +12dBm, and P1dB blocker compression is close to 0 dBm.
- In Paper 4.2, the University of Twente describes 8-path notch filters in 65nm CMOS technology with a notch frequency tunable from 100MHz to 1.2GHz. The filter insertion loss in the passband is 1.4 to 2.8dB, while the rejection at the notch frequency is >20dB. P1dB>+2dBm and IIP3>+17dBm are demonstrated.
- In Paper 4.3, the University of Twente presents a wideband IM3 cancellation technique in 0.16µm CMOS for attenuators that provides 4 discrete attenuation levels with 6dB spacing for DC to 5GHz , S11<-14dB and attenuation flatness for the whole band.
- In Paper 4.4, the University of Twente introduces a 1-to-2.5GHz phased-array receiver front-end in 0.14µm CMOS based on DC-coupled gm-C delay cells designed to minimize parasitic poles. Die area is much reduced w.r.t. to integrated delay lines, while >0.5GHz instantaneous bandwidth is achieved at 10dB noise figure per channel. Delays up to 550ps with 13.75ps resolution are realized.
- In Paper 4.5, KAIST presents a dual-mode 0.18µm CMOS power amplifier for WCDMA that includes all matching networks and linearization bias circuits. In high- (low-) power mode, the PA delivers an output power of 28.0 (16.4)dBm with a PAE of 36.4 (27.4)% with ACLR at a 5MHz offset of -35dBc at 1.95GHz. In low power-mode, the quiescent current is 20mA.
- In Paper 4.6, Toshiba introduces a PA with linearization loop implemented in 0.13µm CMOS. It employs a 2-path feedback scheme where the phase and amplitude are compared separately. The wideband characteristics of the loop improve the WCDMA linear output power by up to 2.3dB. It delivers linear output power of +27.1dBm with a PAE of 28%.
- In Paper 4.7, Fujitsu presents a fully integrated triple-band (800MHz, 1.7GHz, and 2.0GHz) 90nm CMOS power amplifier for WCDMA mobile handsets. The power amplifier with on-chip power and temperature sensors and a digital interface is implemented in a 3.5 x 4 x 0.7mm3 flip-chip package. The PA achieved 27dB gain, 30% PAE and 27.5dBm output power at -34dBc ACPR.
- In Paper 4.8, the University of Toronto describes a mm-Wave Class-D 45nm SOI CMOS PA featuring a stacked-cascode-inverter output stage that enables high-voltage operation without any output matching. The saturated output power is 22.5dBm up to 20GHz, 19.5dBm at 40GHz and 14dBm at 50GHz. The peak PAE is 24% at 15GHz.

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Session 4 Highlights : RF Techniques

[4.7] A Fully Integrated Triple-Band CMOS Power Amplifier for WCDMA Mobile Handsets

[4.6] A 28.3mW PA-Closed Loop for Linearity and Efficiency Improvement Integrated in a +27.1dBm WCDMA CMOS Power Amplifier

Paper 4.7 Authors: K. Kanda, H. Nakamoto, Y. Kawano, T. Sasaki, N. Shirai, T. Tamura, S. Kawai, M. Kudo, T. Murakami, N. Hasegawa, H. Kano, N. Shimazui, A. Mineyama, K. Oishi, M. Shima, N. Tamura, T. Suzuki, T. Mori, K. Niratsuka and S. Yamaura.
Paper 4.7 Affiliation: Fujitsu Laboratories, Kawasaki, Japan

Paper 4.6 Authors: S. Kousai, J. Deguchi, K. Onizuka, T. Yamaguchi, Y. Kuriyama, and M. Nagaoka.
Paper 4.6 Affiliation: Toshiba, Kawasaki, Japan.

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF Subcommittee

CONTEXT AND STATE OF THE ART

- The Power Amplifier (PA) is one of the most power-hungry devices in a cellular phone. Among other factors, one reason 3G smart phones have shorter battery life compared to 2/2.5G phones is that the PA is less power efficient due to the more complex modulation for higher data rate. Although CMOS PAs have been reported for 2/2.5G, until today, few WCDMA CMOS PAs with competitive performance have been reported.

TECHNICAL HIGHLIGHTS

- **World's first tri-band WCDMA CMOS PA with lowest current ever reported**
- Paper 4.7 by Fujitsu demonstrates the world's first tri-band WCDMA CMOS PA. The 90nm PA occupies 1.2mm×3mm die area and is flip-chip packaged in a small form factor of 3.5×4×0.7mm^3. The PA consumes less than 20mA for DG09, the lowest current ever reported, and delivers output power of +27.3dBm with 28.5% PAE.
- **World's first reported RF feedback loop for power efficiency and linearity enhancement**
- Paper 4.6 by Toshiba presents a 0.13um CMOS WCDMA PA with linearization loop employing AM-AM and AM-PM feedback. The PA delivers linear output power of +27.1dBm with 28% PAE and occupies 2.2mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- CMOS PAs for non-constant envelope modulation have the potential to significantly reduce the cost of handsets and pave the path for higher levels of integration.
- The PA is one of the highest power-consuming components in mobile phones. Improving PA power efficiency can considerably increase battery life.

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Session 5 Overview : Audio and Power Converters

ANALOG SUBCOMMITTEE

Session Chair: Wing-Hung Ki, HKUST, Hong Kong
Session Co-Chair: Jed Hurwitz, Consultant, UK

Subcommittee Chair: Bill Redman-White, University of Southampton, UK, Analog Subcommittee

Effective conversion of power from one type to another is one of the fundamental analog tasks needed by the electronic world. It is an area that requires numerous solutions to match the diverse applications in order to maintain efficiency and meet the requirements of the load or source and the application. This session begins with three high-fidelity and high-efficiency audio circuits targeting at energy-conscious mobile entertainment and communication platforms, followed by a paper on capacitive DC-DC power conversion and finishes with a series of four papers that relate to different energy harvesting methods. Each paper has a specific power-conversion challenge, and the solution is optimized for each application.

- Paper 5.1 by ST-Ericsson presents a 2.5W 1% THD Class-D amplifier with a dynamic range of 104 dB(A) occupying 2.12mm^2 in 0.13μm CMOS, including current sensing for speaker protection and a new EMI-reduction scheme without affecting in-band noise.
- Paper 5.2 by ICsense combines a 1.5W Class-D amplifier with a boost converter generating 10V power supply using only low-voltage devices in a 1.8V/3.3V 0.18μm standard CMOS technology. The chip passes the 2kV HBM and 200V MM tests.
- Paper 5.3 by Dongbu Hitek presents a 0.028% THD+N 3-level Class-D amplifier with a differential front-end and a new feedback scheme to mitigate the common-mode variation due to asymmetrical outputs. It achieves a power efficiency of 91% with a very low quiescent current consumption of 2mA while occupying 1.14mm^2 in a 5V CMOS process.
- Paper 5.4 by NXP Semiconductors presents a 41-phase fully on-chip switched-capacitor power converter implementing 1/2 and 2/3 conversion ratios to maximize efficiency up to 81% with low (3.8mV) output ripple, and achieving a power density of 38.6mW/mm^2 over an area of 0.25mm^2 in 90nm CMOS.
- Paper 5.5 by Solar Semiconductor presents an embedded system for distributed photovoltaic (PV) energy optimization that leverages a resonant switched-capacitor converter to balance power flow across PV cells at the sub-module level with an efficiency of over 99%. It occupies 5.52mm^2 in a 0.35μm CMOS technology that incorporates high voltage devices.
- Paper 5.6 by Vienna University of Technology presents an analog maximum power point tracker of a 9 solar cell module that generates the PWM signals for a boost converter in 0.44mm^2 of a 0.35μm high-voltage CMOS process. The tracking efficiency is better than 99% for a photo-current of 0.5-to-8A.
- Paper 5.7 by KAIST presents a self-starting boost converter architecture with low-power MPPT control for low-voltage TEG application occupying 0.09mm^2 in 0.13μm CMOS. The transformer is kick-started by noise amplification from as little as 40mV. The transformer is then reused as an inductor during the normal boost converter mode.
- Paper 5.8 by Texas Instruments presents a battery charger and management IC that consumes only 330nA at 3V for use with solar and thermoelectric sources. The hysteretic mode charger is implemented with a programmable MPP loop, and achieves an efficiency of >90% and extracts energy from sources as low as 100mV and 5μW.

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[5.5] A High-Voltage CMOS IC and Embedded System for Distributed Photovoltaic Energy Optimization With over 99% Effective Conversion Efficiency and Insertion Loss Below 0.1%

Paper Authors: J.T. Stauth[1,2], M.D. Seeman[2], and K. Kesarwani[2]
Paper Affiliation: [1]Dartmouth College, Hanover, NH; [2]Solar Semiconductor, Inc., Sunnyvale, CA

Subcommittee Chair: Bill Redman-White, NXP/Southhampton University, UK, Analog Subcommittee

CONTEXT AND STATE OF THE ART

- Solar energy is an important renewable energy source, and the long-term economics of solar panel deployments mean that the payback of even a 1% relative improvement in efficiency can be high.
- Power conversion when the different PV cells of a solar panel may be under differing conditions, such as occurs when there is shading from the environment, is a real-world problem that affects the viability of solar energy as a renewable energy source. Current solutions to this problem are complex.

TECHNICAL HIGHLIGHTS

- **Highest efficiency power-conversion system for grid-connected photovoltaic (PV) cells**
- Solar Semiconductor presents a power-management system for distributed photovoltaic (PV) energy optimization that handles different photocell conditions, achieving power conversion efficiency above 99% and insertion loss below 0.1% by incorporating a distributed resonant-switched-capacitor (ReSC) converter.

APPLICATIONS AND ECONOMIC IMPACT

- This innovation will make balanced power flow at the sub-module level possible, enabling higher integration and finer granularity of PV cells, so that solar energy becomes cheaper and therefore more widely adopted.

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Session 6 Overview : Medical, Displays and Imagers

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Co-Chair: Yusuke Oike, Sony, Kanagawa, Japan
Session Co-Chair: Maysam Ghovanloo, Georgia Institute of Technology, Atlanta, GA

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee

This session presents recent achievements in the area of imaging, display, biosensing, and medical systems. Two low-voltage image sensors and a direct photon-counting X-ray image sensor are highlighted, as well as a capacitive touch controller integrated together with an LCD driver on one chip for ultra-thin touch-screen displays. Moreover, an approach is presented to improve the robustness of biopotential recording systems against motion artifacts for portable/wearable medical devices. Three further papers on biosensors based on different detection principles, capacitive sensing, single-photon detection, and magnetic relaxation, respectively, push the limits on sensitivity, dynamic range, and throughput. A wireless intraoral assistive technology demonstrates a way to enable individuals with high-level disabilities to control their environments using their free tongue motion.

- In Paper 6.1, KAIST presents an X-ray image sensor supporting 3-level energy detection for color X-ray imaging in 0.13µm CMOS. 30% smaller pixel pitch per energy-bin and 10× better uniformity without calibration are achieved compared to state-of-the-art technologies. The 8.8×8.8mm^2 ASIC has a static 4.6µW/pixel power consumption from 3.3V/1.2V supplies.
- In Paper 6.2, the University of Michigan describes a 5×5mm^2 adaptively reconfigurable image sensor in 0.18µm CMOS using a 2.5T pixel structure that operates at 1.36µW on a supply voltage of 0.8V from harvested energy. In addition, the imager is reconfigurable to operate in high-sensitivity or wide-dynamic-range modes.
- In paper 6.3, National Tsing Hua University presents a 1.4×1.4mm^2 PWM image sensor in 0.18µm CMOS with threshold-variation cancelling and a programmable threshold control scheme. A 0.055% pixel FPN and 83dB dynamic range under 0.5V supply voltage operation are achieved.
- In Paper 6.4, Samsung Electronics describes a capacitive touch controller together with an LCD driver integrated in a 24×1.52mm^2 chip in a 90nm triple-well LDI process, achieving 35dB SNR without software filtering in an LCD on-cell touch screen by using a differential sensing scheme.
- In Paper 6.5, imec discusses a 3-channel 160µA biopotential acquisition ASIC in 0.18µm CMOS with 200mHz HPF. The chip is capable of rail-to-rail DC offset rejection for suppressing motion artifacts, while achieving 120dB CMRR, 1GΩ input impedance, and 1.3µV_{rms} input-referred noise at 100Hz bandwidth. The 8×5mm^2 ASIC consumes 192µW from a 1.2V supply.
- In Paper 6.6, KAIST describes an integrated capacitance-based biosensor with 57.8dB sensitivity and 94.6% detection dynamic range realized in 0.35µm CMOS for label-free detection of oligonucleotides. The 4×5mm^2 ASIC consumes 2.34mW from a 3.3V supply.
- In Paper 6.7, the University of Edinburgh presents a 1.7×1.3mm^2 time-resolved single-photon sensor SoC in 0.13µm CMOS with 100Mphoton/s throughput, 22.5µm pitch, 10% fill factor, and 52ps time-resolution for on-chip fluorescence lifetime estimation.
- In Paper 6.8, Georgia Institute of Technology highlights a 12-channel dual-band wireless magnetoresistive sensing system in 0.5µm CMOS for an intraoral tongue-computer interface, which can measure the 3D magnetic field within the oral space and convert it to a set of user-defined commands for environmental control. The 3.8×3.7mm^2 ASIC consumes 700µW from a 1.8V supply, in addition to the 2.6mW consumed by the accompanying MSP430 microcontroller, for a total system power of 3.3mW.
- Finally, in Paper 6.9 the University of California at Berkeley presents a 10kpixel baseline-free magnetic-bead detector implemented in 0.35µm CMOS with column-parallel readout for miniaturized immunoassays, which

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reduces the array scan time to 8s and achieves 9nT Allan Deviation, enabling detection of sub-1μm particles. The $5.1\times3.5mm^2$ ASIC consumes 330mW.

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Session 6 Highlights : Medical, Displays and Imagers

[6.5] A 160µA Biopotential Acquisition ASIC With Fully Integrated IA and Motion-Artifact Suppression

Paper Authors: Nick Van Helleputte, Sunyoung Kim, Hyejung Kim, Jong Pal Kim, Chris Van Hoof, Refet Yazicioglu
Paper Affiliation: imec, Heverlee, Belgium, and Samsung Advanced Institute of Technology, Korea

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee

CONTEXT AND STATE OF THE ART

- Wearable/portable medical devices that record biopotentials from the surface of the skin have been prone to motion artifacts. These artifacts cause large DC offsets, which result in saturation of the front-end amplifiers, if they are not properly suppressed.
- Previous techniques lead to degradation in the front-end performance. A new front-end design can suppress those artifacts before amplification by rejecting large DC-offsets without degrading key amplifier characteristics such as CMRR, input impedance, and noise.

TECHNICAL HIGHLIGHTS

- **First analog motion artifact suppression technique that does not degrade the performance of an analog front-end:**
- A 3-channel 160µA biopotential acquisition ASIC is presented with 200mHz highpass filter capable of rail-to-rail DC offset rejection to suppress motion artifacts, while achieving 120dB CMRR, 1GΩ input impedance, and 1.3µV_{rms} input-referred noise in 100Hz.

APPLICATIONS AND ECONOMIC IMPACT

- There has been a growing interest in wearable/portable biopotential-monitoring systems, which have very strict requirements in terms of power dissipation, high signal quality, small area (minimal use of off-chip components) and robust operation during ambulatory use.
- The latter is especially evident as a problem, since in real-life ambulatory conditions, motion artifacts will disturb and potentially saturate the readout channel. In addition, requirements for multimodal information acquisition demand even more functionality with minimal power dissipation.
- The biopotential acquisition ASIC improves the quality of recording in portable biopotential monitoring systems, particularly in electrocardiography (ECG).

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Session 7 Overview : Multi-Gb/s Receiver and Parallel I/O Techniques

WIRELINE SUBCOMMITTEE

Session Chair: Robert Payne, Texas Instruments, Dallas, TX
Session Co-Chair: Tatsuya Saito, Hitachi, Kawasaki, Japan

Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY

Multi-Gb/s data transmission is needed to communicate over cabling between systems, on traces on a printed circuit board, and even between multiple die contained within a single package. No single technology can optimally address the constraints imposed by various standards and systems requirements. High-speed backplanes require complex equalization; optical communication requires conversion and interface between the electrical and optical domains and memories require compact parallel I/Os that tackle crosstalk and skew. This session proposes techniques that enable these interconnects.

- In Paper 7.1, Caltech describes an optical receiver implemented in a 65nm CMOS technology. By using an RC double-sampling front-end and dynamic offset modulation, the receiver achieves up to 18.6Gb/s data rate and better than -7.3dBm optical sensitivity. In an electrical-only test at 20Gb/s, it consumes 7.2mW from a 1.2V supply with an area less than 0.0028mm^2.
- In Paper 7.2, Rambus describes a near-ground 40nm CMOS receiver that uses a common-gate input stage whose transconductance provides a portion of the transmission-line termination. A replica-biasing scheme adjusts the transconductance and reduces sensitivity to process, supply, and temperature variations. The receiver, which occupies 0.01mm^2, equalizes a 3" FR4 PCB memory link with 15dB of loss at Nyquist frequency to achieve 16Gb/s with 0.4mW/Gb/s power efficiency, operating with a 1V supply.
- In Paper 7.3, IBM describes a 19Gb/s 45nm SOI CMOS serial-link receiver that implements an equalizer using four time-interleaved T/Hs, each followed by a one-tap speculative DFE and a current integrator-based 4-tap FFE combined with a 4-tap DFE. The FFE tap weights are controlled by varying the integration time for each tap. At 19Gb/s, the 0.07 mm^2 receiver consumes 118mW from a 1.1V supply and equalizes a 25dB loss PCB trace to 36% eye opening.
- In Paper 7.4, POSTECH and Samsung present a parallel transceiver for a QDR bidirectional memory interface implemented in 90nm CMOS. Individual data-edge-tracking CDRs used in both the TX and RX reduce the impact of duty-cycle distortion and timing skews. The transceiver, which occupies 0.225mm^2 per lane, achieves 8Gb/s per channel with a 10^{-12} BER at a power efficiency of 4.02mW/Gb/s from a 1.25V supply.
- In Paper 7.5, Rambus introduces a parallel-link coding scheme with no data-rate overhead that uses balanced signaling across multiple lanes to eliminate first-tap post-cursor ISI without a DFE. A 4.1pJ/b 16Gb/s prototype implemented in a 40nm CMOS process achieves error-free transmission over FR4 traces with 15dB of loss at Nyquist.
- In Paper 7.6, POSTECH describes a far-end crosstalk (FEXT) cancellation scheme is added to a single-ended parallel receiver that is implemented in 0.13 m CMOS. Capacitive signal injection from the aggressor lanes is adaptively tuned to minimize the crosstalk-induced jitter. The receiver achieves 5Gb/s at a BER $<10^{-12}$ and reduces FEXT-induced jitter by up to 75% while consuming 4.3mW/Gb/s.
- In Paper 7.7, IBM introduces a compact low-power 3D I/O for through-silicon via (TSV) applications that incorporates a low-swing TX and gated-diode sense-amplifier-based RX. The I/O, operating with a 1V supply, achieves power efficiencies of 0.13mW/Gb/s at 2Gb/s with 190mV swing and 0.11mW/Gb/s at 6Gb/s with 300mV swing. To demonstrate the possibility of communication through multiple stacked dies, the I/O drives a 6-TSV chain at 5.2Gb/s with 0.50mW/Gb/s.

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Session 7 Highlights : Multi-Gb/s Receiver and Parallel I/O Techniques

[7.7] A Compact Low-Power 3D I/O in 45nm CMOS

Paper 7.7 Authors: Y. Liu, W. Luk, and D. Friedman
Paper 7.7 Affiliation: IBM Research, Yorktown Heights, USA

Subcommittee Chair: Daniel Friedman, IBM Research, Yorktown Heights, NY, Wireline

CONTEXT AND STATE OF THE ART

- The increased requirement for very high integration of multiple chips into a single package has led to three-dimensional (3D) silicon integration technology, featuring thinned die-to-die bonding and through-silicon-via (TSV) interconnections.
- This enables dense local chip-to-chip interconnect with potentially thousands of multi-gigabit-per-second I/Os supporting tens of terabits-per-second data bandwidth. However, this ultra-high bandwidth will only be achieved if area and power efficiency challenges can be addressed, which will greatly enhance the flexibility and applicability of these technologies.

TECHNICAL HIGHLIGHTS

- **3D I/O drives 6-TSV chains at 5.2Gb/s with 0.50mW/Gb/s**
- In Paper 7.7, IBM introduces a compact low-power 3D I/O for through-silicon via (TSV) applications that incorporates a low-swing TX and gated-diode sense amplifier-based RX. The I/O, operating with a 1V supply, achieves power efficiencies of 0.13mW/Gb/s at 2Gb/s with 190mV swing and 0.11mW/Gb/s at 6Gb/s with 300mV swing. To demonstrate the possibility of communication through multiple stacked dies, the I/O drives a 6-TSV chain at 5.2Gb/s with 0.50mW/Gb/s.

APPLICATIONS AND ECONOMIC IMPACT

- Multi-stacked chips using TSVs are becoming critical for the long-term development of high performance mixed signal systems-on-chip and application processors.
- The successful implementation of TSVs with more than two or three stacked die will allow the continued expansion of the scaling expected from silicon technology without having to rely on continued scaling of the transistor process technology, which will be critical to the extension of CMOS beyond the scaling limits.

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Session 8 Overview : Delta Sigma Converters

DATA CONVERTERS SUBCOMMITTEE

Session Chair: Brian Brandt, Maxim Integrated Products, North Chelmsford, MA
Session Co-Chair: Gerhard Mitteregger, Intel Mobile Communication, Villach, Austria

Subcommittee Chair: Venu Gopinathan, Texas Instruments, Bangalore, India

Important trends in delta-sigma converter design are the increasing resolution, bandwidths, and sampling frequencies, as well as the increased popularity of direct-RF digitization via bandpass conversion. The papers in this session highlight these advances. Specifically, the issues concerning power efficiency, linearity and stability at very high sampling rates are addressed by employing different advanced techniques like calibration, feedback FIR filtering, and delay compensation. The lowpass delta-sigma converters demonstrate bandwidths from 10 to 150MHz, while the bandpass converters achieve bandwidths from 20 to 150MHz at intermediate frequencies in the range from 200MHz to 1GHz. The delta-sigma converters sample at rates as high as 6GHz.

- In Paper 8.1, Broadcom describes a 6th-order LC bandpass ΔΣ ADC with 3.2GHz sampling clock, 20mW power consumption in a 40nm CMOS process that achieves 70dB SNDR over a 20MHz bandwidth tunable from 700-to-800MHz center frequency. A capacitively coupled CMOS RTZ voltage-mode DAC is used to reduce the thermal noise in the main feedback DAC.
- In Paper 8.2, the University of Michigan presents an 800MS/s low-power continuous-time bandpass ΔΣ modulator with 24MHz bandwidth at 200MHz IF. A power-efficient resonator with a single amplifier is used to implement the 4th-order loop filter. This 65nm CMOS modulator shows 58dB SNDR, 60dB DR and 65dB IMD, and 12mW power.
- In Paper 8.3, Analog Devices reports a DC-to-1GHz tunable continuous-time lowpass/bandpass ΔΣ ADC in 65nm CMOS. It achieves 150MHz bandwidth at 450MHz with 74dB DR and 550mW. The modulator employs a reconfigurable LC and active-RC filter and 7th-order feedforward opamps.
- In Paper 8.4, Oregon State University presents a VCO-based ΔΣ modulator that overcomes the VCO nonlinearity by minimizing the input signal of the VCO. The 90nm CMOS converter achieves 78dB SNDR and 10MHz bandwidth using 16mW.
- In Paper 8.5, Ulm University describes a multi-bit, 3rd-order CT ΔΣ modulator with 25MHz BW and 500MHz sampling frequency. The feedback DAC linearization uses an auxiliary DAC and a cross-correlation-based DNL estimation. The 90nm CMOS modulator achieves 69dB SNR, 67.5dB SNDR, 72dB DR, and 79dB SFDR over a 25MHz bandwidth, while consuming an overall power of 8.5mW, for an FOM of 88fJ/conv.
- In Paper 8.6, IIT Madras shows a 36MHz bandwidth CT ΔΣ ADC with 70.9dB SNDR at a power consumption of 15mW in 90nm CMOS. The 3.6GHz, 1b modulator employs an 8-tap FIR filter in the main feedback DAC, and uses an extra compensation feedback path to overcome the delay associated with the FIR DAC.
- In Paper 8.7, Texas Instruments presents a 45nm CMOS CT ΔΣ converter that samples at 6GHz and achieves 61dB SNDR in 60MHz bandwidth using 20mW. An excess loop delay compensation scheme ensures modulator stability with 1 clock period comparator delay.

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Session 8 Highlights : Delta Sigma Converters

[8.3] A DC-to-1GHz Tunable RF ΔΣ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW

[8.6] A 15mW 3.6GS/s CT-ΔΣ ADC With 36MHz Bandwidth and 83dB DR in 90nm CMOS

Paper 8.3 Authors: H. Shibata[1], R. Schreier[1], W.Yang[2], A. Shaikh[2], D. Paterson[2], T. Caldwell[1], D. Alldred[1], P. Lai[2]
Paper 8.3 Affiliation: [1]Analog Devices, Toronto, Canada, [2]Analog Devices, Wilmington, MA

Paper 8.6 Authors: P.Shettigar, S. Pavan
Paper 8.6 Affiliation: Indian Institute of Technology Madras, Chennai, India

Subcommittee Chair: Venu Gopinathan, Texas Instruments, Bangalore, India

CONTEXT AND STATE OF THE ART

- Paper 8.3 demonstrated a step towards the ultimate ADC capable of directly converting an input RF signal into digital form.
- Analog design techniques enable the realization of power-efficient single-bit continuous-time delta-sigma ADCs at multi-Gb/s speeds.

TECHNICAL HIGHLIGHTS

- **Very high sampling rate RF ΔΣ data converters:**
- Paper 8.3 presents a bandpass ΔΣ ADC that supports a tunable center frequency between DC and 1GHz with a bandwidth between 35 and 150MHz, while supporting a dynamic range of 74dB and an SNR of 69dB. Paper 8.6 presents a 3.6GS/s 1b modulator that shows 36MHz bandwidth with 70.9dB SNDR while consuming only 15mW in 90nm CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- Direct RF-sampling with flexible center frequency handles multiple RF-receiver standards and adapts to the RF environment to reduce cost and power dissipation.
- This modulator enables the direct digitization of the newest generation of wide-bandwidth communication channels with high accuracy and at the low power levels required for mobile devices.

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Session 9 Overview: Wireless Transceiver Techniques

WIRELESS SUBCOMMITTEE

Session Chair: Sven Mattisson, Ericsson, Lund, Sweden
Session Co-Chair: Shouhei Kousai, Toshiba, Kawasaki, Japan

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless Subcommittee

In a world with an ever-increasing number of wireless links, often with multiple radios in the same device, mutual interference is becoming a major problem. This aggravates co-existence issues, such as out-of-band emission and receiver blocking. This session covers several techniques that address these topics. Three papers cover linear transmitters for high data-rate applications, including LTE, 802.11n and upcoming 60GHz communication. On the receiver side, papers feature active feedback and beamforming techniques to improve blocker rejection. System techniques that maintain or improve wireless throughput in a 4-in-1 combo SoC will be presented.

- In Paper 9.1, Marvell describes a SAW-less multistandard TV tuner, with a single input, that covers 40MHz to 1GHz, while achieving a 3dB noise figure. This device consumes less than 450mW and occupies an area of 2×2.8 mm^2 in 80nm CMOS.
- In Paper 9.2, Fujitsu describes a multiband multimode transmitter, implemented in 90nm CMOS that achieves a -63dBc Counter-Intermodulation Rejection (CIMR) ratio for single-Resource Block (RB) allocation at the band-edge of a 20MHz LTE signal.
- In Paper 9.3, the University of Twente presents a very compact active-feedback receiver, demonstrating up to 48dB stop-band rejection and +12dBm out-of-band IIP3 in <0.06mm^2 of 65nm CMOS.
- In Paper 9.4, Intel describes an out-phasing transmitter for WLAN applications that delivers +20dBm output power at 2.4GHz, while reaching 22% power-added efficiency at -25dB error-vector magnitude with an all-digital phase modulator in 32nm CMOS.
- In Paper 9.5, KU Leuven presents a 60GHz out-phasing transmitter that features a power amplifier with a power-added efficiency of 25% at 15.6dBm saturated output power. This TX occupies 0.33mm^2 in 40nm CMOS.
- In Paper 9.6, MediaTek describes a 4-in-1 WiFi-Bluetooth-FM-GPS 65nm combo SoC designed for co-existence in the 2.4GHz ISM-band that achieves 90% WiFi throughput during simultaneous Bluetooth operation.
- In Paper 9.7, the University of Twente presents an all-passive switched-capacitor beamforming receiver front-end, designed for interference rejection in the 1.5-to-5.0GHz range, that delivers +2dBm input-referred compression point and 72dB spurious-free dynamic range. This RX consumes an area of 0.18mm^2 in 5nm CMOS.

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Session 9 Highlights : Wireless Transceiver Techniques

[9.3] Active Feedback Receiver with Integrated Tunable RF Channel Selective, Distortion Cancelling, 48dB Stop-Band Rejection and > +12dBm Wideband IIP3, Occupying < 0.06mm2 in 65nm CMOS

Paper 9.3 Authors: S.Youssef, R.Van Der Zee, B.Nauta
Paper 9.3 Affiliation: University of Twente, Twente

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless Subcommittee

CONTEXT AND STATE OF THE ART

- Classical receivers perform channel selection at IF or base band.
- The chip area of such an approach, even in CMOS, is large, and does not offer RF flexibility.

TECHNICAL HIGHLIGHTS

- **Dramatic application of tunable RF channel-selection for software radio**
- This receiver performs channel selection at RF, addressing both linearity (+12dBm IIP3) and flexibility (1-to-2.5GHz tunable center frequency) using active feedback.
- Realized in 65nm CMOS, the 0.06mm² receiver allows a drastic reduction in chip area, and easy scalability in process technology.

APPLICATIONS AND ECONOMIC IMPACT

- The receiver will enable lower power, lower complexity Software-Defined Radio (SDR) addressing standards in the 1-to-2.5GHz range.
- The flexibility of such an approach should allow simplified multimode, multiband receivers.
- This proposed receiver will drastically reduce the RF functionality cost in scaled CMOS processes.

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[9.5] A 60GHz Outphasing Transmitter in 40nm CMOS with 15.6dBm Output Power

Paper 9.5 Authors: D.Zhao, P.Reynaert
Paper 9.5 Affiliation: Katholieke Universiteit Leuven, Leuven

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless

CONTEXT AND STATE OF THE ART

- Until now, the trend has been to build Cartesian transmitters in the 60GHz application space using Class A-AB amplifiers.
- These applications were first served by III-V amplifiers. Then in the past five years SiGe solutions were developed, and most recently CMOS is coming into the picture.

TECHNICAL HIGHLIGHTS

- **The first Application of an outphasing power amplifier at 60GHz**
- A CMOS outphasing transmitter based on IQ modulation is realized in 40nm CMOS.
- The transmitter achieves 25% PAE at a linear output power of 15.6dBm.

APPLICATIONS AND ECONOMIC IMPACT

- The 60GHz transmitter supports WiGig and IEEE 802.11ad systems for high-data-rate wireless uncompressed video streaming.
- High PAE allows a significant reduction in the power consumption, which enables the trend toward portable 60GHz terminals.

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Session 10 Overview : High-Performance Digital

HIGH PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: Lew Chua-Eoan, Qualcomm, San Diego, CA
Session Co-Chair: Se-Hyun Yang, Samsung Electronics, Kiheung, Korea

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee

The session covers a wide spectrum of high-performance digital systems, from single functional blocks to massively parallel supercomputers. In this regard, 3D Integration, SIMD and FPU blocks, links and other circuit-level issues will be examined in the latest 22nm/32nm processes. Performance and power-efficient computing techniques (e.g. near/subthreshold and micro-architectural optimizations) are addressed in the context of the latest computing applications.

- In Paper 10.1, Intel describes a 0.048mm^2 280mV-to-1.1V 256b reconfigurable SIMD vector permutation engine with 2D shuffle in 22nm CMOS. Wide dynamic supply scalability across 280mV (subthreshold) to 1.1V increases the permutation engine's energy-efficiency by 9×.
- In Paper 10.2, Technische Universität Dresden presents a serial on-chip link over 6mm with 43µm bus width in 65nm LP with an energy efficiency of 174fJ/mm at the highest speed of 90Gb/s (10Gb/s/line) and 1.25V V_{DD}. The circuit includes a SerDes transceiver with source-synchronous instantaneously stoppable clocking architecture and data synchronization for globally asynchronous locally synchronous (GALS) systems.
- In Paper 10.3, Intel describes a 0.045mm^2 IEEE single-precision floating-point-fused multiply-add unit fabricated in 32nm CMOS that achieves 54GFLOPS/W at 1.45GHz, 1.05V, 25ºC. The device provides up to 4× higher throughput and 3.1× higher energy efficiency at 162GFLOPS/W with single-precision accuracy. Robust near-threshold circuits operating from 300mV to 1.2V enable a peak energy efficiency of 1.2TFLOPS/W.
- In Paper 10.4, Intel fabricates a 0.064mm^2 single-cycle-throughput lighting accelerator for 3D graphics in a 32nm CMOS process. The design enables 560mV-to-1.2V operation with 2.05 Gvertices/s throughput and 0.56% mean error measured at 1.05V, 25ºC, and a 47% reduction in critical-path logic stages.
- In Paper 10.5, IBM fabricates eDRAM-based L3 cache memory chips in 45nm logic technology stacked on a processor proxy chip and interconnected with 50µm pitch TSVs. The design utilizes a modular cascading multiplexor circuit for inter-layer communication and a stack-wide shorted clock tree for high-frequency synchronous signaling to achieve inter-layer memory accesses up to 2.7GHz.
- In Paper 10.6, Georgia Tech presents 3D-MAPS, a 3D die-stack many-core processor integrating a logic die with 64 277MHz general-purpose processor cores and a memory die with 256KB SRAM. This processor at 0.13µm contains 33M transistors, 50K TSVs, and 50K face-to-face pads in a 20mm^2 footprint and runs at 1.5V consuming up to 6.3W.
- In Paper 10.7, the University of Michigan presents Centip3De – a chip that integrates 64 Cortex-M3 cores in a 3D stacked process and achieves 3930DMIPS/W in 0.13µm LP technology. It exploits near-threshold computing to create configurable compute clusters with 1-to-4 cores operating at 670mV and occupying 63mm^2.
- In Paper 10.8, Fujitsu describes the K computer system, which integrates over 548k cores using SPARC64 VIIIfx and the Tofu interconnect. It is currently ranked number one in the TOP500 list of supercomputers with a speed of 8.162PFLOPS, 93% efficiency and 9.89MW power consumption.

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Session 10 Highlights : High-Performance Digital

[10.8] K Computer: An 8.162 PetaFLOPS Massively Parallel Scalar Supercomputer Built With Over 548k Cores

Paper 10.8 Authors: H. Miyazaki, Y. Kusano, H. Okano, T. Nakada, K. Seki, T. Shimizu, N. Shinjo, F. Shoji, A. Uno, M. Kurokawa
Paper 10.8 Affiliation: Fujitsu Limited, Kawasaki, Japan

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

CONTEXT AND STATE OF THE ART

- Massively parallel supercomputers exhibit the highest level of integration achievable by current silicon base platforms. The K computer ranks first in the latest TOP500 list of supercomputers, and integrates over 548,000 cores.

TECHNICAL HIGHLIGHTS

- **8.162 PETAFLOPS —the highest floating point performance ever achieved**
- Paper 10.8 describes the highest-ever level of digital system integration with over 80,000 compute nodes, each of which consists of an 8-core SPARC64 VIIIfx.
- High-bandwidth 6D mesh/torus Tofu interconnect.
- Significant power saving of over 1MW corresponding to an electricity cost of over approximately $1 million per year.

APPLICATIONS AND ECONOMIC IMPACT

- This design enables an unprecedented number of simulations and opens up new avenues for scientific research in applications including, but not limited to, weather forecasting, protein dynamics, and biological research.
- This design significantly expands the current bounds of system integration and performance.

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Session 11 Overview : Sensors and MEMS

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Co-Chair: Christoph Hagleitner, IBM, Zurich, Switzerland
Session Co-Chair: Maurits Ortmanns, University of Ulm, Ulm, Germany

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany

This session presents recent advances in sensor interfaces for MEMS as well as temperature sensors. The papers span industrial and academic contributions. They exceed industry standard specifications and reveal innovative solutions. The first 4 papers describe capacitive sensor interfaces that bias MEMS microphones, compensate package-related offset, advance precision-displacement sensing, and address sustainability in harsh environments. The last 4 papers describe temperature sensors, which are becoming ubiquitous parts of integrated systems. The papers set new records in temperature range, accuracy, power efficiency, and level of integration by introducing new architectures, advances in technology, and circuit-level innovation.

- In Paper 11.1, Stanford University presents a method to measure and null the offset due to the asymmetry and drift of the parasitic capacitances of the bond wires connecting a MEMS accelerometer and its CMOS interface circuit. The technique reduces bond wire offset by 41dB, to 6.24mg.
- In Paper 11.2, Delft University of Technology describes a capacitance-to-digital converter with 17b resolution for precision displacement-sensing applications. The converter digitizes a 10pF off-chip capacitance with a resolution of $74aF_{rms}$ in a conversion time of 20μs.
- In Paper 11.3, NXP proposes a digitally assisted biasing scheme for a MEMS microphone. It compensates for bidirectional leakage currents of up to 1pA. The achieved noise level is less than -90dBFS, while its 6ms settling time is quite low and facilitates industrial testability.
- In Paper 11.4, Bosch proposes a wireless pressure sensor for harsh automotive environments. The system uses resonant coupling between a sealed capacitive pressure sensor and a readout ASIC to protect the latter from potentially corrosive gases. The system achieves ±2% error between -40 and 150°C using Q-based temperature compensation and a 1kS/s readout rate.
- In Paper 11.5, Delft University of Technology presents a temperature sensor based on the well-defined rate of heat diffusion in silicon. It achieves ±0.4°C inaccuracy over an extremely wide temperature range of -70 to +200°C. The sensor is fully self-contained and does not require an accurate external time reference.
- In Paper 11.6, SiTime describes the first use of a thermistor-based temperature sensor to stabilize a MEMS frequency reference. The resulting system achieves a frequency stability of <0.5ppm over the industrial temperature range, which is the best reported performance for a MEMS frequency reference.
- In Paper 11.7, Delft University of Technology proposes a voltage-calibration scheme for a deep-submicron CMOS temperature sensor. After calibration, the sensor achieves an inaccuracy of ±0.15°C from -55 to 125°C, and is the most energy-efficient BJT-based temperature sensor ever reported.
- In Paper 11.8, Intel demonstrates that BJT-based temperature sensors can reliably be realized in highly scaled 32 and 22nm technologies. Not only are the resulting sensors some of the smallest ever reported, their 10-to-100μs conversion times make them fast enough for hot-spot monitoring in multi-core microprocessors.

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Session 11 Highlights: Sensors and MEMS

[11.4] ASIC for a Resonant Wireless Pressure-Sensing System for Harsh Environments Achieving ±2% Error Between -40 and 150°C Using Q-Based Temperature Compensation

[11.6] A Temperature-to-Digital Converter for a MEMS-based Programmable Oscillator With Better Than ±0.5ppm Frequency Stability

Paper 11.4 Authors: M. Rocznik, J. Vanderhagen, F. Henrici and R. Has
Paper 11.4 Affiliation: Robert Bosch, Palo Alto, California

Paper 11.6 Authors: M. Perrott, J. Salvia,F. Lee, A. Partridge,S. Mukherjee, C. Arft, J.-T. Kim,N. Arumugam, P. Gupta,S. Tabatabaei, S. Pamarti, H. Lee and F. Assaderaghi
Paper 11.6 Affiliation: SiTime, Sunnyvale, California

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany

CONTEXT AND STATE OF THE ART

- Paper 11.4 by Bosch proposes an automotive solution for wireless pressure sensing in harsh environments. The system uses resonant coupling between a sealed capacitive pressure sensor and a readout ASIC to protect the circuit from potentially corrosive gases.
- Paper 11.6 by SiTime describes the first use of a MEMS-thermistor-based temperature sensor to stabilize a MEMS frequency reference.

TECHNICAL HIGHLIGHTS

- **Resonant coupling between a capacitive sensor and a readout circuit:**
- The system in Paper 11.4 achieves ±2% error between -40 and 150°C using Q-based temperature compensation and a 1kS/s readout rate. The circuit also facilitates automatic frequency tuning to compensate for manufacturing tolerances.
- **First use of a MEMS-thermistor for high-resolution, high-stability temperature sensing, along with an innovative readout circuit:**
- The system in Paper 11.6 achieves a frequency stability of <0.5ppm over the industrial temperature range, which is the best reported performance for a MEMS frequency reference.

APPLICATIONS AND ECONOMIC IMPACT

- The capacitive pressure sensor will open up new automotive applications.
- MEMS frequency references will compete with crystal oscillators, while offering smaller size and increased robustness to shock and vibration.

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Session 12 Overview : Multimedia and Communications SoCs

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Session Co-Chair: Shannon Morton, NVIDIA, Bristol, UK

Subcommittee Chair: Tzi-Dar Chiueh, National Chip Implementation Center, Hsin-Chu, Taiwan, Energy-Efficient Digital

Multimedia and communications SoCs are becoming extremely complex, requiring a variety of different solutions for consumer and mobile applications. State-of-the-art presentations in this field include Samsung's next-generation application processor in 32nm high-k metal-gate LPCMOS, which is targeted for smartphone applications. Advances in object-recognition processing from KAIST enable fast and accurate detection of moving-target objects, which can be useful in unmanned aerial vehicle (UAV) applications. Emerging applications for 60GHz communications are facilitated by the first complete transceiver system presented by the Tokyo Institute of Technology and Sony.

- In Paper 12.1, Samsung presents a 32nm Exynos™ application processor with multi-core CPU and GPU engines employing multiple power planes, a 1MB L2 cache, and thermal sensors to efficiently manage power across the die.
- In Paper 12.2, the Technical University of Dresden describes a 65nm, 1.1-to-1.35V, 4G detection-decoding engine that supports soft-output 64QAM 4×4 MIMO signaling and operates at 381MHz in a 65nm CMOS process. Data rates of 923Mb/s are achieved with just 50mW power dissipation.
- In Paper 12.3, the Tokyo Institute of Technology and Sony describe the first complete 40nm 1.1V 60GHz 16QAM transceiver system including RF, analog, and baseband functions. The system supports all four 60GHz channels, and achieves 6.3Gb/s data rates with less than 600mW total system power.
- In Paper 12.4, KAIST describes a 1.2V 0.13µm 32mm^2 real-time moving-object recognition processor utilizing simultaneous multi-threaded feature extraction, key-point matching, and dynamic resource control. The processor is implemented in 0.13µm CMOS, dissipates 320mW, and achieves 640GOPS/W during 720p video recognition.
- In Paper 12.5, Toshiba describes a 1.1V 40nm 44.5mm^2 real-time image recognition processor using a heterogeneous multi-core SoC and several image processing accelerators. Manufactured in a 40nm process, the SoC consumes a maximum of 749mW at 620GOPS/W efficiency.
- In Paper 12.6, Waseda University and Shanghai Jiao Tong University describe the first single-chip implementation of a Super Hi-Vision video decoder supporting a resolution of 7680×4320 pixels at 60fps. At 16mm^2 in 65nm CMOS at 1.2V, it dissipates 410mW and can be used to decode 16 HD streams for 3DTV applications.
- In Paper 12.7, Texas Instruments describes a programmable low-power full HD codec used in the 1.1V nominal AVS-adaptable 45nm OMAP™ 4 application processor. The codec supports a plethora of video industry standards and focuses on reducing DDR bandwidth and adaptive voltage scaling to achieve less than 145mW power dissipation.

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Session 12 Highlights : Multimedia and Communications SoCs

[12.3] A Full 4-Channel 6.3Gb/s 60GHz Direct-Conversion Transceiver With Low-Power Analog and Digital Baseband Circuitry

Paper 12.3 Authors: K. Okada[1], K. Kondou[2], M. Miyahara[1], M. Shinagawa[2], H. Asada[1], R. Minami[1], T. Yamaguchi[1], A. Musa[1], Y. Tsukui[1], Y. Asakura[2], S. Tamonoki[2], H. Yamagishi[2], Y. Hino[2], T. Sato[1], H. Sakaguchi[1], N. Shimasaki[1], T. Ito[1], Y. Takeuchi[1], N. Li[1], Q. Bu[1], R. Murakami[1], K. Bunsen[1], K. Matsushita[1], M. Noda[2], A. Matsuzawa[1]
Paper 12.3 Affiliation: [1]Tokyo Institute of Technology, [2]Sony Corporation, Tokyo, Japan

Subcommittee Chair: Tzi-Dar Chiueh, National Chip Implementation Center, Hsinchu, Taiwan, Energy-Efficient Digital

CONTEXT AND STATE OF THE ART

- Tired of connecting USB or Firewire cables to your camera, MP3 player, laptop, etc.? Tired of waiting minutes for up and downloading video and music content?
- The 60GHz band is a free and unlicensed band with a large worldwide overlap. Its large bandwidth enables the wireless transmission of very high volumes of information at very high speed.
- During recent years, partial solutions, mostly RF (radio frequency) have been demonstrated at ISSCC.

TECHNICAL HIGHLIGHTS

- **First ever complete 60GHz transceiver in silicon**
- In Paper 12.3, the Tokyo Institute of Technology and Sony Corporation present the first complete 60GHz direct-conversion transceiver on silicon, comprising a 65nm CMOS front-end IC that consumes 319mW and 223mW in transmitting and receiving mode, respectively, and a 40nm CMOS baseband IC that operates at 1.1V and consumes 196mW and 398mW for 16QAM in transmitting and receiving mode.
- The entire system, including both RF (radio frequency) and BB (baseband) ICs, using a 6dBi antenna built in an organic package can transmit 3.1Gb/s over 1.8m in QPSK, and 6.3Gb/s over 0.05m in 16QAM mode.

APPLICATIONS AND ECONOMIC IMPACT

- With multi-Gb/s transmission speed, one can upload a music album in one second, or a movie in 10 seconds, all without any connecting cables.

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Session 12 Highlights : Multimedia and Communications SoCs

[12.6] A 2Gpixel/s H.264/AVC HP/MVC Video Decoder Chip for Super Hi-Vision and 3DTV/FTV Applications

[12.7] A True Multistandard, Programmable, Low-Power, Full HD Video-Codec Engine for Smartphone SoC

Paper 12.6 Authors: D. Zhou[1], J. Zhou[1], J. Zhu[2], P. Liu[2], S. Goto[1]
Paper 12.6 Affiliation: [1]Waseda University, Kitakyushu, Japan; [2]Shanghai Jiao Tong University, Shanghai, China

Paper 12.7 Authors: M. Mehendale, S. Das, M. Sharma, M. Mody, R. Reddy, J. Meehan, H. Tamama, B. Carlson, M. Polley
Paper 12.7 Affiliation: Texas Instruments, Bangalore, India; Nice France; Dallas, TX

Subcommittee Chair: Tzi-Dar Chiueh, National Chip Implementation Center, Hsinchu, Taiwan, Energy-Efficient Digital

CONTEXT AND STATE OF THE ART

- Consumer demand for high-quality video has made high-definition 1080p video encoding and decoding a mandatory feature of smartphones and other mobile devices. To be most useful, a mobile device must encode and decode a wide range of video standards to interoperate with the range of video equipment available on the network and the range of video content available on the Internet. Additionally, the device should be flexible for supporting new video features such as 3D video.
- Dedicated hardware capable of power-efficient high-definition 1080p video encode and decode has reached mainstream production in application processors for smartphones. The near future holds another 16× increase in resolution.

TECHNICAL HIGHLIGHTS

- **High-definition video engine for smartphone SoC features support for 14 different video standards**
- In Paper 12.7, Texas Instruments presents a 1.1V nominal AVS-adjusted 45nm video engine capable of low-power encode and decode in a production smartphone. It uses semi-programmable hardware accelerators integrated into the smartphone SoC system, achieving power dissipation as low as 100mW for 1080p H.264 base profile.
- **Worlds first single-chip 8k×4k video resolution Super Hi-Vision (SHV) decoder implementation**
- In Paper 12.6, Waseda University and Shanghai Jiao Tong University present a 1.2V 65nm 8k×4k video resolution Super Hi-Vision (SHV) 16mm^2 decoder chip. They achieve 16× the resolution of standard 1080p high-definition video at only 410mW. Computing parallelism and bandwidth-reduction techniques are employed to achieve this new performance level.

APPLICATIONS AND ECONOMIC IMPACT

- The 1920×1080 high-definition low-power video engine in the production SoC enables a smartphone to function as a high-quality camcorder, a multi-standard video player, or a portable videoconferencing device.
- The 8K×4K Super Hi-Vision video decoder chip can be used for bigger and better digital TV or 16 encoded views to enable new applications like glasses-free 3D TV.

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Session 13 Overview : High-Performance Embedded SRAM

MEMORY SUBCOMMITTEE

Session Chair: Leland Chang, IBM, Yorktown Heights, NY
Session Co-Chair: Michael Clinton, Texas Instruments, Dallas, TX

Subcommittee Chair: Kevin Zhang, Intel, Hillsboro, OR, Memory

Continued scaling of embedded SRAM into the 22nm node and beyond will be critical to VLSI applications ranging from high-performance computing to low-power consumer electronics. With growing variability and power constraints, the introduction of new transistor structures such as tri-gate, continued reliance on assist techniques, and the use of novel access schemes will be key to maintaining robustness, area efficiency, and low voltage operation in aggressively scaled memories. The papers in this session present innovations that will drive continued improvements in performance and power efficiency for high-performance embedded memories.

- In Paper 13.1, Intel describes the first tri-gate 6T-SRAM at the 22nm node with the smallest bit cells (0.092μm^2 for high density and 0.108μm^2 for low voltage) demonstrated to date and 175mV lower Vmin and 1.7× faster performance than 32nm designs.
- In Paper 13.2, University of Tokyo describes a post-fabrication technique that pinpoints and repairs only weak cells in a large SRAM array by hot carrier injection to realize 57% faster read delay and 31% energy reduction.
- In Paper 13.3, Intel describes a 22nm 8T-SRAM that leverages intrinsic device and interconnect coupling capacitance to boost wordline voltages without level shifters, charge pumps, or separate supplies, which improves write V_{MIN} by 140mV.
- In Paper 13.4, Renesas describes a 28nm two-port SRAM that circumvents read disturbs by time shifting simultaneous port activation to achieve high-speed read access latency of 360ps.

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Session 13 Highlights : High-Performance Embedded SRAM

[13.1] A 4.6GHz 162Mb SRAM Design in 22nm Tri-Gate CMOS Technology With Integrated Active V_{MIN}-Enhancing Assist Circuitry

Paper Authors: E. Karl, Y. Wang, Y.-G. Ng, F. Hamzaoglu, U. Bhattacharya, K. Zhang, K. Mistry, and M. Bohr
Paper Affiliation: Intel, Hillsboro, OR

Subcommittee Chair: Kevin Zhang, Intel, Hillsboro, OR, Memory

CONTEXT AND STATE OF THE ART

- Previous state-of-the-art 6T-SRAM demonstration (Texas Instruments, ISSCC 2011): 28nm planar bulk CMOS, 0.12μm^2 cell.
- Previous Intel 6T-SRAM (ISSCC 2010): 32nm planar bulk CMOS with high-k/metal-gate, 0.171μm^2 cell size, 4.2mm^2/Mb, 2GHz operation at 0.8V.

TECHNICAL HIGHLIGHTS

- **World's smallest embedded SRAM cell (and first 22nm node tri-gate 6T-SRAM demonstration)**:
- In Paper 13.1, Intel describes the first tri-gate 6T-SRAM at the 22nm node with the smallest bit cells (0.092μm^2 for high density and 0.108μm^2 for low voltage) demonstrated to date and 175mV lower Vmin and 1.7× faster performance than 32nm designs.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrates continued Moore's Law scaling of SRAM bit cells at the 22nm node.
- Enables dense, low-power embedded caches for advanced microprocessor and consumer applications.

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Session 14 Overview : Digital Clocking and PLLs

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: Anthony Hill, Texas Instruments, Dallas, TX
Session Co-Chair: Hiroo Hayashi, Toshiba, Kawasaki, Japan

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

Many analog components are now leveraging digital technology. PLLs are increasingly integrating digital techniques and building blocks and are being built directly on digital SoCs. This integration continues to reduce power and cost in systems. This session begins with four papers on digital PLLs that showcase new design techniques. This includes an MDLL with a 400fs jitter and a PLL using cutting-edge 22nm process technology. We also have an innovative PLL that advances critical figures-of-merit through use of digital techniques.

- In Paper 14.1, Samsung presents a 32nm time-domain 0.004mm^2 250µW TDC with a time-difference accumulator and a 0.012mm^2 0.85V 2.5mW ADPLL.
- In Paper 14.2, Oregon State University presents a calibration-free digital MDLL using a 1b TDC and an efficient regulator to reduce output jitter in the presence of large supply noise. Fabricated in 0.13µm CMOS, the MDLL consumes 890µW at 1.5GHz output frequency and achieves 400fs jitter and better than 20fs/mV supply noise sensitivity.
- In Paper 14.3, National Taiwan University describes a low-area wide-range ADDLL. The NOR-gated ring oscillators replace the coarse delay line used in the phase-tracking delay unit for low cost with a 6.7MHz-to-1.24GHz operating range at 1.2V consuming 14.5mW. The locking time remains at five cycles regardless of the input frequency and the chip occupies 0.0318mm^2 active area in 90nm CMOS.
- In Paper 14.4, Intel demonstrates a TDC-less ADPLL to provide dynamic tuning, scalability, and power/area efficiency in mobile SoC designs. A ring-oscillator-based DCO that dissipates less than 1mW/GHz over a frequency range from 0.20 to 3.20GHz is shown. The loop locks within 300 reference clock cycles with an rms period jitter of 1.15ps at 1GHz within an area of 140×120µm^2 in 22nm high-k, tri-gate CMOS.
- In Paper 14.5, Toshiba presents a 65nm 0.32mm^2 digitally-stabilized type-III PLL with a ring VCO. It exhibits 1.01ps$_{rms}$ integrated jitter at 3.24GHz consuming 27.5mW at 1.2V.

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Session 14 Highlights : Digital Clocking and PLLs

[14.1] A 0.004mm² 250μW ΔΣ TDC With Time-Difference Accumulator and a 0.012mm² 2.5mW Bang-Bang Digital PLL Using PRNG for Low-Power SoC Applications

[14.4] A TDC-Less ADPLL With 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS

Paper 14.1 Authors: J-P. Hong, S-J. Kim, J. Liu, N. Xing, T-K. Jang, J. Park, J. Kim,T. Kim, and H. Park
Paper 14.1 Affiliation: Samsung Electronics, Yongin, Korea

Paper 14.4 Authors: N. August, H.-J. Lee, M. Vandepas
Paper 14.4 Affiliation: *Intel, Portland, OR*

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital

CONTEXT AND STATE OF THE ART

- Phase-locked loops (PLLs) provide the heartbeat of all processors – from mobile/handheld to large compute farms in data centers. No modern processors could be constructed without them.
- Historically, PLLs for high-performance and mobile processors were built with analog components. In many cases, this requires custom manufacturing processes and increases cost. The emergence and adoption of all-digital PLLs is driving further cost reduction in modern processors as they eliminate many of the custom design steps and components.
- Power optimization of modern processors is critically important to maximizing battery life. The development of digital PLLs has directly led to power reduction in mobile and desktop processors, which extends battery life and gives consumers more for less. All-digital PLLs offer up to 10× power and area improvement over analog PLLs and portability from process to process.

TECHNICAL HIGHLIGHTS

- **Samsung presents a tiny all-digital phase-locked loop for mobile applications:**
- In Paper 14.1, Samsung presents an impressively small 0.012mm² all-digital PLL in 32nm CMOS technology targeted for mobile applications. They do this while drawing a mere 2.5mW of power.
- **The world's first 22nm digital phase-locked loop using Intel's 3D transistors:**
- In Paper 14.4, Intel presents a 0.017mm² 3mW all-digital PLL in 22nm tri-gate 3D technology. This is the smallest reported process geometry for a digital PLL implementation.

APPLICATIONS AND ECONOMIC IMPACT

- Low-jitter digital PLLs enable less-complex and costly design for leading-edge devices. They are a key enabler for reducing cost and making complex devices more widely available to consumers.
- This class of digital phase-locked loops will continue driving integration of digital systems.

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Session 15 Overview: mm-Wave and THz Techniques

RF SUBCOMMITTEE

Session Chair: Ehsan Afshari, Cornell University, Ithaca, NY
Session Co-Chair: Yorgos Palaskas, Intel Labs, Hillsboro, OR

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF

Millimeter-wave and terahertz frequencies have many applications in short-range, high-data-rate communication systems, medical imaging and sensing, and spectroscopy. Implementation of these systems in deep-submicron CMOS is challenging. Papers in this session describe various aspects of signal generation, amplification, frequency multiplication, imaging and mm-Wave system integration.

- In Paper 15.1, ST microelectronics presents a 1kpixel silicon-lens integrated camera for active THz applications in 65nm CMOS. Each pixel includes a ring antenna, a resistive mixer, row/col select and an integrate-and-dump circuit.
- In Paper 15.2, the University of Florida presents two terahertz imagers at 280 and 860GHz using Schottky diodes in standard 0.13µm CMOS. The first is a lens-less 16-pixel imager and the second one is a single pixel detector.
- In Paper 15.3, Caltech presents a scalable transmitter architecture for power generation and beamforming at 280GHz in 45nm SOI CMOS. The two-dimensional 4x4 array radiates with an EIRP of +9.4dBm and beam-steers in 2D over 80° in azimuth and elevation.
- In Paper 15.4, Cornell presents a terahertz varactor-less VCO inspired by the theory of coupled-mode oscillators. Two VCOs are implemented at 283 to 296GHz and 318 to 326GHz with peak output powers of 0.76mW and 0.46mW both in a 65nm bulk CMOS.
- In Paper 15.5, NTU presents a 1V 79GHz power amplifier with 8-path power-combining technique in 65nm CMOS. The power amplifier achieves the saturated power of 19.3dBm and PAE of 19.2% for an area of only 0.855mm^2.
- In Paper 15.6, Nanyang Technological University presents an efficient mm-Wave frequency quadrupler at 121 to 137GHz in 0.13µm SiGe BiCMOS. The generated output power is -2.4dBm with core efficiency of 9%, drawing 1.6mA from a 1.6V supply.
- In Paper 15.7, UCLA presents a 144GHz 3D-imaging phase-based radar that alleviates range ambiguity with ranging measurements at different IF frequencies. The 65nm CMOS chipset achieves measured depth resolution of 0.76cm.
- In Paper 15.8, Toshiba presents a 65nm CMOS transceiver chipset incorporating RF chip with in-package antenna and PHY/MAC chip with fast TX-RX switching to optimize MAC throughput. The transceiver achieves 2.07Gb/s throughput over 3cm distance.
- In Paper 15.9, imec presents a 0.7mm^2, low-power 60GHz transceiver in 40nm CMOS that achieves 7Gb/s data rate in all 60GHz band channels using a subharmonic injection-locked VCO with 8GHz locking range.
- In Paper 15.10, HKUST presents a 65nm CMOS 4-path LO generation scheme for mm-Wave phased arrays consisting of injection-locked phase shifters with on-chip successive-approximation calibration that achieves an rms phase step error of 0.93^o.

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Session 15 Highlights : mm-Wave and THz Techniques

[15.1] A 1kPixel CMOS Camera Chip for 25fps Real-Time Terahertz Imaging Applications

[15.2] 280GHz and 860GHz Image Sensors Using Schottky-Barrier Diodes in 0.13μm Digital CMOS

Paper Authors: H. Sherry[123], J. Grzyb[1], Y. Zhao[1], R. Al Hadi[1], A. Cathelin[2], A. Kaiser[3], U.Pfeiffer[1]
Paper Affiliation: [1]University of Wuppertal, Wuppertal, Germany, [2]STMicroelectronics, Crolles, France, [3]ISEN, Lille, France

Paper Authors: R. Han [1,3], Y. Zhang[2], Y. Kim[2], D. Y. Kim[2], H. Shichijo[2], E. Afshari[3], K. K. O[2]
Paper Affiliation: [1]University of Florida, Gainesville, FL, [2]University of Texas at Dallas, Richardson, TX, [3]Cornell University, Ithaca, NY

Subcommittee Chair: A. Cathelin, STMicroelectronics, Crolles, France, RF

CONTEXT AND STATE OF THE ART

- Electromagnetic waves at 300 GHz and above, broadly known as “terahertz waves”, are able to penetrate clothing, clouds, and other materials. As such, low-cost terahertz cameras are useful for security, navigation, and biomedical applications.
- Existing terahertz imaging sensors primarily rely on compound-semiconductor technology. At ISSCC 2012, two papers, 15.1 and 15.2, demonstrate terahertz imaging sensors operating from 300 to 900 GHz, implemented in conventional low-cost CMOS technology.

TECHNICAL HIGHLIGHTS

- **World’s first integrated Terahertz, 1k-pixel real-time camera in 65-nm CMOS**
- Paper 15.1 demonstrates a Terahertz camera for real-time imaging at frequencies between 600 and 900GHz in conventional 65nm CMOS. The imaging array includes on-chip antennas, passive mixers, and a read-out solution for the 1kpixel camera. This imager has been demonstrated using an external lens and an external terahertz source for real-time, 24 frame-per-second, terahertz imaging.
- **The 16 pixel image sensor integrates antenna and power detectors while achieving record sensitivity**
- Paper 15.2 demonstrates a 16-pixel image sensor for broadband sub-millimeter-wave imaging using 0.13μm CMOS. The imager includes on-chip antennas and power detectors implemented with Schottky-diodes. The chip has been characterized at 280 and 860 GHz and exhibits record sensitivity.

APPLICATIONS AND ECONOMIC IMPACT

- Low-cost CMOS sensors will dramatically reduce the cost of a terahertz imaging system when used together with low-cost terahertz sources, some of which are also being demonstrated at ISSCC 2012.
- Low-cost terahertz cameras will be useful for security scanning, biomedical imaging, and manufacturing control applications.

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Session 16 Overview : Switching Power Control Techniques

ANALOG SUBCOMMITTEE

Session Chair: Baher Haroun, Texas Instruments, Dallas
Session Co-Chair: Gyu-Hyeong Cho, KAIST, South Korea

Subcommittee Chair: Bill Redman-White, University of Southampton, UK, Analog Subcommittee

Multiple efficient LED drivers are presented, in the first half of this session. Two approaches for 5-output Single-Input Multiple-Output DC-DC converters, using adaptive energy recovery and a combined switched capacitor with absolute inductor current emulation techniques, are presented. For LED lamps, a cost-effective and novel primary-side regulation method is disclosed. The second half of the session addresses evolving areas for efficient power converters; a wide range high-conversion-ratio switched-capacitor converter, a very-high-voltage Silicon Carbide JFET switching driver and inductive power transmission techniques.

- Paper 16.1 by MediaTek presents a single-inductor 5-output buck converter with adaptive energy-recovery control technique with 67µV/mA cross-regulation and 1.2W/mm^2 in 65 nm CMOS.
- Paper 16.2 by KAIST presents an efficient AMOLED 5-output SIMO DC-DC, using absolute inductor current emulation and 2 flying switched capacitors to reduce voltage stress while balancing and sharing energy. The chip occupies 4.56mm^2 in a 0.5µm power BCD process.
- Paper 16.3 by Anaperior Technology presents a 12W LED lamp driver in a 0.35µm BCD process supporting TRIAC dimming with 0.98 power factor using off-the-line primary-side regulation not requiring an optical isolator.
- Paper 16.4 by University of Pavia presents a 0.1-to-2A scalable buck-boost DC-DC for LED Drivers with 91%-efficiency occupying 4.125mm^2 in 0.18µm CMOS with 5V option.
- Paper 16.5 by University of California at Berkeley presents a 7.5-to-13.5V switched capacitor DC-DC converter using feedback and feedforward control to regulate a 1.5V output with 92% efficiency in 11.55mm^2 of a 0.18 m CMOS process.
- Paper 16.6 by Infineon Technologies presents a 1400V galvanically isolated SiC JFET gate driver for DC-DC converters achieves 99% efficiency using both 0.6µm BiCMOS and 0.8µm BCD process technologies.
- Paper 16.7 by Georgia Institute of Technology presents a 13.56MHz inductively coupled power transmission using an automatically reconfigurable active voltage doubler/rectifier with 77% power conversion efficiency occupies 1mm^2 in a 0.5µm CMOS process.
- Paper 16.8 by Keio University presents a 0.18µm CMOS 13.56MHz sub-harmonic resonant switching wireless power delivery system with suppressed spurious emission up to 0.52W with 50% power conversion efficiency occupying 6.25mm^2 for each of the transmitter and rectifier chips.

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Session 16 Highlights : Switching Power Control Techniques

[16.3] Off-the-Line Primary-Side Regulation LED Lamp Driver With Single-Stage PFC and TRIAC Dimming Using LED Forward Voltage and Duty Variation Tracking Control

Paper Authors: J. T. Hwang, M. S. Jung, D. H. Kim, J. H. Lee, M. H. Jung, J. H. Shin
Paper Affiliation: Anaperior Technology, Seoul, Korea

Subcommittee Chair: Bill Redman-White, University of Southampton, Southampton, UK, Analog Subcommittee

CONTEXT AND STATE OF THE ART

- Primary-side regulation flyback converters have been of interest in LED drivers because they require neither current-sensing circuits nor opto-isolators unlike conventional flyback converters. However, they do not meet load and line regulations.

TECHNICAL HIGHLIGHTS

- **Improved regulation addresses a key challenge for LED lighting:**
- Paper 16.3 presents a new primary-side regulation method for LED lamps, which solves the load and line regulation problem, based on LED forward voltage and duty variation tracking methods.
- The chip is implemented in a 0.35μm BCD process and achieves above 81% efficiency in the 6-to-12W output range, under 2% line regulation in 180-to-260Vac and maximum 0.98 power factor.

APPLICATIONS AND ECONOMIC IMPACT

- This design can provide viable and cost-effective primary-side regulation flyback converter solutions for isolated LED drivers, which are in many cases preferred for safety as the transformer used isolates the lamp from the line voltage.

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Session 17 Overview: Diagnostic and Therapeutic Technologies for Health

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: Alison Burdett, Toumaz, UK
Session Co-Chair: Fu-Lung Hsueh, TSMC, Taiwan

Subcommittee Chair: Siva Narendra, Tyfone, Portland OR, Technology Directions

Advanced semiconductor systems-on-chip combined with miniaturized sensors enable the development of low-cost and compact devices for mobile healthcare applications. The implementation of small and lightweight systems allows integration into form factors that provide a high level of comfort and wearability to the patient, allowing the delivery of next-generation diagnostics and therapy outside of a traditional clinical setting. This has the potential to provide patients with a higher quality-of-life while reducing healthcare costs.

This session presents recent advances in semiconductor devices for health status diagnosis and therapy, from ICs for wearable monitoring and analysis of physiological signals including ECG and EEG, to SoCs for therapeutic applications such as electro-acupuncture, and even future applications such as sensing, imaging and minimally invasive surgery enabled by the development of remote-controlled implantable locomotive devices.

- Paper 17.1 from Masdar Institute of Science and Technology, describes an 8-channel scalable EEG acquisition system. The 25mm^2, 0.18μm CMOS chip integrates an EEG analog front-end with an application-specific seizure-classification processor, resulting in a power consumption as low as 2.03μJ per classification within a 2-second classification window.
- Paper 17.2 from KAIST, describes an IC for mental-health-status monitoring, which is designed to be integrated into a fabric headband. The 0.13μm CMOS chip integrates a sensor front-end, ADC, custom algorithmic processing and body-channel communication within 11.75mm^2. Total system power consumption is less than 260μW when acquiring and processing EEG signals for stress analysis.
- Paper 17.3 from KAIST presents an adaptive stimulator IC for a compact electro-acupuncture patch system. The 0.13μm CMOS chip consumes 6.8mW at 1.2V, and supports 32 different drive current levels with high-precision DC balancing (< 10nA).
- Paper 17.4 from the University of Washington describes a wireless sensor node SoC powered solely from a body-worn thermoelectric generator. Implemented in 0.13μm CMOS, the chip dissipates less than 19μW while performing ECG heart-rate extraction and wireless transmission at 400/433MHz.
- Paper 17.5 from Toumaz describes a multi-mode wireless transceiver for wireless body-area networks. The power consumption of the 0.13μm CMOS chip is 5mW for continuous 2.4GHz RX/TX, while satisfying IEEE 802.15.6/Bluetooth-LE PHY requirements.
- Paper 17.6 from Stanford presents a mm-sized wireless implantable system capable of controlled motion in fluid, implemented in 65nm CMOS. A 1.86GHz carrier delivers 500μW into the device to power locomotion, propelling the implant at a speed of 0.5cm/s.
- Paper 17.7 from KAIST describes a system designed to sort and analyze single cells in a microfluidic channel. The 0.13μm 0.38mm^2 CMOS IC compensates for the differential electrode drift in real-time for a total power consumption of 7.6mW.

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Session 17 Highlights : Diagnostic and Therapeutic Technologies for Health

[17.3] A Sub-10nA DC-Balanced Adaptive Stimulator IC With Multimodal Sensor for Compact Electro-Acupuncture System

Paper 17.3 Authors: K. Song, H. Lee, S. Hong, H. Cho
Paper 17.3 Affiliation: *KAIST, Daejeon, Korea*

Subcommittee Chair: Siva Narendra, Tyfone, Portland, OR

CONTEXT AND STATE OF THE ART

- Electro-acupuncture is a combination of acupuncture and electric current stimulation and accomplishes transcutaneous nerve stimulation, which has been widely used since the 1970s for chronic pain relief.
- Stimulation traditionally uses long wires and an external power supply, and it is very cumbersome to stimulate a large number of needles. In addition, state-of-the-art systems in open-loop fashion and do not reflect the real-time stimulation status.

TECHNICAL HIGHLIGHTS

- **The first compact electro-acupuncture patch**
- In Paper 17.3, a patch-type system is realized using planar fashionable PCB technology (a printed-circuit-on-fabric technology developed by KAIST) and is powered by a coin battery.
- This smart solution is multimodal: it measures EMG and temperature to analyze the stimulation status. It supplies a programmable adaptive stimulation current (40μA-to-1mA) with 32 different current levels.
- The SoC includes power management to generate a 3.3V stimulation voltage, a charge-balanced stimulator front-end with high-precision (<10nA) balancing, a low-noise (input noise 3.0μV_{rms}) front-end for EMG and temperature acquisition and digitization, body-channel communication and a system controller.

APPLICATIONS AND ECONOMIC IMPACT

- Practitioners have the opportunity to perform patient-specific treatment with increased safety.
- Patients enjoy increased convenience thanks to the patch-type wireless system.
- The electro-acupuncture market is currently approximately 2 billion USD.

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Session 17 Highlights : Diagnostic and Therapeutic Technologies for Health

[17.6] A mm-Sized Wirelessly Powered and Remotely Controlled Locomotive Implantable Device

Paper 17.6 Authors: A. Yakovlev, D. Pivonka, T.H. Meng, A.S.Y. Poon
Paper 17.6 Affiliation: Stanford University, Stanford, CA

Subcommittee Chair: Siva Narendra, Tyfone, Portland, OR

CONTEXT AND STATE OF THE ART

- Sensing, imaging and minimally invasive surgery benefit from positional and directional control. Achieving such propulsion is easily achieved in macroscopic systems but is very hard to miniaturize.
- State-of-the-art miniature propulsion can be piezoelectric or magnetic but this requires significant power and is difficult to control and scale.

TECHNICAL HIGHLIGHTS

- **The first ever miniature wirelessly powered implant with locomotion and remote control**
- This paper realizes a mm-sized wireless system capable of controlled motion in fluids at a speed of 0.5cm/s. The entire system occupies 0.6mm^2 in 65nm CMOS.
- The system is RF-powered through a TX antenna at a 1.86GHz carrier frequency and 500μW is delivered to the system. Wirelessly received data controls high-current drivers to power the locomotion with 0.5-to-2mA at 0.2V. The demodulator operates at 25Mb/s and consumes only 0.5pJ/b.

APPLICATIONS AND ECONOMIC IMPACT

- While this system does not yet achieve the objectives of the famous movie 'the Fantastic Voyage' (1969), it demonstrates extremely low-power electronics combined with remote powering to achieve a tiny remotely controlled locomotion device.

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Session 18 Overview : Innovative Circuits in Emerging Technology

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: Masaitsu Nakajima, Panasonic, Osaka
Session Co-Chair: Shekhar Borkar, Intel, Hillsboro

Subcommittee Chair: Siva Narendra, Tyfone, Portland, OR, Technology Directions

This session highlights seven exciting papers that cover a broad spectrum of technologies from organics to mainstream SOI and demonstrating a wide range of applications. The papers feature organics and heterogeneous technologies for inexpensive consumer applications, spanning energy harvesting and management, sensors, wireless communications, and novel concepts in self-healing to account for device aging.

- In Paper 18.1, the University of Tokyo proposes an organic electronics based pedometer in a shoe for a consumer fitness application. The system uses a piezoelectric energy harvester, a 2V PMOS rectifier, and a counter, whereby a negative voltage is generated by a charge pump to mimic pseudo-CMOS.
- In Paper 18.2, KU Leuven presents the first-ever organic electronics-based touch sensor for keypad applications. It features triangular 1D and 4×4 2D capacitive touch sensors. A sampling rate of 1.5kHz together with a localization accuracy of ~1mm are achieved, drawing 6μA from a 15V supply.
- In Paper 18.3, imec Leuven presents an RFID that demonstrates for the first time bi-directional communication using large-area low-temperature technology. The chip is based on hybrid organic oxide complementary technology and operates at supply voltages as low as 3.75V reaching an uplink speed of up to 1.2kb/s.
- In Paper 18.4, Eindhoven University of Technology demonstrates the application of amorphous Gallium-Indium-Zinc-Oxide TFTs in an impressive 6b 10MS/s current-steering DAC. The circuit, which can be integrated in a display backplane, exhibits a settling time of 4μs, DNL < 0.3 LSB and INL < 0.2 LSB, and achieves maximum SFDR of 55dB.
- In Paper 18.5, the University of California, Los Angeles presents a 60GHz 4Gb/s CMOS radio capable of self-healing to account for temperature, process variations, and device degradation over time. It uses a controller to optimize the mm-wave front-end, incurring only 10% area and 3% power overhead.
- In Paper 18.6, Holst Centre / imec demonstrates the hybrid combination of piezoelectric MEMS sensors and CMOS circuits to realize an electronic nose capable of detecting ethanol at 7.6ppm. The system consumes a peak power of 1.35mW, which reduces to only 23.4μW for a 1.7% duty cycle.
- In Paper 18.7, CEA-LETI-MINATEC shows a mass sensitivity as high as 1.2kHz/ag by integrating 1.2μm long, 80nm wide, 25nm thick NEMS resonators in a 0.3μm fully depleted SOI technology.

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Session 18 Highlights : Innovative Circuits in Emerging Technology

[18.1] Insole Pedometer With Piezoelectric Energy Harvester and 2V Organic Digital and Analog Circuits

Paper 18.1 Authors: K.Ishida[1], T. Huang[1], K. Honda[1], Y. Shinozuka[1], H. Fuketa[1], T. Yokota[1], U. Zschieschang[2], H. Klauk[2], G. Tortissier[1], T. Sekitani[1,3], M. Takamiya[1], H. Toshiyoshi[1], T. Someya[1,3], and T. Sakurai[1]

Paper 18.1 Affiliation: [1]University of Tokyo, Tokyo, Japan
[2]Max Planck Institute for Solid State Research, Stuttgart, Germany
[3]JST/ERATO, Tokyo, Japan

Subcommittee Chair: Siva Narendra, Tyfone, Portland, OR

CONTEXT AND STATE OF THE ART

- Conventional silicon circuits are well suited to realize flexible large-area energy harvesters.
- In energy-harvesting applications, the harvested power is small and the rectified voltage is in the 1V range.
- The principal design challenge for organic circuits using piezoelectric energy harvesting is the robust operation of PMOS-only circuits at low supply voltage.

TECHNICAL HIGHLIGHTS

- **The first self-powered wearable lifestyle system that uses organic electronics:**
- Paper 18.1 by the University of Tokyo, Tokyo, Japan and Max Plank Institute for Solid State Research, Stuttgart, Germany and JST/ERATO, Tokyo, Japan describes a 22×7cm^2 batteryless organic flexible pedometer integrated in a shoe harvesting at least 10μW power through 20×28cm^2 flexible piezoelectric films.
- The organic insole pedometer consists of a 2V all-PMOS rectifier, 14bit counter, a negative voltage generator and clock generator based on a Schmitt trigger that are made out 462 DNTT PMOS organic transistors with minimum gate lengths of 20μm (analog) and 50μm (digital).

APPLICATIONS AND ECONOMIC IMPACT

- This paper paves the way toward the realization of low-cost large-area energy-harvesting systems employing organic flexible electronics.

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Session 18 Highlights : Innovative Circuits in Emerging Technology

[18.7] Towards Ultra-Dense Arrays of VHF NEMS With FDSOI-CMOS Active Pixels for Sensing Applications

Paper 18.7 Authors: G.Arndt, C. Dupré, G. Cibrario, O. Rozeau, L. Duraffourg, E. Ollier, E. Colinet
Paper 18.7 Affiliation: CEA LETI MINATEC, Grenoble, France

Subcommittee Chair: Siva Narendra, Tyfone, Portland, OR

CONTEXT AND STATE OF THE ART

- Resonant Nano Electro Mechanical Systems (NEMS) based mass detectors are emerging devices because they offer extreme mass sensitivity. Their submicron dimensions make them converge towards CMOS fabrication.
- Compact integration of multiple NEMS with their readout electronics on a common die is required to design robust systems with even higher performance.
- Previous NEMS-CMOS co-integration chips reported in the literature offer a low mass sensitivity and were unable to address extreme mass sensing applications because the NEMS resonators were relatively large and are made with non-single-crystal silicon exhibiting poor mechanical characteristics.

TECHNICAL HIGHLIGHTS

- The first NEMS resonator co-integrated with a 0.3μm fully depleted SOI technology:
- Paper 18.7 by CEA-LETI-MINATEC presents the first realization on a 30×30μm^2 single chip of a fully co-integrated 100MHz NEMS resonator with a 0.3μm fully depleted SOI technology.
- By using a NEMS resonator, a beam of 1.2μm length 80nm width and 25nm thickness, a mass sensitivity of 1.2kHz/ag is achieved, which is 1000× better than state-of-the-art work.

APPLICATIONS AND ECONOMIC IMPACT

- In the next 5 to 10 years, NEMS should offer a real breakthrough for mass spectrometry or gas analysis applications because they can achieve similar resolution to conventional lab equipment, but at a lower cost due to their compatibility with VLSI processes. This work paves the way toward the integration of large NEMS arrays for mass-sensing applications in a similar fashion to what happened for CMOS imagers.

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Session 19 Overview : 20+ Gb/s Wireline Transceivers and Injection-Locked Clocking

WIRELINE SUBCOMMITTEE

Session Chair: Ken Chang, Xilinx, San Jose, CA
Session Co-Chair: SeongHwan Cho, KAIST, Korea

Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY, Wireline

In an effort to keep pace with increasing data demands, standards such as 100GBe and OIF CEI-25G are evolving to require the transmission of ever-higher data rates through existing channels. Faster data rates extending electrical and optical communication capabilities can only be achieved with advancements in equalization architectures, equalization circuits, and signal modulation schemes. Additionally, stringent timing and power requirements push the need for ultra-low jitter clocks, demanding innovative techniques such as injection locking. This session includes three papers demonstrating 28Gb/s transceivers for backplane and chip-to-chip applications, as well as two papers describing optical transceivers supporting advanced modulation schemes for communication beyond 40Gb/s. Also described in the session is a multi-mode transceiver capable of 20+ Gb/s data transfers over plastic, copper, and short-reach wireless channels. The final two papers in the session discuss self-calibrated and fractional-N-suitable injection-locking techniques, respectively.

- In Paper 19.1, IBM describes the first 28Gb/s transceiver addressing medium reach, 35dB loss, electrical channels in 32nm SOI CMOS that features a source-series terminated driver with 4-tap FFE, a two-stage peaking amplifier with active feedback topology, and a 15-tap DFE. The transceiver consumes 693mW per lane; the per-TX/RX port area with PLL contribution amortized is 0.81 mm^2.
- In Paper 19.2, Inphi demonstrates a power-efficient 28Gb/s SerDes using a 3-tap TX FIR and adaptive linear equalization developed in 40nm CMOS for chip-to-chip and chip-to-module communications. The worst-case power at high voltage and temperature is 225mW per TX/RX lane with a BER of $<10^{-15}$ over -13dB channels; each TX/RX pair occupies 0.9 mm^2.
- In Paper 19.3, ClariPhy describes a 40nm CMOS DSP-based transceiver for coherent optical communications at 50Gb/s. The chip integrates the transmitter, receiver, framer and host interface, and features a 25Gs/s 6b ADC with a FOM of 0.4pJ/conversion. The 75 mm^2, 40-million gate -count chip consumes 25W from a nominal 1.2V supply and compensates 200ps differential group delay, 8,000ps^2 2nd-order polarization-mode dispersion and 55ns/nm chromatic dispersion.
- In Paper 19.4, Broadcom describes a dual-23Gb/s chipset designed in 40nm CMOS for 40Gb/s DQPSK transmission. The TX has a 2-tap FIR and exhibits 10ps rise/fall time, 0.2ps_{rms} RJ, 0.8ps_{pp} DJ, and ±0.5UI skew adjustment to clock. The RX includes a peaking filter, decision threshold adjustment, and 1-tap loop-unrolled DFE, achieves 7mV_{ppd} input sensitivity and 0.7UI_{pp} high-frequency jitter tolerance. The TX occupies 2.8mm^2 and consumes 0.63W from 1V/1.5V supplies while the RX occupies 6mm^2 and dissipates 1.2W from a 1V supply, including 20G front-end and SFI 5.1 TX and RX interfaces.
- In Paper 19.5, Sony and Caltech describe a versatile multi-modality transceiver that enables data transmission over three types of transmission media: copper wireline, dielectric waveguide, and wireless using the exact same circuit. The fabricated chipset in 40nm low-power logic CMOS technology with impedance transformation-based diplexer enables single-pad frequency multiplexing, and demonstrates data transmission at rates up to 29.6Gb/s. The active footprints including diplexer/de-diplexer are 0.16mm^2 and 0.26mm^2, for the TX and RX chips, respectively; the TX consumes 52mW and the RX 85mW from 1.1V supplies.
- In Paper 19.6, IBM demonstrates a 28Gb/s source-series-terminated (SST) TX targets emerging 25-to-28Gb/s I/O standards. The TX features a 4-tap FFE, duty-cycle adjustment, PVT driver impedance correction, T-coil impedance

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matching, and a true/complementary output skew function. Implemented in 32nm CMOS SOI, the circuit consumes 217mW at 28Gb/s (7.75mW/Gb/s), at a nominal supply of 1.1V; area of the TX macro is .036 mm^2.

- In Paper 19.7, KAIST describes the first injection-locked ADPLL capable of changing the output frequency in fractional steps of the reference frequency. Implemented in 65nm CMOS, the ring-oscillator-based PLL achieves a 1MHz frequency step size using a 32MHz reference, and exhibits 4.2ps of rms jitter at 580MHz while consuming 10.5mW.
- In Paper 19.8, National Taiwan U shows a sub-harmonically injection-locked LC-PLL implemented in 0.18μm CMOS with optimized injection timing and achieves 145fs_{rms} jitter at 2.4GHz while consuming 12.6mW from a 1.8V supply. The self-calibrated injection scheme improves the robustness of the PLL to PVT variations.

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Session 19 Highlights : 20+ Gb/s Wireline Transceivers and Injection-Locked Clocking

[19.1] A 28Gb/s 4-Tap FFE/15-Tap DFE Serial-Link Transceiver in 32nm SOI CMOS Technology

Paper [19.1] Authors: J.Bulzacchelli, T.Beukema, D.Storaska P.-H.Hsieh, S.Rylov, D. Furrer, D.Gardellini, A.Prati, C.Menolfi, D.Hanson, J.Hertle, T.Morf, V.Sharma, R.Kelkar, H.Ainspan, W.Kelly, G.Ritter, J.Garlett, R.Callan, T.Toifl, D.Friedman
Paper [19.1] Affiliation: IBM Research, Yorktown Heights, USA

Subcommittee Chair: Daniel Friedman, IBM Research, Yorktown Heights, NY

CONTEXT AND STATE OF THE ART

- High speed networking and communication systems for the Internet and cloud computing systems require 100 gigabit-per-second data rates in the next few years. This is nearly a two and a half times increase over today's state-of-the-art systems.
- This paper shows new technology that will enable the next generation of high-speed networking routers using four channels of 25 gigabit per second.

TECHNICAL HIGHLIGHTS

- First 28Gb/s transceiver addressing medium reach, 35dB loss, electrical channel in 32nm SOI CMOS:
- In Paper 19.1, IBM describes the first 28Gb/s transceiver addressing medium reach, 35dB loss, electrical channel in 32nm SOI CMOS that features a source-series terminated driver with 4-tap FFE, a two-stage peaking amplifier with active feedback topology, and a 15-tap DFE. The transceiver consumes 693mW per lane; the per TX/RX port area with PLL contribution amortized is 0.81 mm^2.

APPLICATIONS AND ECONOMIC IMPACT

- It is targeted at OIF, CEI-25G, 32G-FC, and next generation 100GbE systems.
- Successful development of these high-speed technologies at low power and with low silicon area will be critical to the continued evolution of the internet and the future of cloud computing.

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Session 19 Highlights : 20+ Gb/s Wireline Transceivers and Injection-Locked Clocking

[19.5] A Versatile Multi-Modality Serial Link

Paper [19.5] Authors: Y.Tanaka, Y.Hino, Y.Okada, T.Takeda, S.Ohashi1, H.Yamagishi, K.Kawasaki1, A.Hajimiri
Paper [19.5] Affiliation: Sony, Japan, and California Institute of Technology, CA, USA

Subcommittee Chair: Daniel Friedman, IBM Research, Yorktown Heights, NY

CONTEXT AND STATE OF THE ART

- New chip-to-chip and board-to-board interconnects borrowing RF wireless techniques provide higher integration and communication capability for many consumer applications.
- This paper shows how these new interconnect technologies can be used together in the same chips and applications, greatly enhancing the flexibility and applicability of these technologies.

TECHNICAL HIGHLIGHTS

- **A spectrally-efficient multi-carrier interconnect operating at >20Gb/s at millimeter-wave frequencies in the 50GHz to 90GHz range**
- In Paper 19.5, Sony and Caltech describe a versatile multi-modality transceiver that enables data transmission over three types of transmission media: copper wireline, dielectric waveguide, and wireless using the exact same circuit. The fabricated chipset in 40nm low-power logic CMOS technology with impedance transformation-based diplexer enables single-pad frequency multiplexing, and demonstrates data transmission at rates up to 29.6Gb/s. The active footprints including diplexer/de-diplexer are 0.16mm^2 and 0.26mm^2, for the TX and RX chips, respectively; the TX consumes 52mW and the RX 85mW from 1.1V supplies.

APPLICATIONS AND ECONOMIC IMPACT

- Typical applications would be in small form-factor consumer products such as mobile platforms integrating many different functions including video, communications, audio, etc.
- This new class of interconnect technology will eventually enable the consumer industry to become more integrated and reduce the cost of these products while providing the high performance required.

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Session 20 Overview : RF Frequency Generation

RF SUBCOMMITTEE

Session Chair: R. Bogdan Staszewski, Delft University of Technology, Delft, The Netherlands
Session Co-Chair: Taizo Yamawaki, Renesas Mobile, Gunma, Japan

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF

This session covers high-performance RF frequency synthesizers and their building blocks for the single-GHz frequency range. The trend in the frequency synthesis is towards digitization (e.g. all-digital PLL), finer process geometries (e.g., 32nm CMOS), and constructing advanced PLL structures for the direct frequency modulation and cascading of PLLs. Three papers on RF oscillators (VCOs and DCOs) address cellular applications and attempt to minimize phase noise at the lowest possible dissipated power.

- In Paper 20.1, Politecnico di Milano presents a 65nm CMOS wideband RF frequency modulator based on a fractional bang-bang digital-N PLL. The modulator uses digital two-point frequency modulation. The DCO consists of multiple varactor banks with various frequency step sizes, whose values are calibrated by LMS algorithms.
- In Paper 20.2, KAIST presents a 0.13µm CMOS low-jitter cascaded PLL consisting of an integer-N PLL and providing a high 800MHz reference clock to a fractional-N charge-pump RF PLL. The integer-N PLL is a low-power bang-bang PLL structure incorporating dual-pulse ring oscillator.
- In Paper 20.3, Audax Technologies presents a 40nm CMOS all-digital PLL utilizing an injection-locked ring oscillator to replace the conventional inverter-string TDC for the phase detection. The injection locking synchronizes the TDC gain to the DCO frequency to remove the need for calibration. The systematic TDC phase quantization noise is further compensated.
- In Paper 20.4, the University of Pavia presents a new topology of a digitally-controlled oscillator that can seamlessly add PMOS cross-coupled transistors to an N-only cross-coupled transistor oscillator structure to optimize the current consumption to the required phase noise of either GSM or WCDMA standards.
- In Paper 20.5, Delft University presents a new technique for generation of ultra-low-noise RF waveforms, suitable for both handset and base-station cellular applications. The 65nm CMOS oscillator exploits clipping of a resonating waveform followed by restoration of the fundamental harmonic to eliminate effects of active devices on the phase noise.
- In Paper 20.6, Intel presents an RF divider with fractional frequency division ratio, implemented in 32nm CMOS, and using all-digital calibration to suppress spurs. The divider can be used for reconfigurable frequency planning for interferer avoidance.
- In Paper 20.7, the University of Pavia presents a hybrid VCO for cellular phones operating in both class-C and class-B. It combines the benefits of the class-C operation providing low phase noise at low current with the class-B operation ensuring reliable startup.

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Session 20 Highlights : RF Frequency Generation

[20.4] A 36mW/9mW Power Scalable DCO in 55nm CMOS for GSM/WCDMA Frequency Synthesizers

Paper [20.4] Authors: A. Liscidini[1], L. Fanori[1], P. Andreani[2], R. Castello[1]
Paper [20.4] Affiliation: [1]Università di Pavia, Pavia, Italy; [2]Lund University, Lund, Sweden

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF

CONTEXT AND STATE OF THE ART

- Today's cell phones are multiband and multistandard capable. The performance requirements on the radio-frequency signal generator, which accounts for a sizable amount of the power consumption of the whole radio, vary widely across standards and bands. Power can be saved if the performance of the signal generator (digitally controlled oscillator, DCO, in this paper) can be tailored for the different standards.
- Traditionally, this issue has been addressed by either accepting a waste of power in certain standards, or by using two or more different DCOs, which is costly.

TECHNICAL HIGHLIGHTS

- **Reconfigurable DCO breaks power/complexity trade-off for different standards**
- This paper presents a DCO capable of breaking the power/complexity trade-off by reconfiguring the DCO for different standards. The phase-noise figure-of-merit (FOM) of the DCO, which quantifies how low noise the DCO is for a given amount of power, is kept constant at -185dBc/Hz across the standards.The DCO achieves a 4× power reduction when operating at the relaxed 3G performance.
- The DCO has been designed in a 55nm CMOS process, and it covers the 6.5-to-9.0GHz range, with a phase noise of -129dBc/Hz/-135dBc/Hz at 2MHz offset frequency, with a power consumption of 9mW/36mW.

APPLICATIONS AND ECONOMIC IMPACT

- This DCO will enable a longer battery life in smartphones without sacrificing performance.
- Adaptive power vs. performance techniques will be applied across the whole signal chain in future smartphones addressing the LTE standard (4G) as well.

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Session 21 Overview : Analog Techniques

ANALOG SUBCOMMITTEE

Session Chair: Jafar Savoj, Xilinx, San Jose, CA
Session Co-Chair: Chris Mangelsdorf, Analog Devices, Tokyo, Japan

Subcommittee Chair: Bill Redman-White, University of Southampton, UK

Analog technology continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. Entries span the range from a DC reference to a 10GHz filter, from sub-Volt signal processing to 90V ultrasound drivers. New frontiers of precision, speed, and power are established.

- Paper 21.1 by University of Twente presents a 0.3-to-1.2GHz tunable 4th-order BPF that integrates poly-phase g_m-C and N-path techniques to improve the shape and ultimate rejection compared to a simple 4-path filter. The prototype operates from a 1.2V supply and occupies 0.127mm^2 in a 65nm CMOS process.
- Paper 21.2 by Oregon State University presents a 7MHz bandwidth 4th-order Butterworth filter that achieves 61dB SNR 67dB SFDR and operates from a 0.55V supply. A ring-oscillator-based integrator is used as an alternative to conventional OTA-based integrators. The design occupies 0.29mm^2 in a 90nm CMOS process.
- Paper 21.3 by STMicroelectronics presents a GHz range g_m-C low pass filter that occupies 0.01mm^2 in 65nm CMOS and achieves a tunable cut-off frequency of up to 10GHz with a 1.4V supply, more than 3 times higher than the highest cut-off frequency reported to date.
- Paper 21.4 by University of Twente presents a bandgap voltage reference in 0.16μm CMOS that generates a reference voltage of 0.94V with σ=0.84%. Its small active area of 50×50μm^2 enables local generation of reference voltages across the chip.
- Paper 21.5 by University of Michigan presents a crystal oscillator that consumes 79% less power than the lowest reported at the same oscillation frequency. The chip occupies 0.3mm^2 in 0.18μm CMOS technology and maintains frequency performance of the crystal over a wide operating range.
- Paper 21.6 by University of Macau presents a 0.016mm^2 144μW three-stage amplifier in 0.35μm CMOS combining current-buffer Miller compensation and parasitic-pole cancellation that achieves 4.48× improvement in the FOM compared to previously reported amplifiers.
- Paper 21.7 by Università degli Studi di Pavia presents the first integrated linear amplifier suited for ultra-sound harmonic imaging systems that achieves the highest gain-bandwidth product at large output voltage swing with a small static dissipation of 37mW. The design occupies 3.2mm^2 in a BCD6-SOI technology that embeds 5V npn bipolar devices and 0.35μm CMOS with a nominal supply of 3.5V.
- Paper 21.8 by K.U. Leuven presents a 1.2V 24μW fully integrated direct-current feedback instrumentation amplifier with rail-to-rail output that is implemented in 0.13μm CMOS. Feedback resistors are integrated on-chip for a small size of 0.465 mm^2 and low cost.
- Paper 21.9 by Delft University of Technology presents a capacitively coupled instrumentation amplifier has ±30V input CM range and achieves 6.5× better NEF, 64× lower power consumption and 17dB higher CMRR compared to previous art. Implemented in a HV CMOS 0.7μm technology, the design operates from a 3V supply.
- Paper 21.10 by Analog Devices presents a 60V programmable gain amplifier with ±10V differential input range that uses a capacitive gain architecture to achieve high gain and small input-referred noise. This circuit, occupying 3.08mm^2 in a 0.18μm technology with high-voltage devices, can acquire small voltage signals in the presence of very large common-mode voltages.

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Session 21 Highlights : Analog Techniques

[21.2] A 0.55V 61dB-SNR 67dB-SFDR 7MHz 4th-Order Butterworth Filter Using Ring Oscillator Based Integrators in 90nm CMOS

[21.9] A Capacitively Coupled Chopper Instrumentation Amplifier with ± 30V Common Mode Range, 160dB CMRR and 5μV Offset

Paper 21.2 Authors: B. Drost, M. Talegaonkar, and P. K. Hanumolu
Paper 21.2 Affiliation: Oregon State University, Corvallis, OR, USA

Paper 21.9 Authors: Q. Fan, J. H. Huijsing and K. A. A. Makinwa
Paper 21.9 Affiliation: Delft University of Technology, Delft, The Netherlands

Subcommittee Chair: Bill Redman-White, University of Southampton, UK, Analog

CONTEXT AND STATE OF THE ART

- Analog filters and amplifiers are the foundation of any system interfacing to the physical world. The scaling of semiconductor technology, lower supply voltage, and increased performance demands force analog designers to invent new solutions.

TECHNICAL HIGHLIGHTS

- **Analog signal processing moves to temporal domain:**
- Paper 21.2 from Oregon State University removes the traditional integrator of classic analog filters and the limitations of its finite DC gain. Signal integration is moved from the voltage and current domains to the phase domain using controlled oscillators enabling ultra-low-power operation.
- **Highest CMRR instrumentation amplifier:**
- Paper 21.9 from Delft University presents a high-performance chopping instrumentation amplifier capable of detecting a few μV of differential signal buried within ±30V of common-mode variation. It achieves an astonishing Common-Mode Rejection Ratio of 160dB.

APPLICATIONS AND ECONOMIC IMPACT

- Paper 21.2 targets low-voltage applications with stringent requirements for analog filtering. The circuit can operate at voltages close to 0.5V without any degradation in its linearity.
- Paper 21.9 addresses the growing demand for high-precision current sensors for efficient control of battery current during charge and discharge. The high-performance circuit senses the current with minimum power loss even in high-voltage batteries without using any special components.

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Session 22 Overview : Image Sensors

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Co-Chair: David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Session Co-Chair: Robert Johansson, Aptina Imaging, Oslo, Norway

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee

The advancements in CMOS technologies over the last few decades have resulted in image sensors being a ubiquitous part of everyday life. However, new challenges are emerging in this field, requiring sensors with high dynamic range, sub-electron noise performance, simultaneous capturing of high-resolution 3D and 2D color images, and high-speed high-resolution image capture. This session presents recent advancements in response to these challenges.

- In Paper 22.1, Sony describes a single-exposure 5Mpixel, global-shutter CMOS image sensor with an in-pixel storage node. An extended dynamic range of 83dB, a full-well capacity of 67,700e^-, readout noise of 4.8e^-_{rms}, and parasitic light sensitivity (MEM/FD) of less than 100dB are reported.
- In Paper 22.2, Tohoku University presents a global shutter 400(H)×256(V) pixel CMOS image sensor including 128 on-chip memory elements/pixel with a capture speed of 10Mfps in burst operation without cooling, and a readout speed of 7.8kfps in continuous operation.
- In Paper 22.3, Delft University of Technology describes a CMOS imager that combines in-pixel buried-channel source followers, column-level amplifiers, and correlated multiple sampling by column-parallel single-slope ADCs, resulting in 0.7e^- temporal readout noise.
- In Paper 22.4, Stanford University highlights a 256×256 CMOS image sensor with column parallel $\Delta\Sigma$ ADC and built-in single-shot compressed sensing during A/D conversion. Compression ratios of 1/4, 1/8, and 1/16 are achieved at 480, 960 and 1920fps, respectively. Readout noise (351µV_{rms}) and power consumption (96.2mW) are unchanged from 120 to 1920fps.
- In Paper 22.5, NHK Science & Technology Research Laboratories demonstrate a CMOS image sensor with 12b column-parallel pipelined cyclic ADCs and 96 parallel LVDS output ports, resulting in a total output data rate of 51.2Gb/s for the 33Mpixel large-pixel array operated at 120fps. The sensor read noise is 6.1e^- at 0.96 gain and 3.9e^- at 6.8 gain in the readout chain, at a power consumption of 2.32W and 2.54W, respectively. An input-referred ADC noise of 148.5µV_{rms} is reported.
- In Paper 22.6, Samsung Electronics presents a CMOS image sensor employing an extended counting ADC with 14b of resolution and 12.8µs conversion time. A full-frame still-shot mode with 6.5fps, 14b resolution, and 24Mpixel operation, as well as a video mode with 30fps,10b resolution, and 6Mpixel operation are supported. The reported full-frame power consumption is 1.25W, and the read noise is 420µV_{rms}.
- In Paper 22.7, Samsung Electronics introduces a 1.5Mpixel RGBZ FSI CMOS image sensor with 1920(H) ×720(V) 2.25×2.25µm^2 2.5T RGB pixels and 480(H)×360(V) 2.25×9.0µm^2 5T single-tap Z pixels. The Z-pixels are organized in horizontal rows in-between the RGB color pixel rows. A range error of 0.5 to 2.5% from 1 to 7m with a 10ms integration time and modulation frequency of 20MHz is reported.
- In Paper 22.8, Fondazione Bruno Kessler reports a QVGA CMOS image sensor with buried-channel photo-demodulator pixels for time-of-flight range imaging. The sensor has a pixel pitch of 14µm with a fill-factor of 48%, allowing a maximum frame rate of 70 3D fps. Dynamic range extension using multiple-exposure times is demonstrated.
- In Paper 22.9, Samsung Advanced Institute of Technology highlights a RGBZ CMOS image sensor based on standard pinned photodiodes binned together in time-of-flight mode, generating both a 1920(H)×1080(V) color image as well as a 480(H)×270(V) range image. The pixel demodulates a 20MHz time-of-flight signal with 52.8% contrast. The range error is smaller than 38mm between 0.75 and 4.0m.

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Session 22 Highlights : Image Sensors

[22.2] A Global-Shutter CMOS Image Sensor With Read-Out Speed of 1Tpixel/s Burst and 780Mpixel/s Continuous

[22.7] A 1.5Mpixel RGBZ CMOS Image Sensor for Simultaneous Color and Range Image Capture

Paper 22.2 Authors: Y. Tochigi, K. Hanzawa, Y. Kato, R. Kuroda, Hi Mutoh, R. Hirose, H. Tominaga, K. Takubo, Y.Kondo, and S. Sugawa
Paper 22.2 Affiliation: Tohoku University, Sendai, Japan; Link Research, Odawara, Japan; Shimadzu, Kyoto, Japan
Paper 22.7 Authors: Wonjoo Kim, Y.M. Wang, I. Ovsiannikov, S. Lee, Y.D. Park, C.H. Chung, and E.R. Fossum
Paper 22.7 Affiliation: Samsung Electronics, Hwaseong, Korea; Samsung Semiconductor, Pasadena, CA

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany, IMMD Subcommittee

CONTEXT AND STATE OF THE ART

- Very high-speed image capture is important for specific scientific applications. Typically, 100-to-200 consecutive frames at 100-to-200kpixel resolution are captured at a burst rate of around 10MHz, and then read out at lower speed. Most current implementations use CCD pixels, each linked to storage elements.
- 3D time-of-flight imaging is an emerging technology in gaming, gesture control and virtual reality. However, existing systems are not able to simultaneously capture depth maps and 2D color images.

TECHNICAL HIGHLIGHTS

- **CMOS image sensor with high-speed burst capture rate of 10Mframes/s and burst readout rate of 1Tpixels/s:**
- In Paper 22.2, Tohoku University, Link Research and Shimadzu, present a CMOS imager with 400×256 pixels that achieves a burst capture rate of 10Mfps and a burst readout rate of 1Tpixel/s using 40 parallel outputs, and has a memory for 128 images. Alternatively the sensor can be operated at half the resolution using the memory for 256 images, with a burst capture rate of 20Mfps.
- **Real-time color and 3D imaging over 1-to-7m distances:**
- In Paper 22.7 Samsung Electronics and Samsung Semiconductor present a 1.5Mpixel image sensor with 1920(H)×720(V) 2.25×2.25μm^2 2.5T RGB pixels interlaced with 480(H)×360(V) 2.25×9μm^2 5T single-tap Z pixels. The sensor can capture 3D images over a 1-to-7m distance range with a range error between 0.5 and 2.5%. Simultaneous capture of 3D and color images is reported.

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APPLICATIONS AND ECONOMIC IMPACT

- The very-high-speed CMOS imager in Paper 22.2 is intended to support research that requires the analysis of very fast transient events, e.g. the initiation and propagation of lightning, temporal analysis of deformation of objects by impact, shock waves, etc.
- Real-time color and 3D imaging, as in Paper 22.7, could potentially be used in many consumer applications such as gaming, gesture control, virtual reality, etc.

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Session 23 Overview : Advances in Heterogeneous Integration

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: Tadahiro Kuroda, Keio University, Yokohama, Japan
Session Co-Chair: David Ruffieux, CSEM, Neuchâtel, Switzerland

Subcommittee Chair: Siva Narendra, Portland, OR, Technology Directions Subcommittee

This session presents recent advances in heterogeneous integration in various domains and applications: Ni-Fe magnetic coils on silicon interposer combined to UDSM CMOS to implement compact regulators for dynamic voltage and frequency scaling (DVFS); an autonomous, modular advanced sensor platform based on multiple CMOS dies and battery stacking; GaN-based HFET integration on sapphire combined to a 3D microwave coupler for power devices; monolithic stacking of resistive RAM (RRAM) onto standard CMOS for FPGAs.

- In Paper 23.1, Columbia University and IBM presents a voltage regulator for DVFS integrated on a 45nm SOI process and flip-chipped onto a silicon interposer comprised of coupled magnetic-core power inductors. When supplied at 1.8V, the regulator switches at a frequency of 75MHz and reaches a peak efficiency of 75% when delivering 3A at an output voltage of 1.1V.
- In Paper 23.2, the University of Michigan presents a general-purpose, sensor node platform with a stacked heterogeneous multi-layer structure. The platform comprises 3 I^2C-linked CMOS ICs in 0.18μm, 0.13μm and 65nm, a 0.6μAhr thin-film battery, and a decoupling capacitor layer achieving a total thickness of only 0.4mm in a volume of $1mm^3$. The system features vision and temperature sensors, a 40nW energy harvesting solar cell, an optical communication unit, two 32b processors, 3kB and 16kB SRAMs, and a power-management unit. The sensor node platform achieves a standby power of 11nW with an active timer.
- In Paper 23.3, Panasonic presents a compact $2.5\times5mm^2$ DC-isolated direct gate driver IC with a 5.8GHz electromagnetic resonance coupler and AlGaN/GaN HFETs on sapphire for power-switching applications. This method of coupling eases integration and eliminates other bulky components such as opto-couplers or DC isolators.
- In Paper 23.4, Stanford University demonstrates the combination of a 0.18μm CMOS FPGA with monolithically stacked 21kb configuration non-volatile RRAM. As examples, 4-bit adders and LFSRs are mapped onto the FPGA containing 289 logic tiles and are operating at up to 250MHz.

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Session 23 Highlights : Advances in Heterogeneous Integration

[23.2] A Modular 1mm^3 Die-Stacked Sensing Platform With Optical Communication and Multi-Modal Energy Harvesting

Paper Authors: *Y. Lee, G. Kim, S. Bang, Y. Kim, I. Lee, P. Dutta, D. Sylvester, D. Blaauw*
Paper Affiliation: *University of Michigan, Ann Arbor, MI*

Subcommittee Chair: *Siva Narendra, Tyfone, Portland, OR*

CONTEXT AND STATE OF THE ART

- Today's commercial wireless sensor networks are cubic-cm-sized and suffer from limited autonomy consuming several 10's of mW.
- Miniaturization and power reduction effort initiated a couple of years ago to achieve a 1mm^3 node.
- Smart dust requires a cubic mm-scale, wireless sensor node with perpetual energy harvesting. Conventional cubic mm-scale microsystems, however, cannot be reprogrammed nor designed to enable use in multiple application domains.

TECHNICAL HIGHLIGHTS

- **First optically reconfigurable sensor node with complete power-management unit, power-on reset, as well as brown-out detection for CPU and memory integrity preservation.**
- In Paper 23.2, University of Michigan describes a fully autonomous solution with only 11nW standby power. A thin-film battery is combined with energy harvesting from multiple sources (solar, thermo-electric generator) to achieve continuous operation without maintenance.
- 32-bit processors, power management unit, imager, temperature sensor, battery, and solar cells are stacked in 1mm^3, with all stacked layers communicating with ultra-low-power inter-layer connections using an I^{2}C interface (144pJ/bit).
- Global optical communication controls the status of all nodes and entails programmability.

APPLICATIONS AND ECONOMIC IMPACT

- This design has the potential to realize battery-less complex general-purpose multi-functional sensor nodes.
- It paves the way towards ubiquitous computing with embedded processing capability.
- Ubiquity of such sensor nodes will further enrich human life.

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Session 24 Overview : 10GBASE-T and Optical Front Ends

WIRELINE SUBCOMMITTEE

Session Chair: Miki Moyal, Intel, Israel
Session Co-Chair: Chewnpu Jou, TSMC, Hsinchu

Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee

Consumer expectations for more Internet bandwidth require improvements in electrical transceivers to increase throughput on data-center legacy channels and new optical transceivers to make fiber-to-the-home a reality. 10GBase-T offers a 10× increase in capacity over existing twisted-pair cables. The first two papers in the session offer low-power and low-distortion solutions for the 4-2 wire interface. Fiber is increasingly displacing cable and twisted pair to the home. 10G-EPON, enabled by a burst-mode LDD and TIA/LIA, provides the highest data rates to the home. The challenges of achieving low average power and fast DC restoration are cleverly addressed in the session's next two papers. In the session's final paper, new techniques for achieving ultra-low power in VCSEL-based links are described.

- In Paper 24.1, Applied Micro describes a standards-compliant 10GBase-T transceiver implemented in 40nm triple-gate CMOS technology. A single DAC shared by the line driver and echo canceller achieves greater than 68dB EC SFDR across a 400MHz bandwidth. The AFE, which also includes a receiver consisting of a PGA and time-interleaved 10b and 800MSample/s SHA-less pipeline ADC, dissipates <2W power from 0.9/1.2/2.5V supplies, and occupies a die area of $17mm^2$.
- In Paper 24.2, Aquantia describes a 10GBASE-T transmitter, using a current-mirroring amplifier to perform a first-order echo cancellation. The transmitter linearity is >57dBc, while the residual linear echo and distortion are -28dBc and 76dBc, respectively. The transmitter is implemented in 40nm CMOS, occupies $0.25mm^2$, and consumes 200mW.
- In Paper 24.3, NTT presents a power-saving burst-mode LDD for 10G-EPON applications implemented in a 0.18µm SiGe BiCMOS process. It consumes 66mW in LD-off state and 1116mW in LD-on state from 3.3V/5V supplies. A 94% power reduction is facilitated by a fast 16ns turn-on time. The die size is $1.9×3.3mm^2$.
- In Paper 24.4, imec/Ghent University presents a 10Gb/s burst-mode TIA and limiting amplifier chipset in 0.13µm SiGe BiCMOS. The optical dynamic range for an APD-TIA spans from -27.3dBm to -1.8dBm at a BER of 10^{-10}. The three-step gain-switching TIA settles within 8ns, and the burst-mode limiting amplifier takes 73ns. Power consumption for the $1.3mm^2$ TIA and $1.52mm^2$ LA are 400mW from 2.5V and 430mW from 2.2V, respectively.
- In Paper 24.5, IBM describes two circuits in 90nm CMOS for converting the output of a 25Gb/s optical link. A CML RX achieves a 22% UI eye opening (BER=10^{-10}) at 25Gb/s and a CMOS inverter RX at 15Gb/s. The full link with CMOS inverter RX achieves a power efficiency of 1.37pJ/bit from 1.2/1.6V supplies; core RX area is $.0038 mm^2$.

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Session 25 Overview : Non-Volatile Memory Solutions

MEMORY SUBCOMMITTEE

Session Chair: Tadaaki Yamauchi, Renesas Electronics, Hyogo, Japan
Session Co-Chair: Satoru Hanzawa, Hitachi, Tokyo, Japan

Subcommittee Chair: Kevin Zhang, Intel, Hillsboro, OR, Memory

Strong market demands drive a diverse range of non-volatile memory technologies that show continued increases in density, reliability, and performance. This year, the leading-edge process node for NAND Flash is scaled down to the sub-20nm regime, enabling the world's highest density of 128Gb. To maintain high reliability without performance degradation, solid-state-drive (SSD) controllers are being used for NAND Flash in advanced process nodes. Embedded Flash is addressing the automotive industry that requires high reliability. Finally, emerging memories such as Resistive RAM (ReRAM) devices are being pursued for future applications.

- In Paper 25.1, Toshiba reports a 64Gb NAND Flash memory with a single-array architecture suitable for micro-SD card with minimized performance degradation, supporting 15MB/s write throughput and 400Mb/s/pin read throughput.
- In Paper 25.2, University of Tokyo describes a solution for solid-state disk (SSD) applications to both extend data lifetime by 10× and reduce write errors 76% without performance degradation.
- In Paper 25.3, KAIST reports the highest BCH-decoding throughput, supporting 6.4Gb/s bandwidth with minimized hardware resources.
- In Paper 25.4,Infineon describes an embedded Flash memory with the fastest read latency of 11ns and 2.9GB/s read throughput for automotive applications.
- In Paper 25.5, Samsung reports a 64Gb NAND Flash memory with various schemes to reduce the cell V_{th} variations in a cutting-edge sub-20nm process technology and the highest read throughput reported, as fast as 533Mb/s.
- In Paper 25.6, Panasonic describes an 8Mb multi-layered cross-point ReRAM macro using a bidirectional diode developed in 0.18µm process. The fast switching performance of TaO achieves 433MB/s write throughput. These features show the feasibility of high-density and high-throughput ReRAM.
- In Paper 25.7, National Tsing Hua University reports the first embedded ReRAM macro using the unipolar write behavior of ReRAM devices. A reverse-read cell structure and a newly developed body-drain-driven CSA achieves a 45ns macro access time at a 0.5V V_{DD}.
- In Paper 25.8, Sandisk presents the largest monolithic NAND Flash memory density of 128Gb and fast write throughput of 18MB/s using 3-bit per cell structure, achieving a read throughput of 400Mb/s.

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Session 25 Highlights : Non-Volatile Memory Solutions

[25.8] 128Gb 3b/Cell NAND Flash Memory in 19nm Technology With 18MB/s Write Rate and 400Mb/s Toggle Mode

Paper Authors: Y. Li, S. Lee, K. Oowada, H. Nguyen, Q. Nguyen, N. Mokhlesi, C. Hsu, J. Li, V. Ramachandra, T. Kamei, M. Higashitani, T. Pham, M. Honma2, Y. Watanabe2, K. Ino2, B. Le, B. Woo, K. Htoo, T-Y. Tseng, L. Pham, F. Tsai, K-H. Kim, Y-C. Chen, M. She, J. Yuh, A. Chu,C. Chen, R. Puri, H-S. Lin, Y-F. Chen, W. Mak, J. Huynh, J. Chan, M. Watanabe, D. Yang,G. Shah, P. Souriraj, D. Tadepalli, S. Tenugu, R. Gao, V. Popuri, B. Azarbayjani, R. Madpur,J. Lan, E. Yero, F. Pan, P. Hong, J. Kang, F. Moogat, Y. Fong, R. Cernea, S. Huynh, C. Trinh, M. Mofidi, R. Shrivastava, K. Quader
Paper Affiliation: Sandisk and Toshiba

Subcommittee Chair: Kevin Zhang, Intel, OR, Memory Subcommittee

CONTEXT AND STATE OF THE ART

- The current largest NAND Flash based on sub 30nm node technology has reached 64Gb density with multi-bit per cell technology. The highest write bandwidth has reached 7MB/s. Consumer electronics with expanded application continue to drive up the density in NAND flash memory.

TECHNICAL HIGHLIGHTS

- **Highest-ever density NAND Flash memory (and fastest 3b/cell write performance of 18MB/s)**
- In Paper 25.8, Sandisk presents the largest monolithic NAND Flash memory density of 128Gb and fast write throughput of 18MB/s using 3-bit per cell structure, achieving a read throughput of 400Mb/s.

APPLICATIONS AND ECONOMIC IMPACT

- This work is strong proof that 3bit/cell Flash memory technology has reached the same level of performance as 1 or 2-bit per cell.
- This technology enables applications requiring higher density and lower-cost flash memory, such as tablets, smart phones, and solid-state drives (SSD).

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Session 26 Overview : Short-Range Wireless Transceivers

WIRELESS SUBCOMMITTEE

Session Chair: Ranjit Gharpurey, University of Texas at Austin, Austin, TX
Session Co-Chair: Woogeun Rhee, Tsinghua University, Beijing, China

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless Subcommittee

Emerging applications for short-range wireless systems require transceivers that are capable of energy-efficient performance, while optimizing data rates and battery life. Interference robustness is also a requirement in several wireless systems. In this session, transceivers that address such applications including high-data-rate and energy-optimized ultra-wide band (UWB) systems and ultra-low power transceivers for sensor applications are presented.

- In Paper 26.1, Sony describes the first SoC for TransferJet™, which integrates PHY including an RF transceiver, achieves a sensitivity of -70dBm at a data rate of 522Mb/s and an effective throughput of 357Mb/s, consuming 16.2mm^2 in 90nm CMOS.
- In Paper 26.2, Keio University presents a 2Gb/s UWB 90nm CMOS transceiver with a high energy efficiency of 75pJ/bit, employs a new carrier recovery scheme and reduces the area by 43% (TX/RX = 0.44/0.81mm^2) and the power by 20%, compared to the conventional Costas loop.
- In Paper 26.3, the National University of Singapore describes a 10pJ/pulse/ch UWB beamforming transmitter with 1° phase resolution utilizing a Vernier delay line calibrated by a Delta-Sigma DLL; this device uses 7.2mm^2 in 0.13µm CMOS.
- In Paper 26.4, KAIST presents a robust wake-up radio for Electronic Toll-Collection Systems (ETCS) implemented in 0.13µm CMOS with an integrated low-power delay-based bandpass filter, significantly reducing the possibility of false wake-ups.
- In Paper 26.5, imec describes a 2.7nJ/b 50kb/s-to-2Mb/s transmitter that supports four short-range wireless standards (IEEE802.15.4/4g/6 and Bluetooth LE), implemented in 90nm CMOS.
- In Paper 26.6, imec presents a complete IR-UWB system using 2mm^2 of 90nm CMOS, which has a link budget of 75dB and a data rate of 0.85Mb/s for a 5-meter wireless link.
- In Paper 26.7, University of Catania describes a crystal-less 5Mb/s RF transceiver for RF-powered WSN nodes that supports a 915MHz FSK downlink and a 2.45GHz OOK uplink; occupying 1.4 x 1.1 mm^2 and implemented in 90nm CMOS. A PLL-based architecture allows TX carrier synthesis from the incoming RX frequency, thus avoiding the use of a local quartz crystal oscillator.
- In Paper 26.8, imec presents a 120 W-RX/900 W-TX envelope-detection transceiver in 90nm CMOS that employs a novel interference-rejection technique that improves the in-band selectivity by 24.5dB without compromising simplicity or power efficiency. The TX/RX occupies 0.71/1.27mm^2.

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Session 26 Highlights : Short-Range Wireless Transceivers

[26.3] 3-to-5GHz 4-channel UWB Beamforming Transmitter With 1° Phase Resolution Through Calibrated Vernier Delay Line in 0.13µm CMOS.

Paper Authors: L.Wang, Y.Xin Guo, Y.Lian, C.Huat Heng
Paper Affiliation: National University of Singapore, Singapore

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA, Wireless

CONTEXT AND STATE OF THE ART

- In the mm-Wave range, beamforming is used to obtain high power through spatial combining.
- So far, beamforming implemented in the RF or LO paths has been based on phase shifting and vector modulation.

TECHNICAL HIGHLIGHTS

- **First beamforming transmitter with 1° phase resolution**:
- A 4-channel UWB beamforming transmitter based on a Vernier Delay Line is described.
- Realized in 0.13µm CMOS, 1° phase resolution has been obtained in the 3-to-5GHz Band, with very low power consumption (<12mW) and drastically-reduced area (10 times smaller).

APPLICATIONS AND ECONOMIC IMPACT

- This CMOS beamforming transmitter can significantly reduce the cost of medical imaging and create higher resolution pictures.
- The beamformer can also drastically reduce the cost of ownership for radar systems.

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Session 27 Overview : Data Converter Techniques

DATA CONVERTERS SUBCOMMITTEE

Session Chair: Dieter Draxelmayr, Infineon Technologies, Villach, Austria
Session Co-Chair: Takahiro Miki, Renesas Electronics, Itami, Japan

Subcommittee Chair: Venu Gopinathan, Texas Instruments, Bangalore, India, Data Converters

This session presents the latest developments in a variety of data conversion fields. The session opens with a current-steering RF DAC. Next, a new technique for building low-power switched-capacitor circuits is introduced, which is demonstrated with a pipelined converter. A time-to-digital converter based on a switched-ring oscillator enables high-resolution time measurement, while being robust against process imperfections such as leakage. This is followed by four SAR data converter papers. Techniques enabling noise shaping and enhanced reconfigurability are discussed. The session concludes with a low-power 2-step pipelined converter.

- In Paper 27.1, Analog Devices present a 14b 3/6GHz current-steering RF DAC in 0.18µm CMOS. Using different switch-driving modes, several frequency bands are covered. A 66dB ACLR at 2.9GHz is demonstrated.
- In Paper 27.2, Oregon State University introduces a concept for operating switched-capacitor circuits at low power. The concept is demonstrated using a 15b 20MHz pipelined converter designed in 0.18µm CMOS, running at an efficiency of 45fJ/conversion-step.
- In Paper 27.3, National Chiao Tung University shows a 10b 200MS/s pipelined converter implemented in 65nm CMOS that consumes 5.37mW. The low power consumption is achieved using a dual-path concept. Two amplifiers per pipelined stage allow individual optimization, resulting in an overall improved power efficiency.
- In Paper 27.4, Oregon State University demonstrates a 13b 315fs_{rms} time-to-digital converter based on a switched ring oscillator that achieves 1st-order noise shaping. This architecture, implemented in 90nm CMOS, overcomes sensitivity to leakage, which was inherent to previous gated ring oscillator TDC designs.
- In Paper 27.5, imec and Renesas demonstrate an 11b 250MS/s converter designed in 40nm CMOS, whoch consumes 1.7mW, yielding an energy efficiency of less than 10fJ/conversion-step. Low-power operation is achieved with a 2× time-interleaved pipelined SAR converter using dynamic residue amplification.
- In Paper 27.6, the University of Michigan introduces the concept of noise shaping into a SAR converter implemented in 65nm CMOS. This is accomplished with an additional memory capacitor for the conversion residue, which is used during the subsequent conversion cycle. An SNDR of 62dB in 11MHz bandwidth at 4× oversampling is achieved.
- In Paper 27.7, imec and Renesas demonstrate a 0-to-80MS/s current-integrating SAR converter in 40nm-LP CMOS. The input information steers a programmable transconductor feeding a charge-domain SAR. Parametric amplification relaxes the comparator requirements. This yields 70dB dynamic range.
- In Paper 27.8, Holst Centre/imec exploits an additional degree of freedom in combining a reconfigurable capacitor array with a noise-adjustable comparator. Together with an optional redundant mode, this yields a 7-to-10b 0-to-40MS/s 6.5-to-16fJ/conversion-step converter in 90nm CMOS
- In Paper 27.9, Oregon State University demonstrates a pipelined converter with an energy efficiency of 31.3fJ/conversion-step. This is achieved with a 2-step approach at the residue amplification stage. The ADC is implemented in 0.13µm CMOS and achieves 70.4dB SNDR at 30MS/s.

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Session 27 Highlights : Data Converter Techniques

[27.2] Ring Amplifiers for Switched-Capacitor Circuits

[27.3] A 5.37mW 10b 200MS/s Dual-Path Pipelined ADC

Paper 27.2 Authors: B. Hershberg[1], S. Weaver[1], K. Sobue[2], S. Takeuchi[2], K. Hamashita[2], U. Moon[1]
Paper 27.2 Affiliation: [1]Oregon State University, Corvallis, OR, [2]Asahi Kasei Microdevices, Atsugi, Japan

Paper 27.3 Authors: *Y. Chai, J. Wu*
Paper 27.3 Affiliation: National Chiao-Tung University, Hsinchu, Taiwan

Subcommittee Chair: Venu Gopinathan, Texas Instruments, Bangalore, India

CONTEXT AND STATE OF THE ART

- After more than 40 years of integrated circuits, improvements in circuit blocks as basic as opamps have been few and far between. This year, two papers show significant improvements in opamp design or the way opamps are used in a pipeline ADC.
- Amplification is increasingly an efficiency bottleneck in many mixed-signal applications. Specifically in ADC design, the opamp is almost always the dominant component of power dissipation and the performance limiter. Paper 27.2 shows a very power-efficient opamp design, whereas Paper 27.3 significantly increases the performance obtained from the opamps.

TECHNICAL HIGHLIGHTS

- **Revolutionary opamp architecture lowers power:**
- In Paper 27.2 Oregon State University and Asahi Kasei Microdevices present a 20MHz, 15b pipeline ADC using ring amplifiers and split-CLS achieves 76.8dB SNDR and 95.4dB SFDR while using 5.1mW, achieving an FOM of 45fJ/conversion-step.
- **Pipelined coarse/fine opamp extends low-power/high-performance tradeoff:**
- In Paper 27.3, National Chiao-Tung University reports that pipelining the residue-amplification using a coarse and a fine amplifier in a pipeline ADC achieves 56.7dB SNDR at 200MS/s while consuming only 5.37mW from a 1V supply.

APPLICATIONS AND ECONOMIC IMPACT

- These two papers break the voltage and power bottleneck imposed on data converters by the ongoing march of miniaturization and expanding functionality of handheld devices.

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Session 28 Overview : Adaptive and Low Power Circuits

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: Michael Phan, Qualcomm Inc., Raleigh, NC
Session Co-Chair: Masaya Sumita, Panasonic, Osaka, Japan

Subcommittee Chair: Tzi-Dar Chiueh, National Chip Implementation Center, Hsinchu, Taiwan, Energy-Efficient Digital

Next-generation low-power applications such as subthreshold-operating processors, energy scavenging, visual recognition and networking processors require new technologies and circuit techniques to achieve the lowest energy-per-operation. These applications are driving new techniques for a reliable on-die timing-error detection and correction for low-voltage operation such as adaptive techniques, architecture and logic. Energy-efficient systems must be optimized to maximize the utility of low-voltage and low-activity periods while also maintaining low-energy operation and high throughput during active modes to meet performance targets. The papers selected for this session highlight technology enhancements, novel circuit techniques, and system designs targeting these goals.

- In Paper 28.1, the University of Michigan describes a 4.5Tb/s 3.4Tb/s/W 64×64 switch fabric with self-updating least-recently-granted priority and quality-of-service arbitration in 45nm CMOS. This single stage 64×64 switch fabric with 128b data bus is fully functional down to 550mV with a measured peak efficiency of 7.4Tb/s/W at 0.6V.
- In Paper 28.2, National Taiwan University describes a 1.0 TOPS/W 36-core neocortical computing processor with 2.3 Tb/s Kautz NoC for universal visual recognition in 65nm CMOS technology operating at 1.0V. It is the first real-time universal visual-recognition neocortical computing processor, achieving 151Tb/s/W power efficiencies at 250MHz operating frequency and 205mW in average power.
- In Paper 28.3, the University of Siena describes a condition push-pull pulsed latch with 726fJ·ps energy-delay product in 65nm CMOS. This pulsed latch exhibits sub-FO4 performance up to 64 fan-out and achieves 2.3× (1.3×) lower ED3 (ED) product.
- In Paper 28.4, the University of Paderborn describes a 65nm CMOS 200mV 32b subthreshold processor with adaptive supply voltage control. It achieves minimum energy-per-cycle of 9.94pJ at 325mV and 133kHz.
- In Paper 28.5, the Semiconductor Technology Academic Research Center describes a 13% power reduction in a 16b integer unit in 40nm CMOS by adaptive power supply voltage control with parity-based error prediction and detection and fully integrated digital LDO. This 16b 20-core unit achieves 100μW power consumption at 9MHz operating frequency.
- In Paper 28.6, the University of Michigan describes an architecture-independent approach to timing-error detection and correction. This design archives 60% energy reduction by reducing timing margins and it also avoids the hold-time issues in prior Razor-style designs.
- In Paper 28.7, Catholic University Louvain describes a 25MHz 7μW/MHz ultra-low-voltage microcontroller SoC in 65nm LP/GP CMOS for low-carbon wireless sensor nodes. It achieves 7μW/MHz power consumption in active mode using an adaptive internal power supply ranging from 0.32-to-0.48V, 1.5μW sleep power and at 0.66mm^2 in area.
- In Paper 28.8, Oregon State University describes a 530mV 10-lane SIMD processor with variation resiliency in 45nm-SOI. This design exhibits 16.5pJ/operation and operates at 144MHz clock frequency with 530mV power supply and 19.3mW power consumption.

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Session 28 Highlights : Adaptive and Low Power Circuits

[28.4] A 200 mV 32b Subthreshold Processor With Adaptive Supply Voltage Control

[28.6] Bubble Razor: An Architecture-Independent Approach to Timing-Error Detection and Correction

Paper 28.4 Authors: Sven Luetkemeier[1], Mario Porrmann[1], Thorsten Jungeblut[2], Ulrich Rueckert[2]
Paper 28.4 Affiliation: [1]University of Paderborn, Paderborn, Germany [2]Bielefeld University, Bielefeld, Germany
Paper 28.6 Authors: Matthew Fojtik, David Fick, Yejoong Kim, Nathaniel Pinckney, David Blaauw, Dennis Sylvester
Paper 28.6 Affiliation: University of Michigan, Ann Arbor, MI

Subcommittee Chair: Tzi-Dar Chiueh, National Chip Implementation Center, Hsinchu, Taiwan, Energy-Efficient Digital

CONTEXT AND STATE OF THE ART

- Energy-efficiency in integrated circuits is becoming more crucial as all devices are going green.
- Increasingly, circuits operate in the near-threshold and subthreshold regions to save dynamic and also leakage power.

TECHNICAL HIGHLIGHTS

- **Subthreshold 32b processor operates down to 200mV in 65nm CMOS**:
- Paper 28.4 describes a processor that achieves 9.94pJ per-cycle at its lowest energy point of 325mV and 133kHz operation.
- **Bubble Razor – an architecture-independent approach to timing-error detection and correction**:
- Paper 28.6 presents a technique that avoids hold-time issues and enables large timing speculation windows, which reduces margin, reducing energy by 60% relative to previous design styles.

APPLICATIONS AND ECONOMIC IMPACT

- “Green” energy-efficient digital circuits combined with the new algorithm and architecture technologies promise a practical and sustainable system for comfortable human life.

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ISSCC 2012
TRENDS

Analog Subcommittee – 2012 Trends

Subcommittee Chair: Bill Redman-White, NXP/Southhampton University, UK

Analog circuits continue to play a key role in modern technology. For example, analog signal amplification is fundamental to interfacing with antennas, microphones, speakers, headphones, and image sensors. Analog circuits are bridges between the digital world and the analog real world. Just like the bridges in our roads, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, digital circuits such as microprocessors drive the market; so semiconductor technology has been optimized relentlessly over the last 40 years to reduce the size, cost, and power consumption of digital circuits. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle has decreased and the variation observed in their analog performance has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by medical, automotive, lighting, and industrial applications. Other applications dictate full integration of analog and digital circuits together in our most modern digital semiconductor technologies. In these applications, advances in analog interfaces are needed to realize the digital processing's full potential. For example, mobile systems with multi-core digital processors routinely have their battery life limited by the power consumption of analog audio playback circuits. Here, analog circuits have embedded within them digital signal-processing circuits that help overcome analog-circuit limitations, and analog circuits are being embedded within digital ICs to monitor their performance and manage their power consumption. Hence, the distinction between analog and digital circuit design is blurring, spawning new advances in the state-of-the-art for both.

The efficient control, storage, and distribution of energy are worldwide challenges, and an increasing focus of analog circuits research. Whereas the manipulation and storage of information is efficiently performed digitally, the manipulation and storage of energy must fundamentally be performed with analog systems. As a result, key technologies for power management are predominantly analog. For example, there is much activity in architectures for DC-DC converters for lighting applications, converters with multiple output voltages, inductor-less, and fully integrated power converters. There is an increasing presence of circuits that harvest energy from ambient light, heat, and motion, store it, and convert it into usable voltages and currents. Efforts are to simultaneously increase the energy efficiency and power density (power-handling vs. size) of power management circuits as shown in the attached trend chart. Future power management systems will startup from sources with voltages well below 100 mV. Similarly, the power consumption of analog circuits is aggressively scaled down in order to enable these low power systems. Micropower instrumentation amplifiers, oscillators, and very efficient audio power amplifiers are examples of this trend. Together, these technologies will permit devices to be indefinitely powered from sustainable sources, opening the door to ubiquitous sensing, environmental monitoring, and medical applications.

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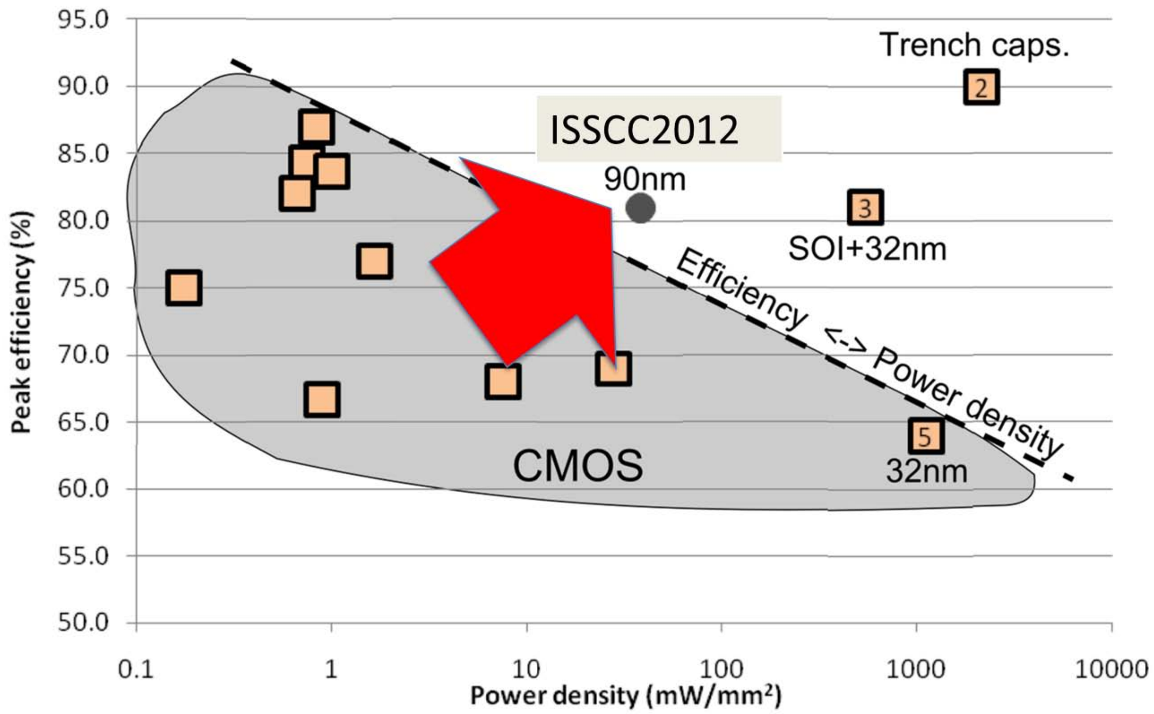

[Session 5: Audio and Power Converters, paper 5.4]

The graph shows an example of trends in integrated power converters: year after year, more is integrated in standard CMOS technologies, optimizing the efficiency versus power density. Also this year the trends are evident at ISSCC in the shift of the boundary to higher performances, as is indicated by the arrow.

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Data Converters – 2012 Trends

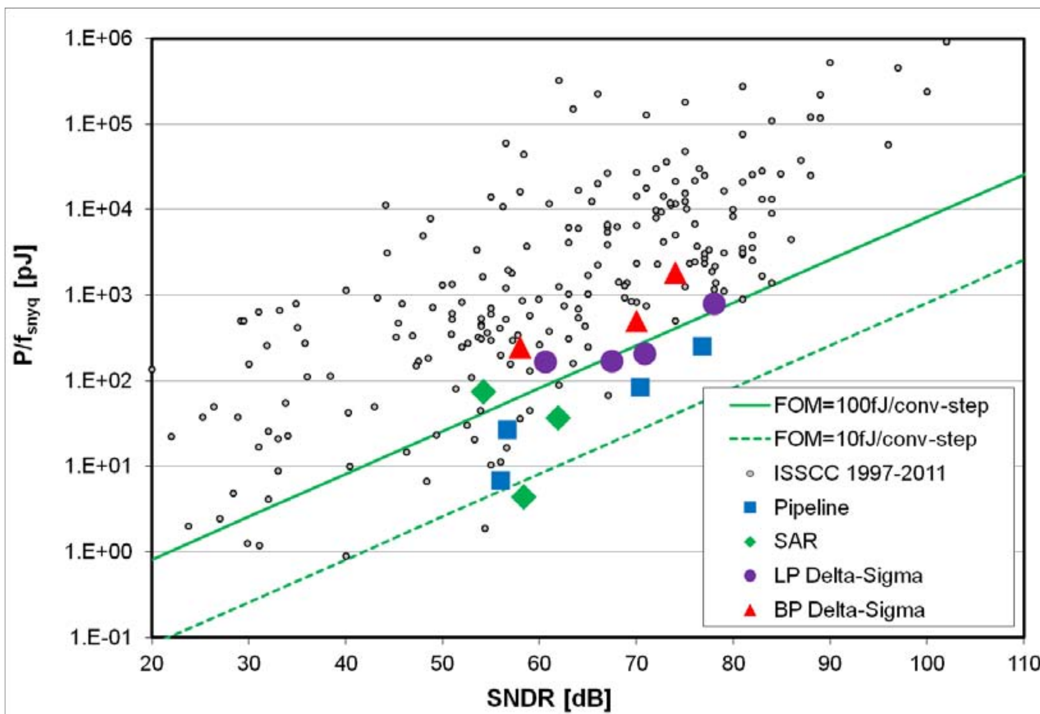
Author: Venu Gopinathan, Texas Instruments, Bangalore, India

The march of progress in converter designs involves exploiting the inherent tradeoffs between signal-to-noise ratio, bandwidth and sampling frequencies, and power efficiency, especially when all need to be improved. The latest designs designs sit at better points in the design space, as evidenced by this year's papers at ISSCC.

The first chart shows power efficiency in terms of power-dissipation-per-Hertz of Nyquist frequency versus signal-to-noise ratio. Since higher signal-to-noise ratio requires more power, constant figure-of-merit trend-lines in the plot are proportional with SNDR. The small dots in the graph are previously published ISSCC papers, whereas the 2012 contributions are indicated by the large triangles, squares, and circles. As the plot indicates, the ISSCC 2012 data converters are once again extending the state-of-the-art.

The second chart shows bandwidth versus SNDR. Generally, bandwidth is lower at higher SNDRs, as is indicated by the trend-lines in the chart. The trend-lines show the equivalence of a constant clock-jitter. Also on this chart, bandpass delta-sigma converters are especially pushing the state-of-the-art.

The last chart shows the figure-of-merit versus Nyquist-bandwidth. At low frequencies the figure-of-merit is optimal (low FoM is better), but as the chart shows, at higher frequencies the FoM is deteriorating. This is primarily caused by the speed limitation of presently available technology. The 2012 designs show good progress, with a SAR pushing the state-of-the-art at lower frequencies and a pipeline design breaking the barrier at higher frequencies.



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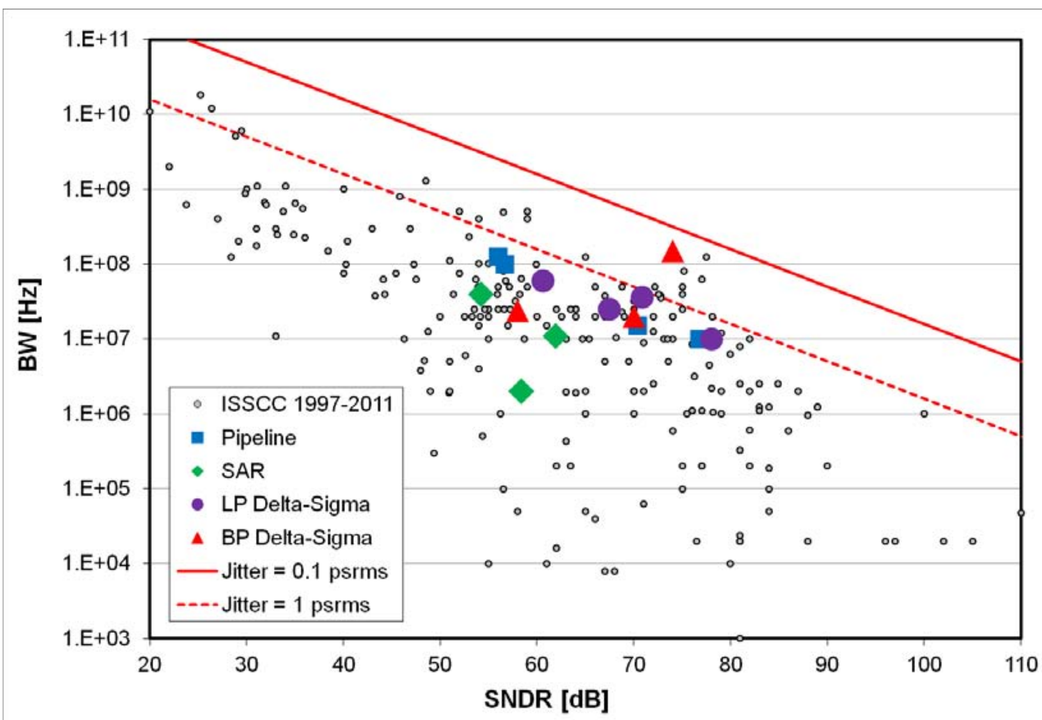

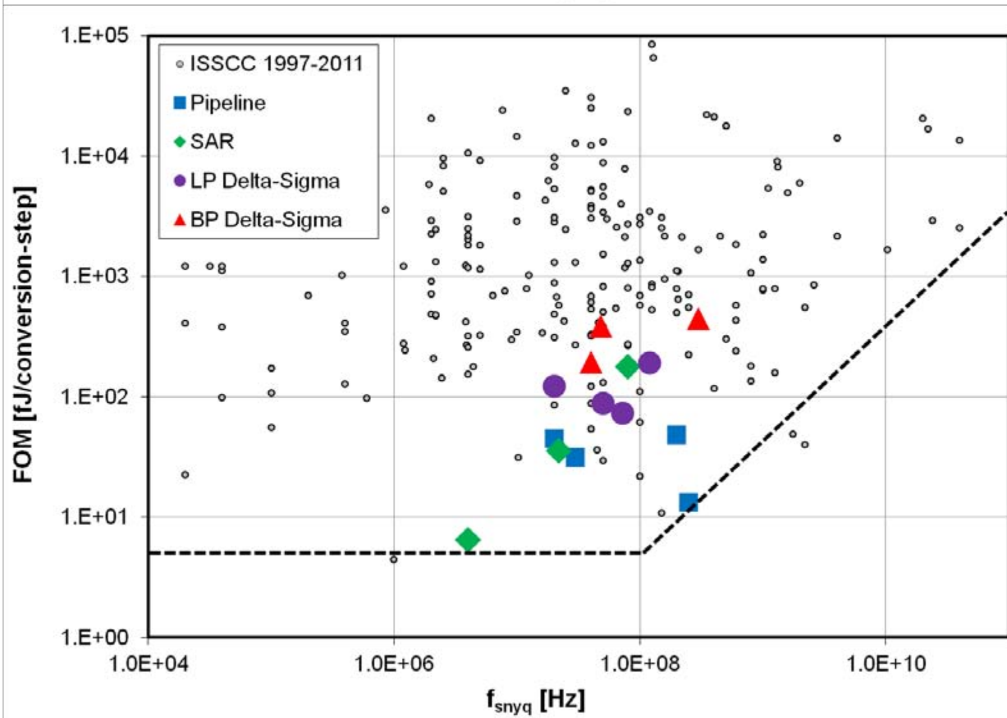

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Energy Efficient Digital – 2012 Trends

Author: Tzi-Dar Chiueh, National Chip Implementation Center, Hsin-Chu, Taiwan, EED

Multimedia and communication technologies have enhanced the lives of mobile consumers by increasing productivity, enhancing the social-networking experience, and delivering improved visual and audio quality for communication links and entertainment. The performance of embedded CPUs has increased to meet the rising demands of general-purpose computations. At the same time, dedicated multimedia accelerators provide a solution for well-defined energy-efficient signal processing under the physical limitations in advanced process technologies. Consumer expectations for increased mobile functionality will continue unabated into the foreseeable future, and hence call for advanced low-voltage technologies coupled with advanced architectures and designs.

While process technology continues advancing and enabling integration on a massive scale, this year's processors come from a wide variety of technological backgrounds. New ground is broken in the key areas of transistor integration, performance-per-unit power and functional integration. This is accomplished across varied process technologies: 65nm, 45nm, 40nm, and 32nm bulk and SOI CMOS technologies.

Figure 1 illustrates the energy efficiency of the main CPU in a smartphone application processor. CPU performance has continually increased in both heterogeneous and homogeneous SoCs. Due to the thermal and power limitations of handsets, the energy efficiency of the CPU has had to increase as well, to stay within the thermal and power envelopes. There is indeed room for further increases in CPU frequency, number of cores, and memory capacity. However, additional power efficiency from technology, circuit, and architecture improvements must be incorporated to offset higher CPU clock frequency, more cores and memory. Many multimedia applications were first implemented in CPUs or other programmable cores. However, the multimedia computational requirements have increased faster than the programmable devices could reasonably address. Historically, this has happened with graphics, imaging and video. Semi-programmable and hardwired cores are now required to fit within thermal limits and economical considerations. There will be a continued need for circuit, architectural, and system innovations to stay on this growth trend. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, and computational imaging, to name a few.

Figure 2 presents the trends in wireless communications standards that have been employed to achieve various link distances and data rates. The wireless networking standards can be roughly segmented into 4 categories: cell phone with the greatest link distance, Wireless LAN (WLAN) with just over 100m link distance, Personal Area Network (PAN) at up to 10m distance and up to 10 Mb/s, and Wideband PAN at up to 10m distance with data rates up to 10Gb/s. In each of these categories, the data rate has increased with time, typically with an increased computational load to move closer and closer to the theoretical channel capacity of the system.

Figure 3 presents video and digital TV trends. A very large number of computations are required to keep up with increasing video bit rates, increasing resolution and frame rates, increasing complexity of the standards for video compression, and new applications such as 3D, and multi-view video, which demand higher resolutions and more concurrent streams. Dedicated high-performance and low-power video processor architectures and high-bandwidth external DRAM interfaces are required to meet the dramatically increasing performance requirements. As the demand for mobile video also follows this trend, energy-efficient implementations are needed to support video streaming, encoding, and decoding for high-definition video. Both low-power video engines and low-power memory architectures leveraging new technology like wide-I/O low-capacitance direct interface to DRAM will be required.

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Application Processor Trends in Smart Phone

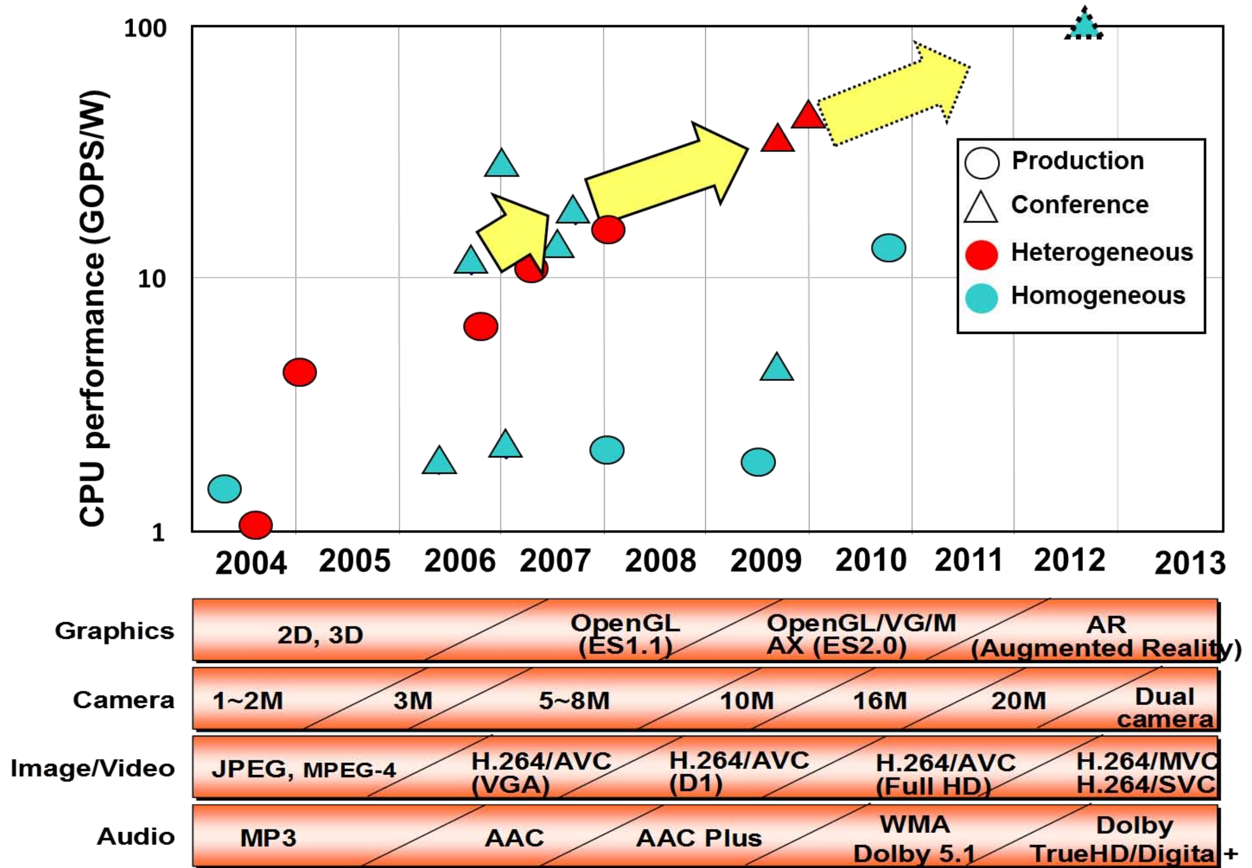

Fig. 1 Application processor trends in smart phones.

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Wireless Network Trends

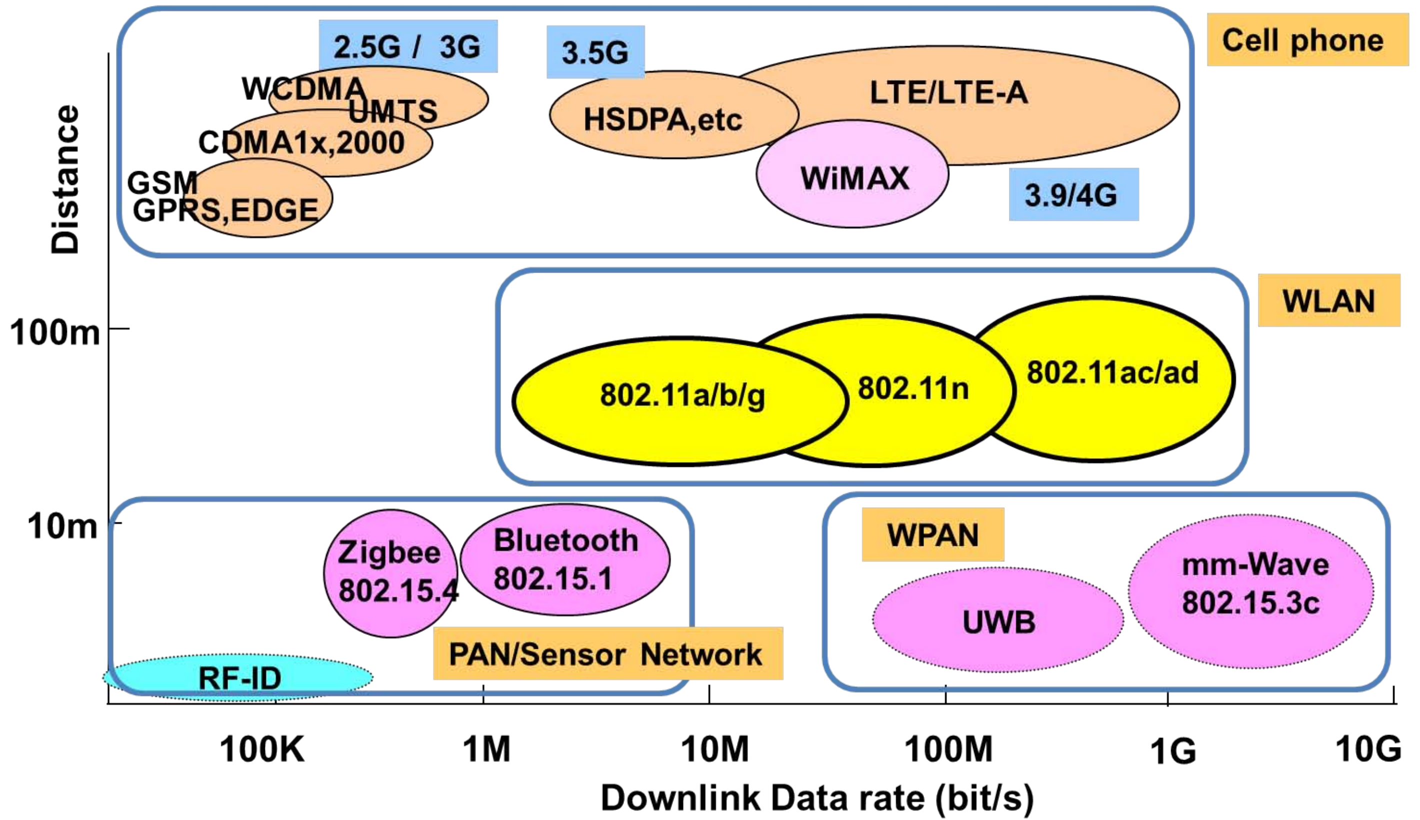

Fig. 2 Wireless network trends.

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Video/DTV Trends

Video Codec (Standard): MPEG-2 / MPEG2(HD) H.264/AVC(VGA) / H.264/AVC (D1/Full-HD) / H.264/MVC H.264/SVC / H.265/HEVC

Application: DVD-Recorder / DTV / Blu-ray Recorder / 3DTV / Digital Cinema / Holographic Recorder

Pixel format: 480i / 1080i / 720P / 480P / 4Kx2K

Bitrate（bps）: ～10M / ～20M / ～50M / ～300M

Memory: DDR-333 / DDR2-667～800 / DDR3-1333/ Wide IO DRAM

Technology: 130n / 90n / 45n / 28n

2004 2005 2006 2007 2008 2009 2010 2011 2012 2013

3DTV application will be leading the consumer market. Multi processor and re-configurable processor support the multiple standard of Quad/3D full HD codec with low power consumption. Higher memory bandwidth is achieved by the high frequency DDRx and wide IO DRAM with 3D packaging. Advanced high speed multimedia interface (HDMI etc.) will be also supported for home network.

Fig. 3 TV and Video trends.

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High-Performance Digital – 2012 Trends

Author: Stefan Rusu, Intel Corp., Santa Clara, CA, High-Performance Digital Subcommittee Chair

This year the continuing progress in CMOS technology provides us with the first 22nm commercial microprocessors featuring new vertical device architectures with triple gates. This enables further improvements in area and energy efficiency.

The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration was achieved some 5 years ago, last year marked the first commercial product exceeding 3 billion transistors on a single die. This trend continues as average complexity continues to increase.

As power reduction becomes mandatory in every application, the trend towards lower clock frequencies also continues, as shown below in the frequency trends plot. This is driven by decreased supply voltages, with processors in the near-threshold or even subthreshold voltage domain. The performance loss of reduced voltage and clock frequency is compensated by further increased parallelism. Leveraging sophisticated strategies to lower leakage, and manage voltage, variability and aging, has bolstered the continuing reduction in total power dissipation. This is helping to rein in the immense demands from PCs, servers, and similar systems, and will yield solutions with less cost and cooling demands, resulting in a greener product.

In addition to the trend to integrate more cores on a single chip as shown in the core trend chart, additional dedicated co-processing units for graphics and communications are now commonly integrated on these complex systems-on-chips. Design of these SoCs requires broad collaboration across multiple disciplines including circuits, architecture, graphics, process technology, system design, energy efficiency and software. New performance and power-efficient computing techniques continue to be introduced at targeted, critical applications such as floating point and SIMD. As a result we can see a downward trend in power consumption, as shown in the power trends chart below.

This year also marks the wider introduction of massively parallel, 3D integrated systems. Thereby, a third dimension of integration becomes available by stacking monolithically-integrated dies and interconnecting them by applying innovative TSV technologies. The result of this integration is a new level of performance in a power-efficient package.

Another trend evident this year is the continued emergence of all-digital phase-locked loops and delay-locked loops to better exploit deep-submicron feature-size scaling, thereby reducing power and area costs. Due to the application of highly innovative architectural and circuit design techniques the features of these “all-digital” PLLs and DLLs have improved significantly versus the recent past. The rms-jitter-versus-power diagram below shows the improvement of the widely accepted figure-of-merit for PLLs and MDLLs.

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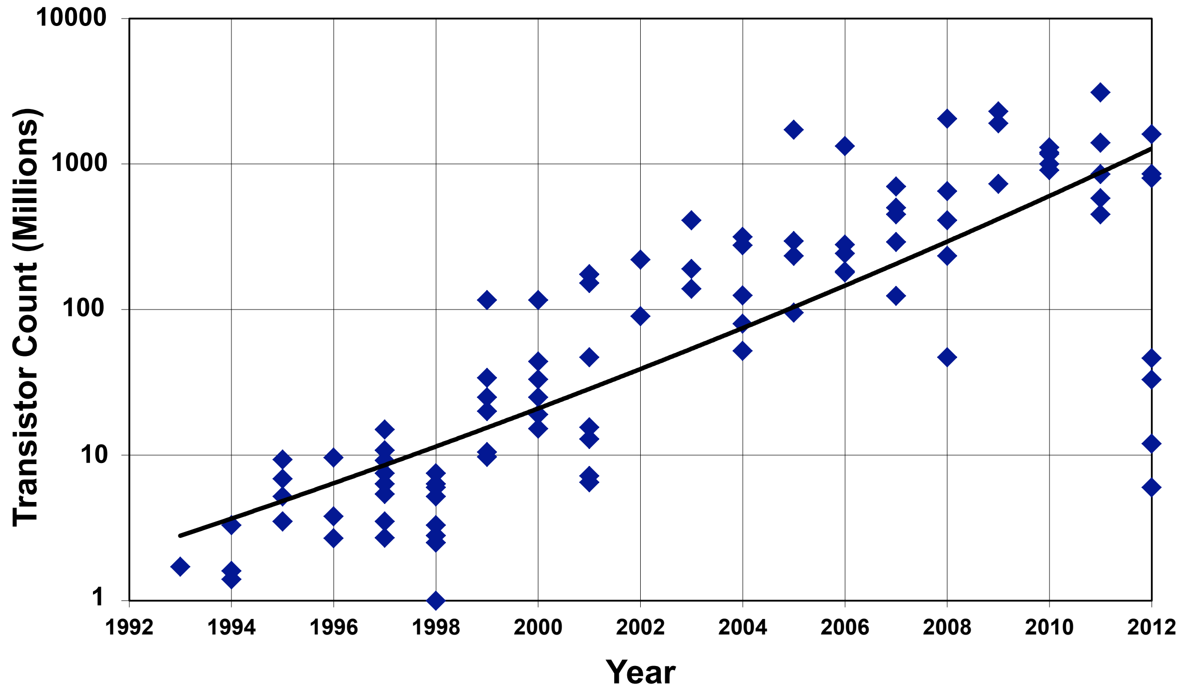

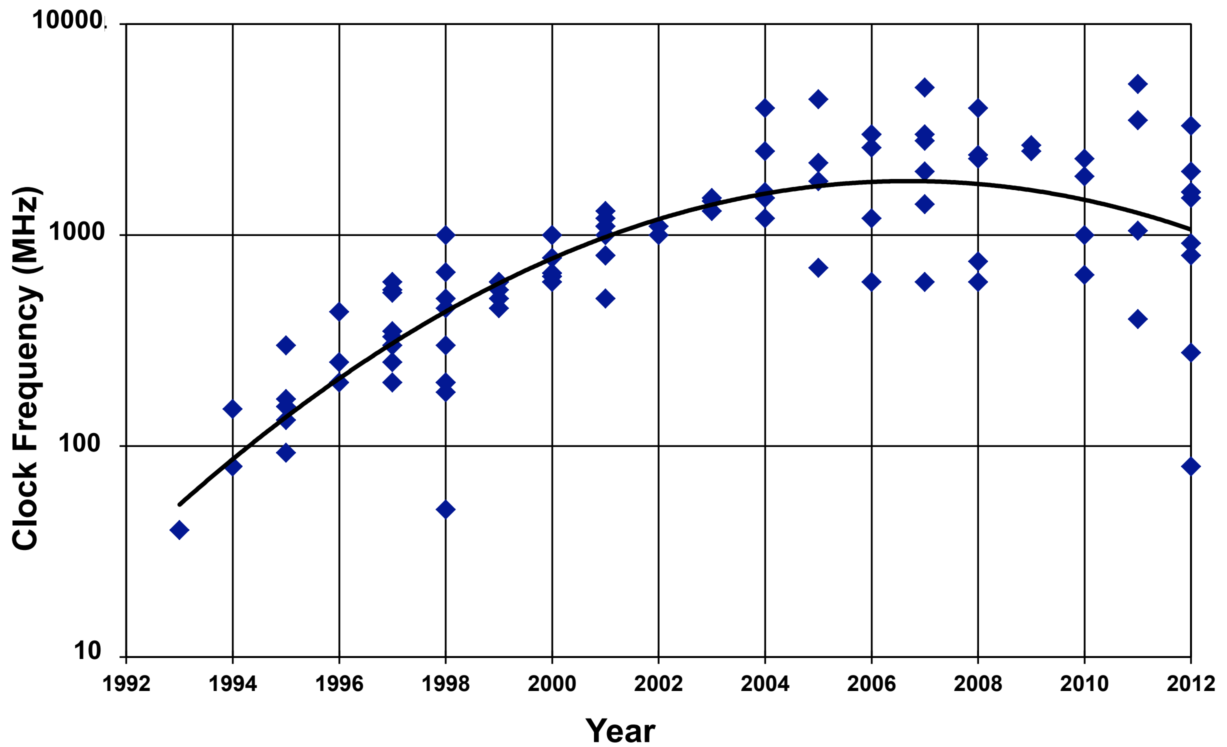

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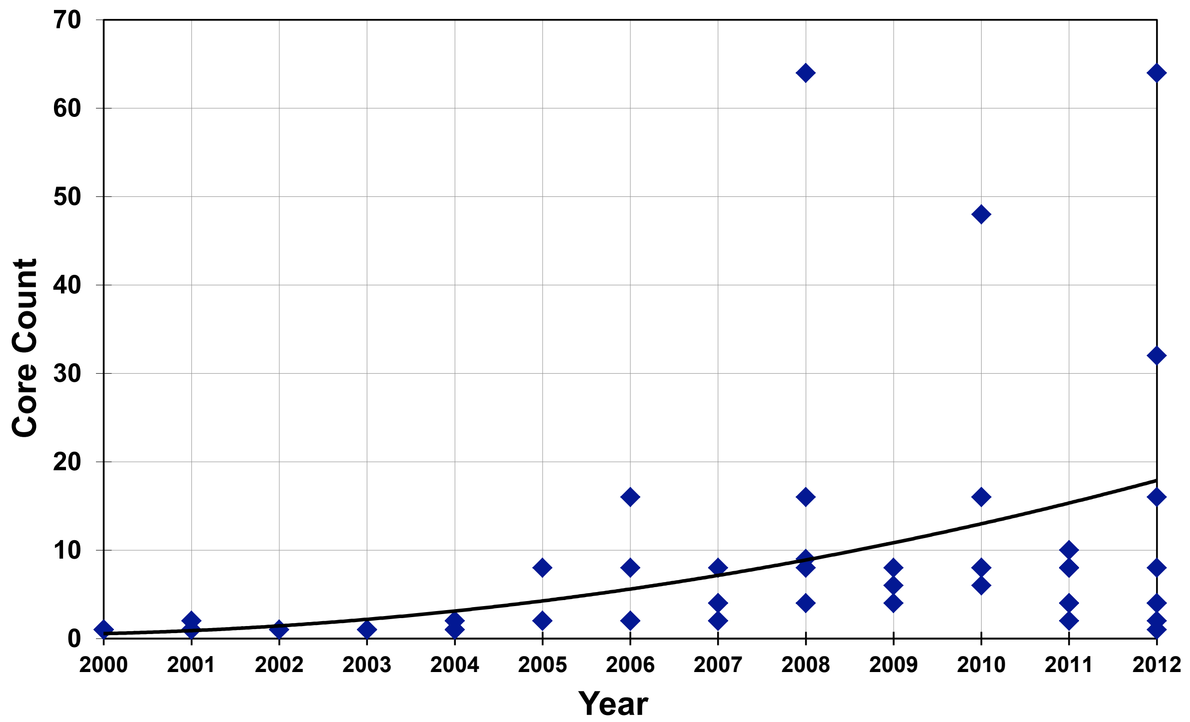

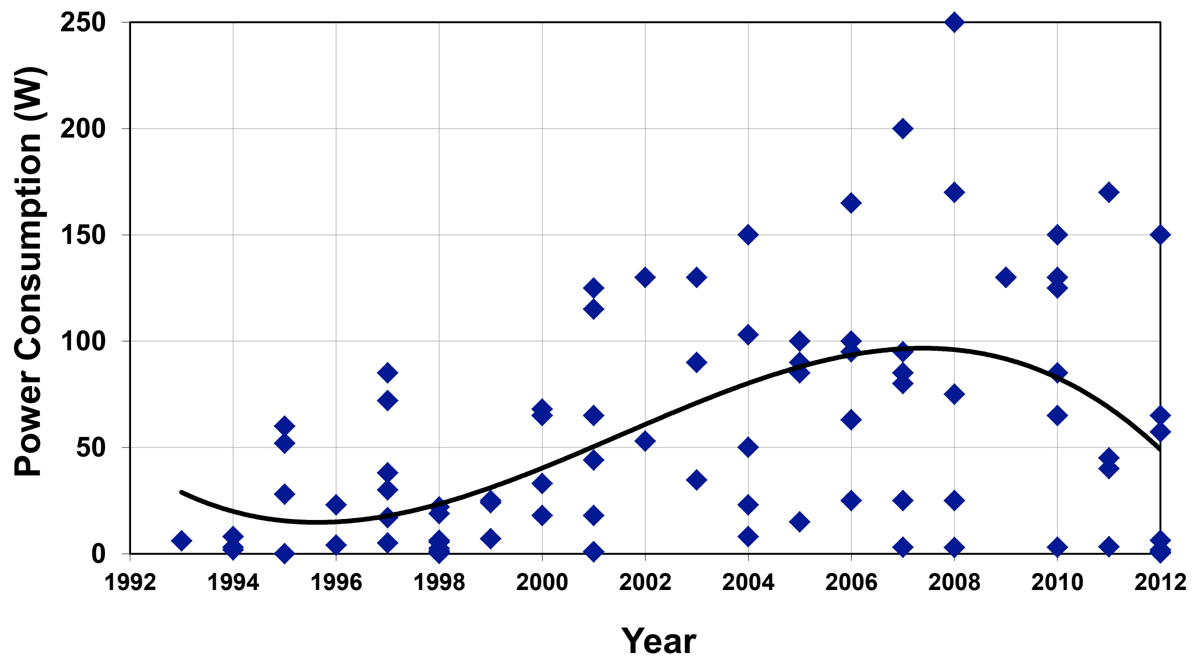

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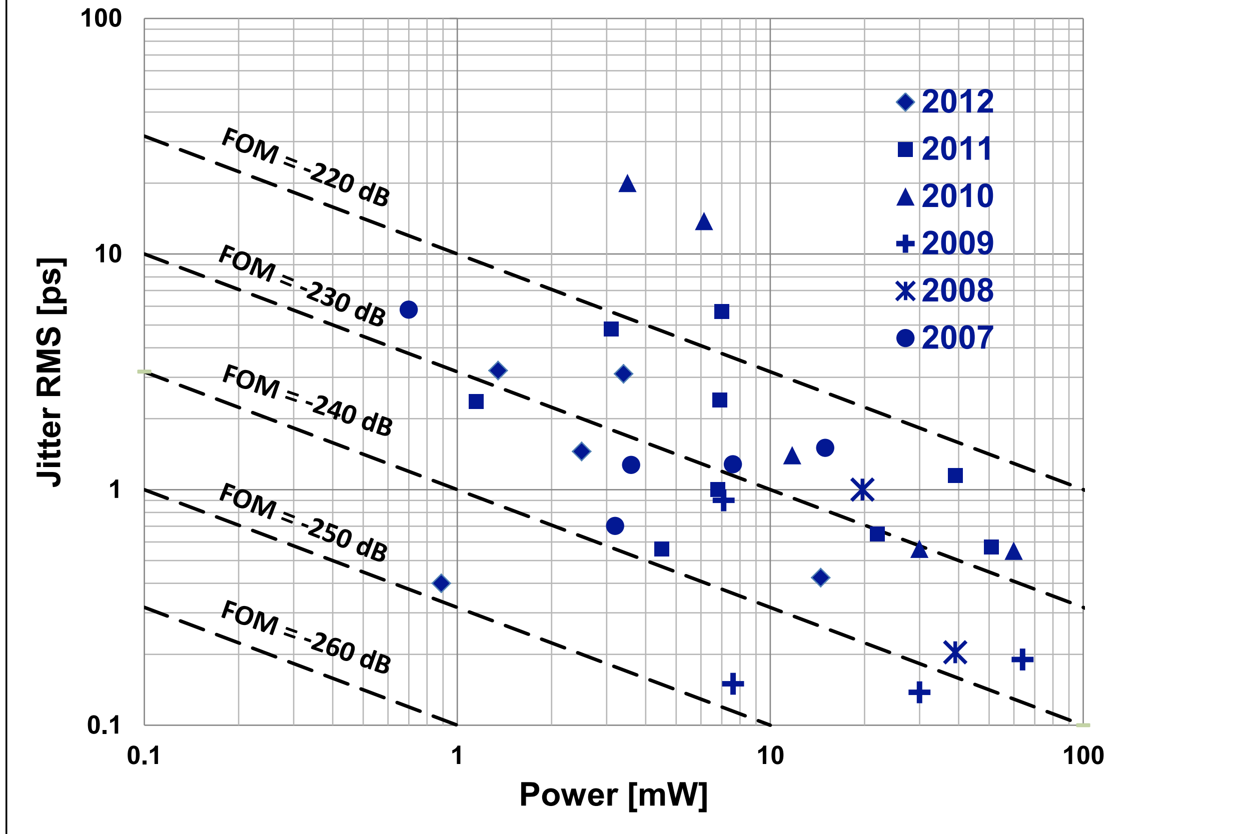

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IMMD – 2012 Trends

Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany

Imagers

The CMOS image sensor business is still one of the fastest-growing segments of the semiconductor industry due to cell phone cameras and other digital-imaging applications. The cell phone camera adoption rate is expected to be approximately 90% for 2009, and 3G mobile technology is accelerating the utilization of multiple cameras per cell phone. Other digital imaging markets include traditional digital still cameras (DSCs) and camcorders, as well as emerging markets such as web cameras, security cameras, automotive cameras, digital-cinema cameras, and gaming.

The resolution and miniaturization races are ongoing, and while the performance requirements stay constant, the pixel size continues to scale down. Pixel resolutions over 20M are commercially available employing enhanced small-size pixels. A column-parallel approach based on pipelined and multiple sampling implementations are emerging for low-power, high-speed, low-noise ADCs for high-resolution DSC and video applications

New innovative technologies are constantly being developed in order to compete in this race. These technologies include advanced sub-100nm CMOS image-sensor fabrication processes, backside illumination and wafer-level cameras. Backside illumination is now a mainstream technology for mobile imaging. Most companies rely on bulk silicon instead of the more expensive SOI approach for backside thinning.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions. In parallel with these efforts is a trend throughout the image sensor industry toward higher levels of integration to reduce system costs.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. High-speed low-power low-noise column-parallel ADCs are becoming a key technology for high-definition video imagers.

Many barriers must be overcome in order to maintain market growth in the image sensor industry. These challenges include better image quality, higher sensitivity, higher sensor resolution, lower cost, higher data-transfer rate, higher system-level integration, lower power consumption, and ‘consumer priced’ integrated 3D imaging. “Sensor plus companion chip” solutions are replacing SoCs except for the most compact camera modules where back-side imaging is combined with 3-D integration.

More groups are presenting sub-electron readout noise performance for low-light imaging applications. For non-consumer, low-light level applications, 2D SPAD-based imager arrays with increasing resolution and smaller pixel sizes are becoming available to compete with EM-CCD technology. These deep-submicron CMOS SPADs are now capable of meeting the requirements for high resolution, high timing accuracy by highly parallel implementation of TDCs, and small pixel pitch with better fill factor.

The trends in emerging markets include lower-bandwidth communication for surveillance cameras, wider dynamic range and optical-communication functions for automotive cameras, faster read-out for digital-cinema cameras, and 3D imaging for gaming. These markets are placing ever-increasing functionality and performance demands on today’s image sensors, which are in turn delivering an exponential rate of growth in both complexity and performance to ensure they can keep pace.

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3D imagers are a very hot R&D topic given the current push toward 3D entertainment, security and automotive applications. Rapid increases in integrated logic functionality are driving a dramatic increase in imager functions and features. Merging 2D with 3D imaging e.g. by interlacing 3D time-of-flight pixels with a standard RGGB pixel architecture as a road towards simultaneous color and depth imaging.

The share of CCDs continues to shrink in machine vision, compact DSC and security applications. Only for the top-end broadcast and top-end digital cameras do CCDs still maintain a significant market share.

Sensors & MEMS

CMOS temperature sensors continue to improve, reaching higher temperatures (200°C), with finer resolution (100μ°C/√Hz), in shorter conversion times (10μs), with simpler calibration (using voltage rather than temperature), and using smaller die size (0.006mm^2).
New technologies for temperature sensors are maturing; thermal diffusivity in particular is proving to be a valuable sensing phenomenon, reaching both high temperatures and good accuracy.
Small-area high-speed temperature sensors in highly scaled 22nm CMOS will be important for microprocessors to limit die temperature to safe values.
MEMS oscillators are improving; phase noise is now low enough for demanding RF applications, 12kHz-to-20MHz integrated jitter is now below 1ps and frequency accuracy is now better than 0.5ppm.
MEMS microphones, accelerometers, and pressure sensors continue to improve as they become common in consumer and automotive applications.

Biomedical

There is an increasing interest in neural applications and significant R&D activity in the field of biopotential sensors for neural recording and stimulation..

- Closed-loop systems being commercialized: acceleration-sensor-enabled neurostimulation devices are CE-marked in Europe, and a closed-loop epilepsy device has completed clinical trials. This is a major innovation leveraging the latest sensor and circuit technology for neural interfacing, allowing for novel diagnostics based on chronic recording.
- Brain-machine interface systems now transferring into pilot clinical trials: there is still some debate about "best methods“. Acute human testing shows a low degree-of-freedom to control robot arms in paralyzed patients, and methods are being adapted for a broader range of neuro applications.
- Continuing efforts are enabling high-spatial-resolution multichannel neural stimulators (e.g. for retinal stimulators) and stimulators with recorders (e.g. for brain research). For example, a retinal implant with 60 pixels received a CE Mark, the next step in sophisticated prosthesis design. Developments are on-going to increase complexity by another order of magnitude.

Expanding demand and growth of telemedicine, remote sensing, and economical design are on the rise as the population ages and cost pressures increase. These pressures are growing significantly with health care reform; the economic value of technical solutions is now being considered along with safety and efficacy.
Silicon technology is enabling new paradigms for biological signal processing. Examples include:

- 0.13μm foundry-based CMOS technology is stabilizing as a low-power process for biomedical purposes, along with 32b processing cores. Partitioning of signal processing between analog and digital domains is still being debated, with both modalities reaching levels that allow for chronic monitoring with minimal energy drain.
- Silicon-based arrays are emerging for analyzing genomes and immunoassays. Multiple paradigms are being explored to eliminate the need for expensive optical components. Proposals are not only to perform hybridization assays on-chip, but also to allow DNA sequencing directly.

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Displays

Single-chip sensing and driving for touch-integrated LCD panels is one of the display technology trends for much thinner and lower-cost realizations. Advanced 3D LCD TV technologies are opening a new era of 3D home theater. The current focus is how to make more realistic views that are comfortable to the eye. 3D realization technologies that do not require glasses, and their driving electronics are emerging for mobile and notebook applications.

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MEMORY – 2012 Trends

Subcomittee Chair: Kevin Zhang, Intel, OR

Mainstream memory technologies continue to be embedded SRAM, DRAM, and floating-gate based Flash for very broad applications. However, as processes continue to shrink in an effort to follow Moore's Law, each incumbent technology is encountering difficulty in maintaining the trend line. SRAM, DRAM and flash cells are becoming increasingly more difficult to scale. In response to the challenges, we see logic processes adopting tri-gate/3D devices along with read and write-assist circuits for SRAMs. Meanwhile, emerging memory technologies are making rapid progress towards product introductions, including PCRAM and MRAM, while resistance RAM (ReRAM) is gaining ground for future applications.
Some current state-of-the-art results from ISSCC 2012 include:

- First 22nm tri-gate/finFET 4.6GHz tri-gate SRAM with assist circuits for lower Vccmin
- Density record beating 19nm 128Gb TLC NAND Flash memory
- New DDR4 3.2Gb/s/pin 4Gb 30nm SDRAM with PVT-tolerant data fetch
- High-speed 443MB/s write throughput multi-layered cross-point ReRAM Macro

SRAM

Embedded SRAM continues to be an important part of wide range of VLSI applications, from high-performance processors to hand-held devices. Historically, the SRAM bitcell follows Moore's Law, shrinking in area by about 0.5× in each generation. This enables designers to put more SRAM bits on die, improving performance. Another key performance metric for SRAM design the lowest reliable operating voltage. This allows memory blocks to reliably operate at the same or better power envelope compared with the previous generation. As the transistor feature size marches toward sub-20nm, device variation has made it very difficult to shrink the bit cell area at the 0.5× rate while maintaining or lowering V_{CCMIN} between generations. Starting at 45nm, the introduction of high-k metal gates reduces the V_t mismatch and enables further device scaling by reducing the equivalent oxide thickness significantly. Design solutions such as read/write-assist circuitry have been used to improve V_{CCMIN} performance at the memory macro level from 32nm and beyond. New transistors such as finFET and FD-SOI emerge as the replacement of planar devices to enable area reduction and V_{CCMIN} scaling of SRAM bit cells.

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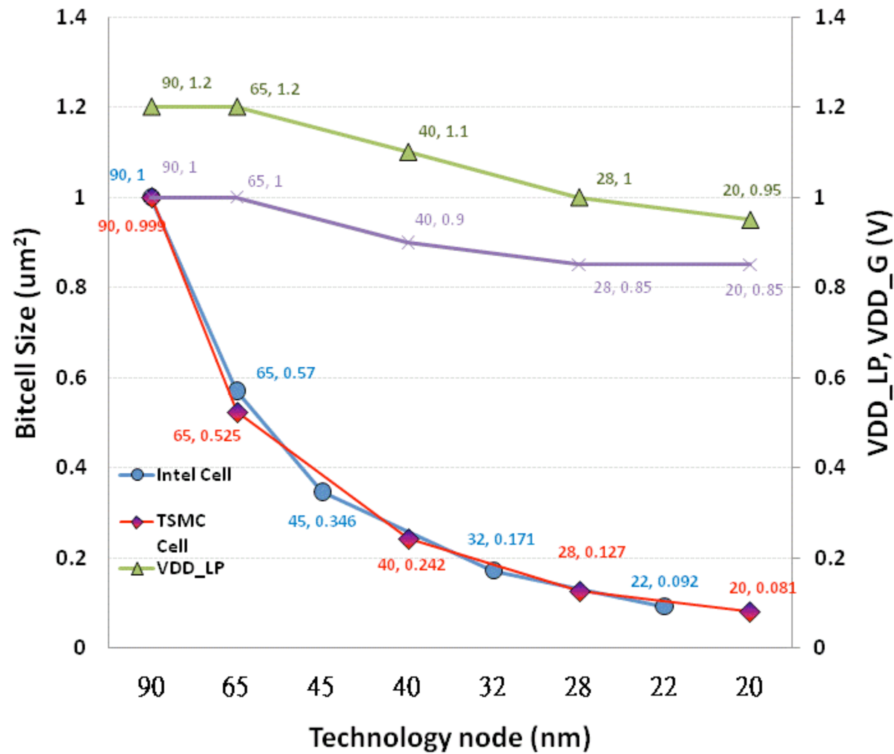

Figure 1. Bit cell Trend

NON-VOLATILE MEMORIES (NVMs)

In recent years, technology and chip development of emerging nonvolatile memories (NVMs) utilizing advanced materials have been intensified. Each of emerging NVMs such as phase change RAM (PRAM), ferroelectric RAM (FeRAM), magnetoresistive RAM (MRAM) and resistive RAM (ReRAM) has excellent read/write and endurance performance as well as low power, as compared with Flash memories. This offers the potential to open up new markets and applications. Commercial uses of these new types of NVM have been very slow to appear because of the rapid reduction of per-bit costs of conventional Flash memory technologies already in the market, as shown in Figure 2. However, these new technologies seem set to capture some specific markets by taking advantage of merits such as high read/write bandwidth over hundreds of MB/s, as shown in Figure 3. This year ISSCC will report on a number of high-density 20nm and sub-20nm designs.

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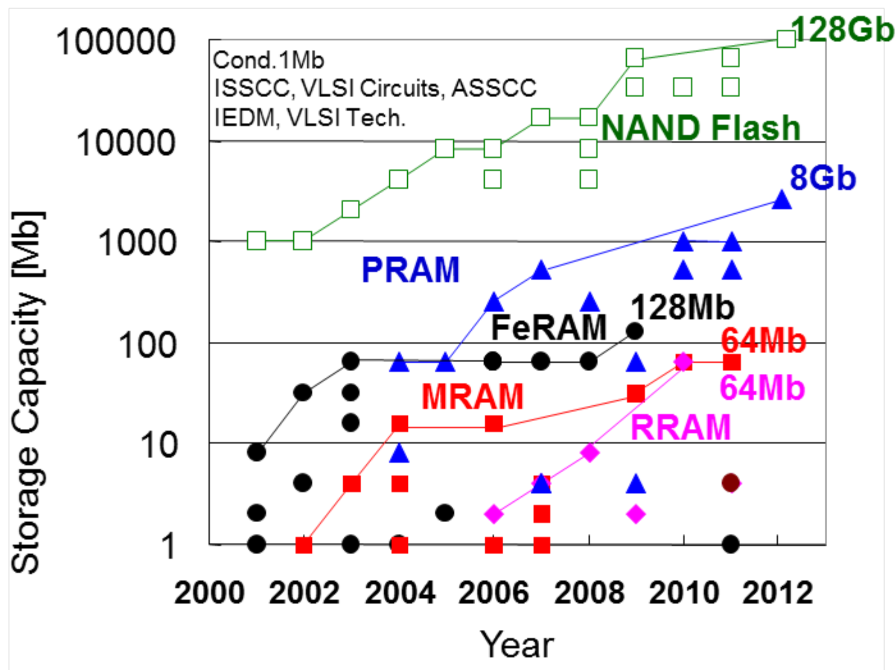

Figure 2. Memory Capacity Trend of Emerging Nonvolatile Memories

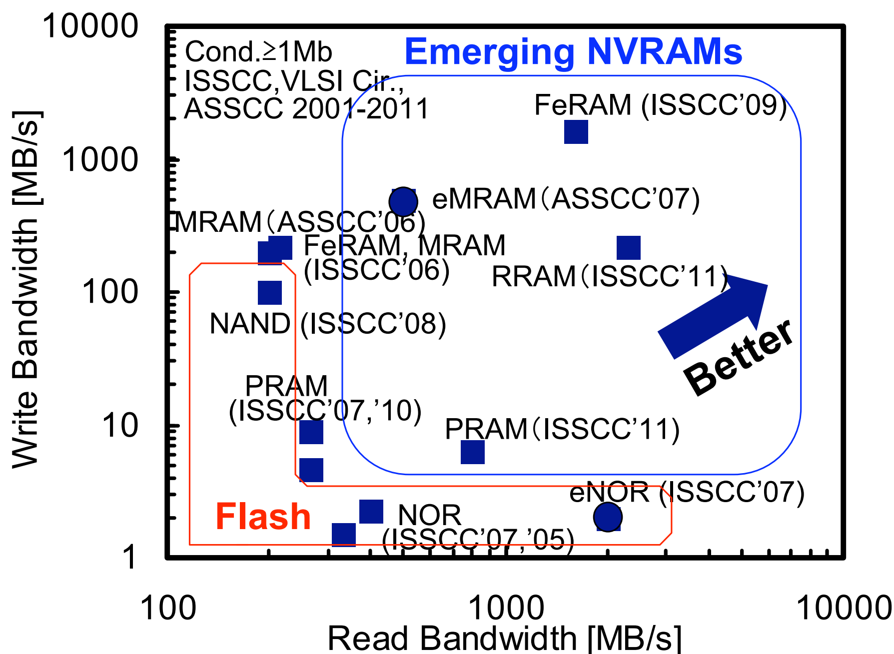

Figure 3. Read/Write Bandwidth Comparison of Nonvolatile Memories

NAND FLASH MEMORY

Significant developments in NAND Flash memory over the past few years are resulting in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). With physical scaling accompanied by advancing multi-level-storage-cell concepts, a 128Gb/die capacity has been demonstrated in 19nm technology with 3 bits/cell operation. Figure 4 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 17 years. As process feature size shrinks, error rates rise, requiring system designers to develop more-sophisticated controllers to offset this issue, some of which are utilized outside the NAND silicon in the system memory controller.

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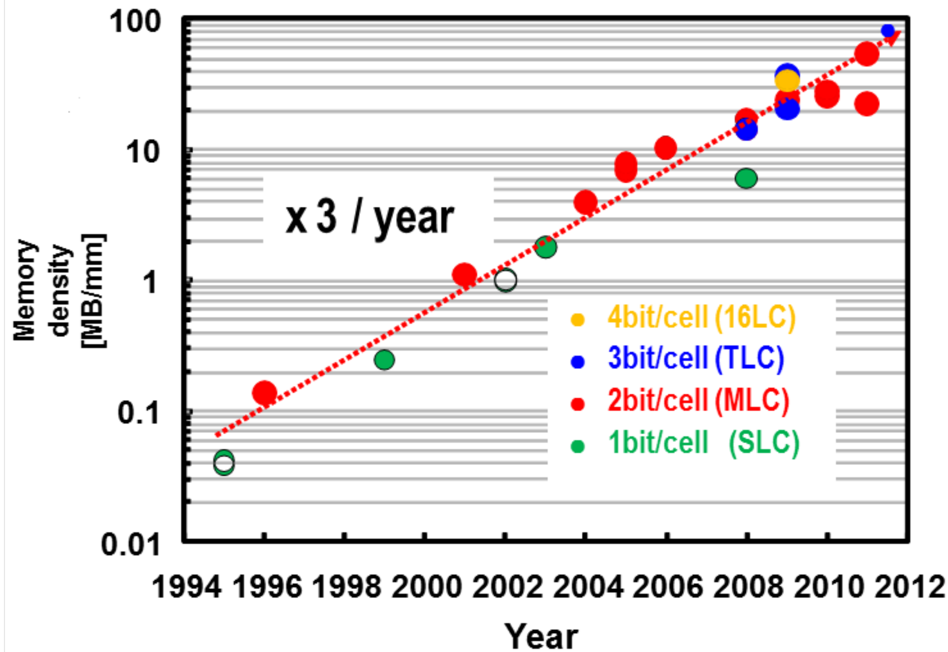

Figure 4 NAND Flash Memory Trends

DRAM & HIGH-SPEED I/O

The gap between on-chip memory/processor frequencies and external data rates continue to increase as conventional high-speed wired interface schemes such as DDRx and GDDRx for DRAM and NAND Flash memory evolve (Figure 5). This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. However, alternatives which accommodate high data rates through the use of wider or differential interfaces will face the problem of increased pin-counts, and enlarged silicon area. Combined with 3D integration of memory and memory/logic in near-future commercial products, new interface technologies will yield more memory stacking, along with lower-power and higher-bandwidth interfaces. This year at ISSCC, papers will cover the first implementations of new standards of LPDDR3, DDR4 along with presentations on through-silicon via (TSV) technologies enabling technology for 3D ICs.

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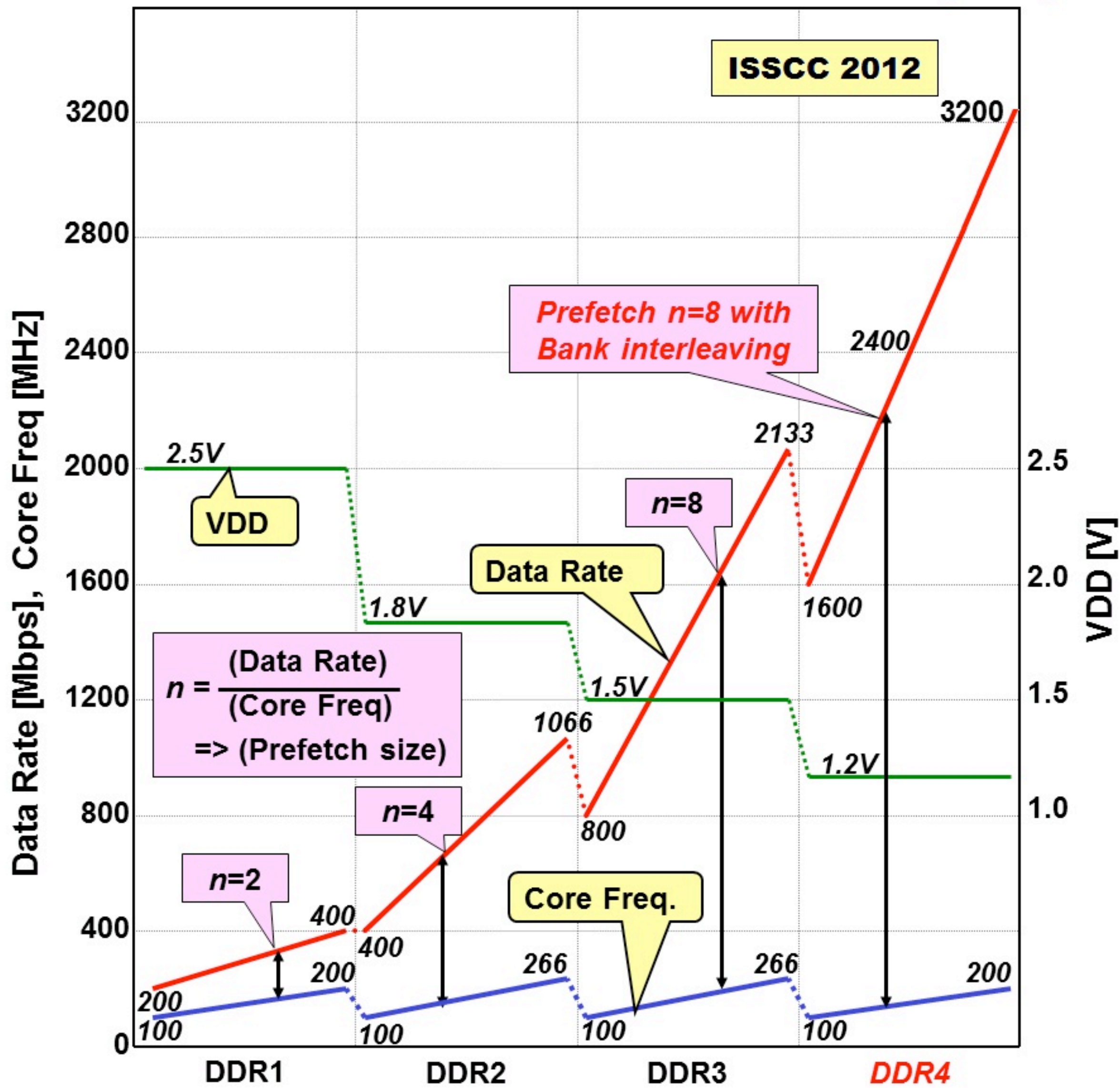

Figure 5 DRAM and High-Speed I/O Trends

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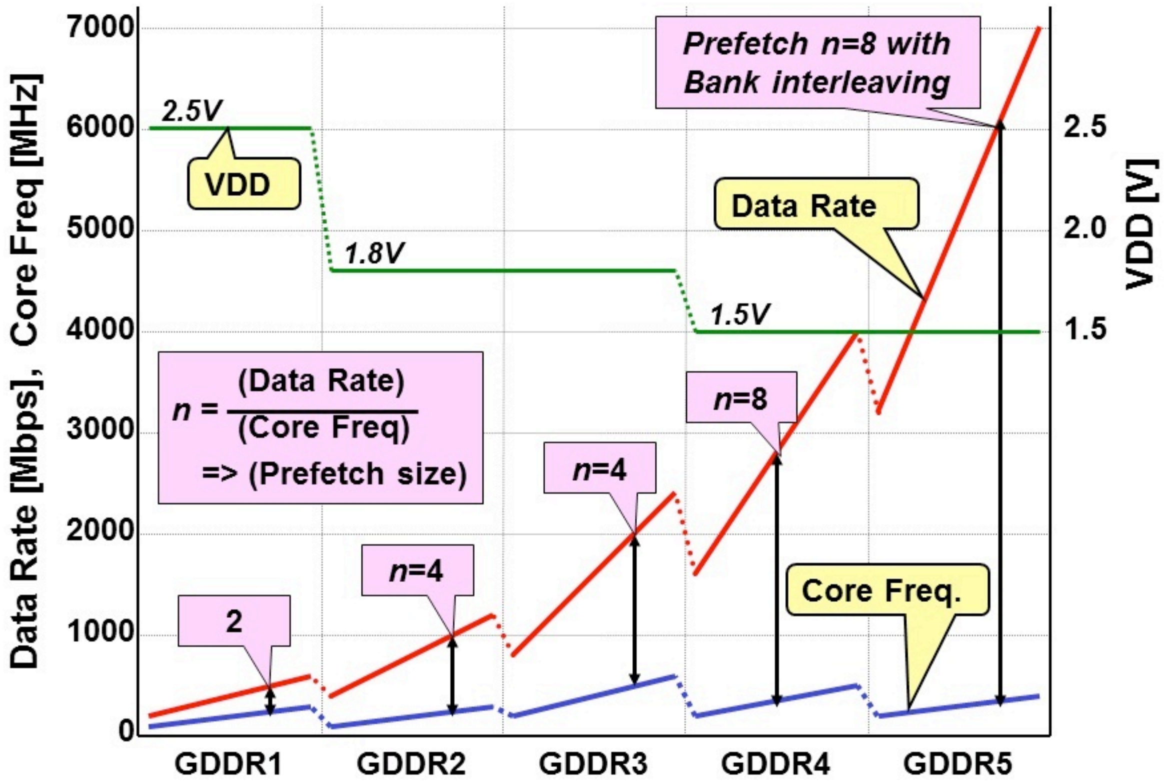

Figure 6 DRAM and High-Speed I/O Trends

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RF – 2012 Trends

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France, RF

Towards the 2012 horizon there are 3 trends that converge, driven by their respective applications. The first one concerns the well-established cellular market, where the demands are focused on high mobility terminals providing high data rates as well, such as the LTE dedicated devices. The second trend is addressing the connectivity sector, where the demand of extremely high data rates (equal to or above 1Gb/s) is contained in devices with several co-existing standards. At the end of May 2011, a press release announced the first product on the market showing extended connectivity features such as dual WiFi, BT and 60GHz WiGig standard compliant. Finally, the third application-driven trend goes towards sensors networks, where the major features are low data rate and above all ultra-low power or even self-contained power-supplied devices. The implementation of all these product families relies on two technology trends. First of all, the transceiver integration, performed either monolithically or using a 3D heterogeneous scheme, pushes towards the ultimate air interface. Hence, a large majority of the devices show full integration up to the antenna(s), as well as a removal of the external bulky SAW or BAW filters at the RF interface. And finally, the trend of multi-radio SoCs is now consolidated for a large majority of products.
In emerging applications, the most advanced sub-nm technology nodes have opened some application fields reserved so far for III-V electronics. For the past few years, more and more academic and research institutes have investigated fully integrated IC's for THz imaging and sensing. As well, these carrier frequencies above 100GHz are well placed for very high data rate communications (>10 to 20Gb/s), hence finding a meeting point with wireline communications.

This document gives highlights on some critical building blocks addressing these applications.

Cellular VCOs

The voltage-controlled oscillator (VCO, and its digitally-controlled counterpart, DCO) is a traditional bottleneck in radio design, where it provides the RF reference frequency needed in all transceivers. The key features of a VCO are oscillation frequency, frequency tuning range, spectral purity (usually quoted in terms of phase noise), and power consumption. A typical trade-off in VCO design involves phase noise, power consumption, and tuning range. Achieving the phase noise performance mandated by the 2G/3G/4G cellular radio standards requires a VCO power consumption that is often a significant part of the total power budget, especially if a large tuning range is needed to cover many bands and standards.

A noticeable trend in VCO design is to let the VCO oscillate at a center frequency of approximately 8GHz with a large enough tuning range, and to recover cellular frequencies via frequency division by 4 or 8. This is shown in Figure 1, which reports the phase noise at 1MHz vs. the oscillation frequency of some of the most significant VCOs published over the last five years. It is apparent that the rate at which phase noise increases with frequency is reduced thanks to this solution, which also allows for a substantial improvement of the phase-noise figure-of-merit (FOM), expressing the noise-power trade-off (Figure 2). A second trend is to design VCOs with increasingly larger tuning ranges, in order to cover newer bands and standards, at the cost of a reduced FOM improvement.

Technology Trends in Millimeter-Wave and Terahertz

Silicon millimeter-wave integrated circuits operating at 60 to 100 GHz continue to be a very active research area. Specifically, the last seven years have witnessed a rapid increase in integration levels, moving from building blocks, to subsystems, to full transceivers, to phased-arrays on a chip, all in either CMOS or BiCMOS technology. Moving ahead, silicon millimeter-wave integrated circuits are expected to mature into fully-qualified commercial solutions with ever-improving performance and efficiency.

An emerging research area is silicon-based sub-millimeter-wave or terahertz sources, detectors, and systems for imaging, radar, and potentially, communications. Silicon technology once again allows reduced cost and high levels of integration, including on-chip antennas. CMOS VCOs have already been demonstrated at 100 to 500 GHz; however, wider tuning

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ranges and higher output powers are still needed to realize useful systems. Detectors or receivers above 100 GHz have been demonstrated in conventional CMOS technology, although improved sensitivities are needed to enable high-throughput passive cameras. Finally, interest in imaging is expected to drive the development of single-chip CMOS terahertz cameras with significantly more than 1,000 pixels.

Power Amplifiers

Since the first introduction of CMOS cellular PAs in 2002, continuing efforts and new design techniques have improved their performance. While in the beginning, an attempt was made for 2G/2.5G to deliver enough output power, recently focus has been shifted to supporting non-constant envelope modulations, improving power efficiency, and supporting more bands for one PA. All PAs to appear this year target WCDMA (need to support 64QAM), and one of them supports 3 bands (Figures 3 and 4).

Concerning power amplifiers at millimeter wave frequencies, the new trend goes towards higher Power-Added Efficiency (PAE), while keeping compliancy with process reliability concerns. The 77GHz PA to appear this year reports a record PAE and saturated output power (Figure 5).

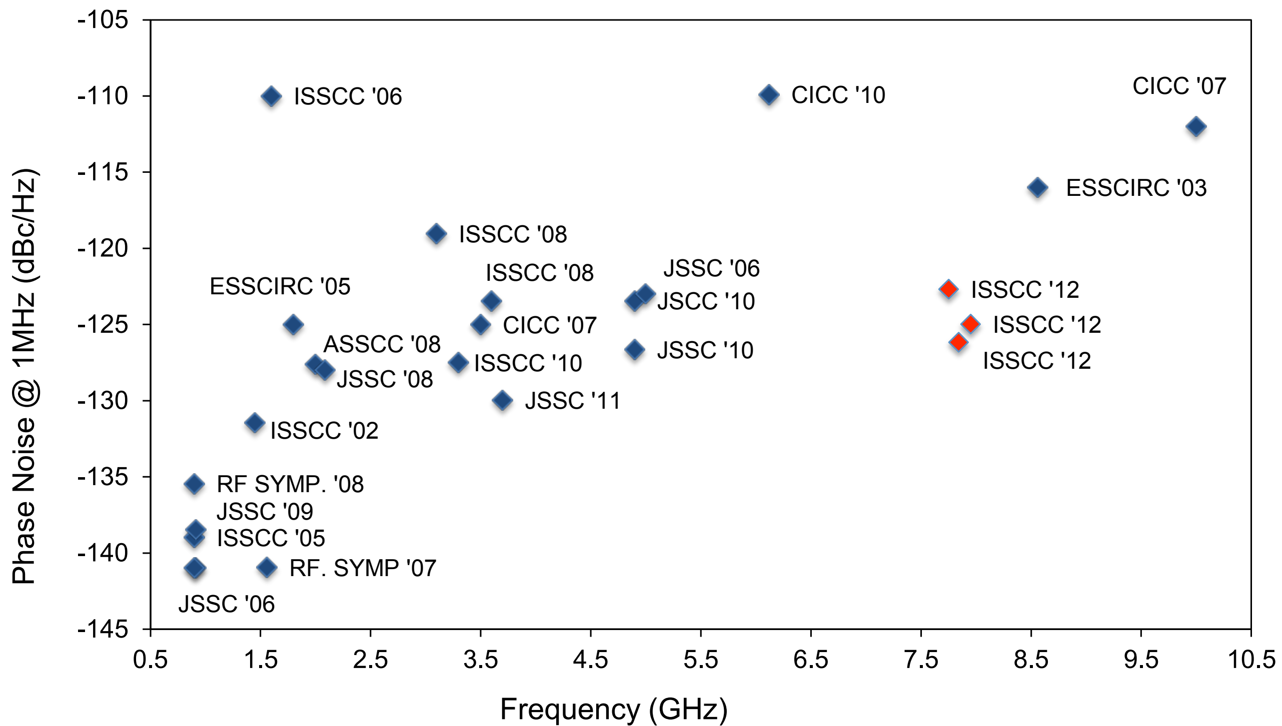

Figure 1: Phase noise at 1MHz offset frequency vs. oscillation frequency

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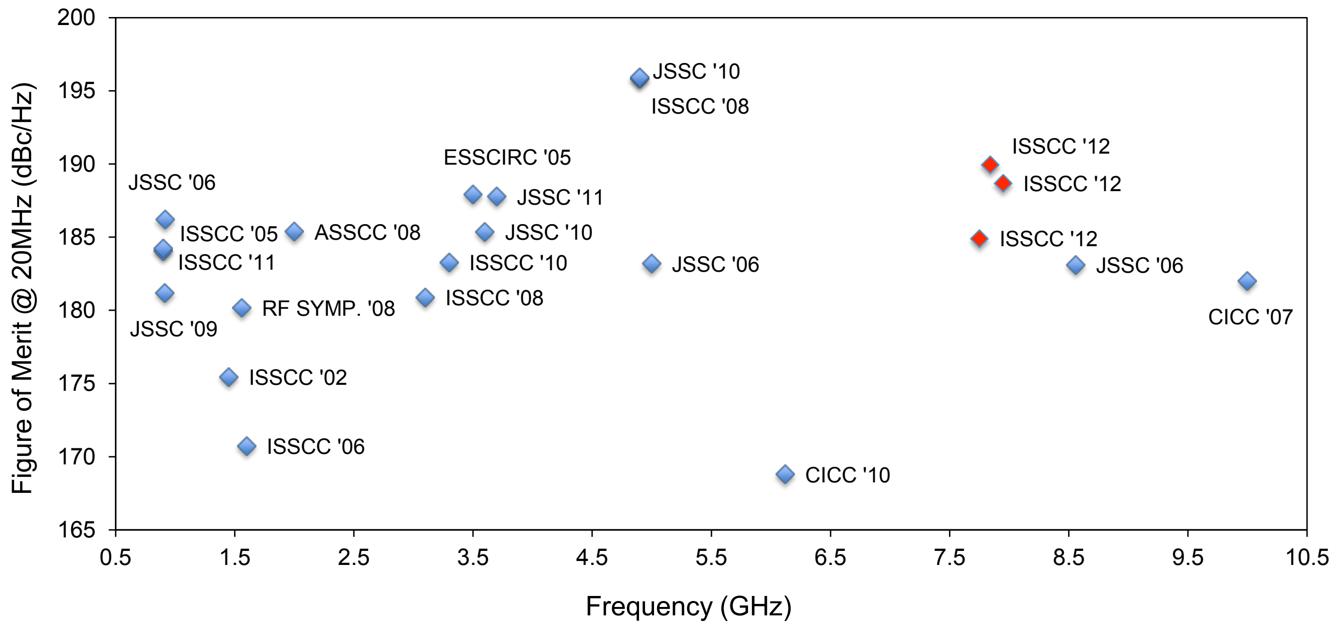

Figure 2: Phase-noise FOM at 20MHz offset frequency vs. oscillation frequency

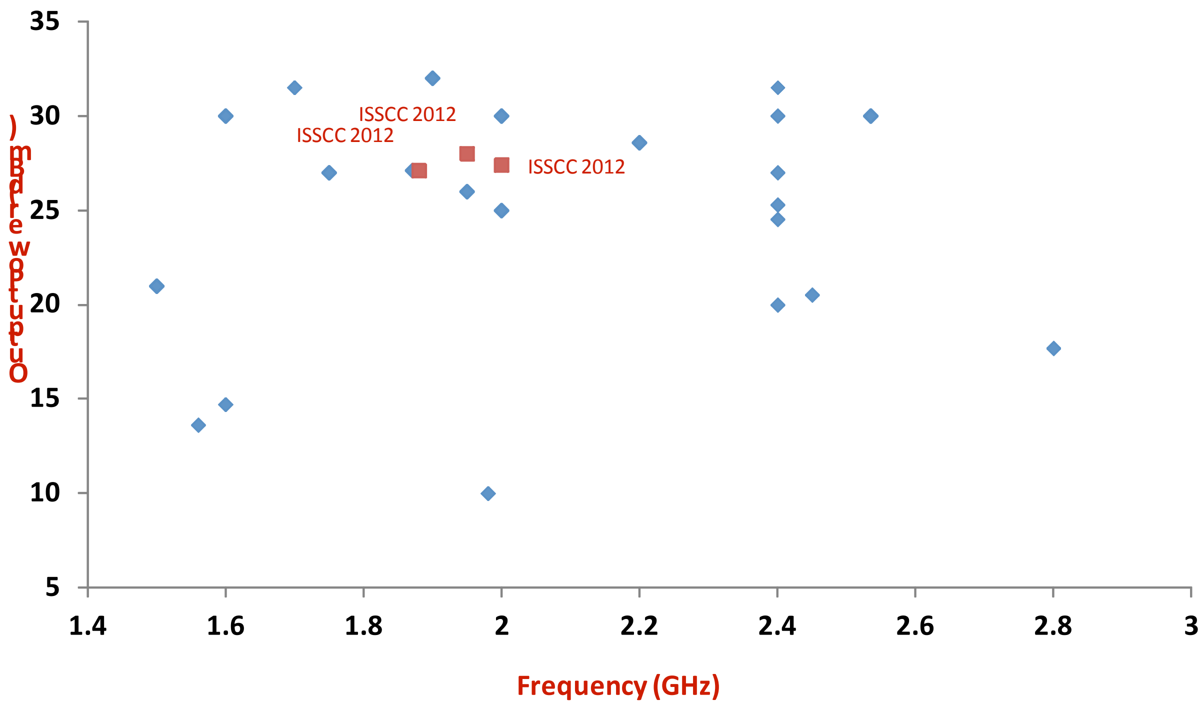

Figure 3: Frequency (GHz) vs. output power (dBm) for RF PAs.

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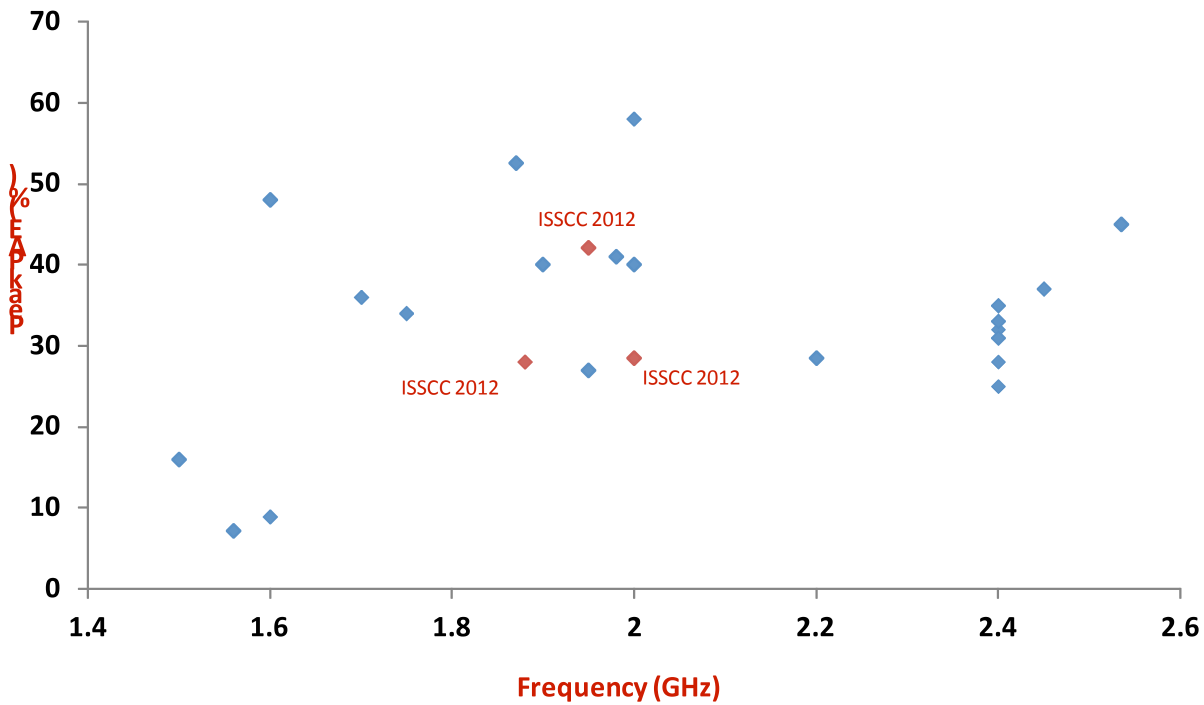

Figure 4: Frequency (GHz) vs. peak power-added efficiency for RF PAs.

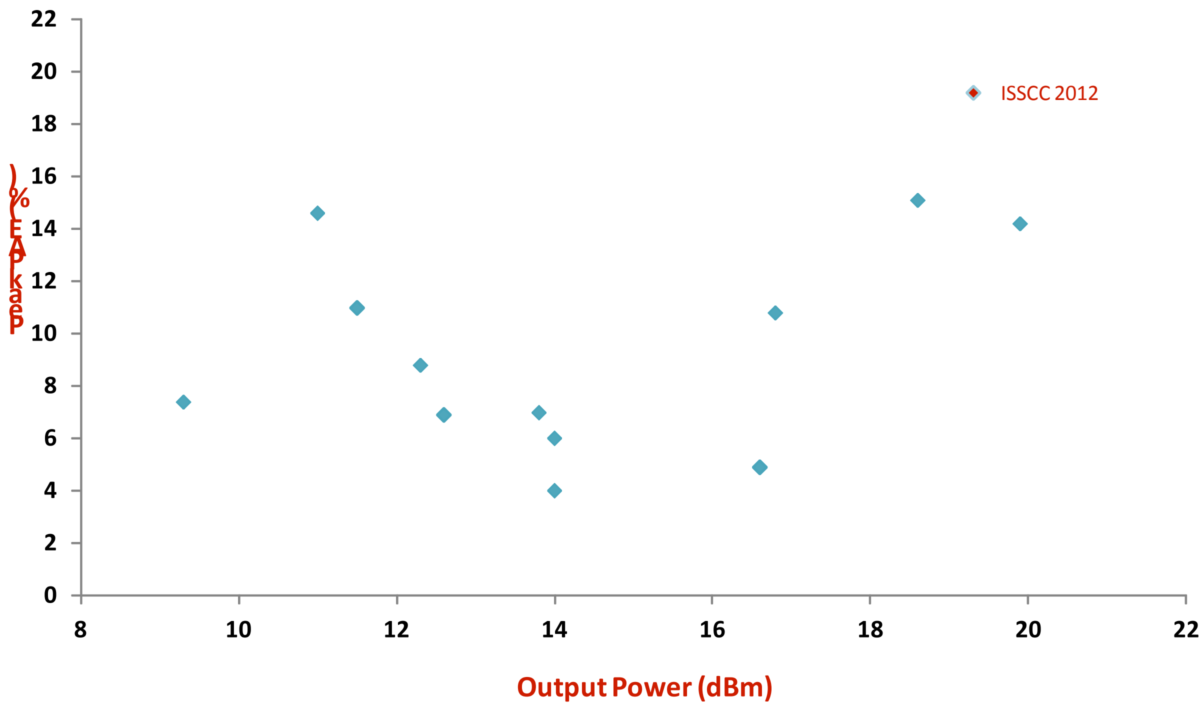

Figure 5: Saturated output power (dBm) vs. peak power-added efficiency (PAE) for millimeter-Wave PAs.

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Technology Directions – 2012 Trends

Author: Siva Narendra, Tyfone, Portland, OR, TD Subcommittee Chair

Large-Area Low-Temperature Electronics

A clear breakthrough in research for large area electronics in the last decade has been the development of thin-film-transistor (TFT) processes with an extremely low temperature budget. Thanks to the low temperatures involved (<150°C), these TFTs can be manufactured on flexible and inexpensive substrates like plastic films and paper.

The semiconductor materials used for these developments have for a long time been carbon-based organic molecules like pentacene (a p-type semiconductor). More recently, organic n-type semiconductors and amorphous metal oxides, which are also n-type semiconductors, have emerged. Popular metal oxide semiconductors are Zinc Oxide (ZnO) and amorphous Indium Gallium Zinc Oxide (IGZO or GIZO). The mobility of n- and p-type organic materials has reached values around 1cm^2/Vs, while metal oxides surpass the 10cm^2/Vs. Operational stability of all semiconductor materials has greatly improved, and should be sufficient to enable commercial applications, especially in combination with large-area compatible barrier layers to seal the transistor stack.

At the state-of-the-art p-type only, n-type only and complementary technologies are available. Most TFTs are still manufactured with subtractive methods based on lithography, but there is a clear emphasis on the development of technologies that could provide higher production throughput, based on different technologies borrowed from the graphic printing world like gravure, screen printing and offset.

The technology roadmap in the field of large-area and low-temperature electronics thus focuses on lowering the cost-per-unit-area, instead of increasing the number of functions-per-unit-area that is accomplished in mono-crystalline Si technology according to the well-known Moore's law.

Together with traditional applications like flexible displays and electronic RFID tags integrated in the wrapping of retail goods, the improvement of TFT performance, reliability and ageing stability has enabled first prototypes of applications integrating sensors and actuators together with low-temperature TFTs. Examples include signage, pressure and light-sensitive foils, sheets capable of distributing RF power to appliances, energy scavenging devices, etc.

According to this trend, ISSCC 2012 will feature a flexible pedometer powered by foot motion, a flexible touchpad based on organic TFTs, an RFID capable of bidirectional communication combining organic and metal-oxide TFTs, and an IGZO digital-to-analog converter that can be used as an integrated column driver in OLED display backplanes (Figures 1 and 2).

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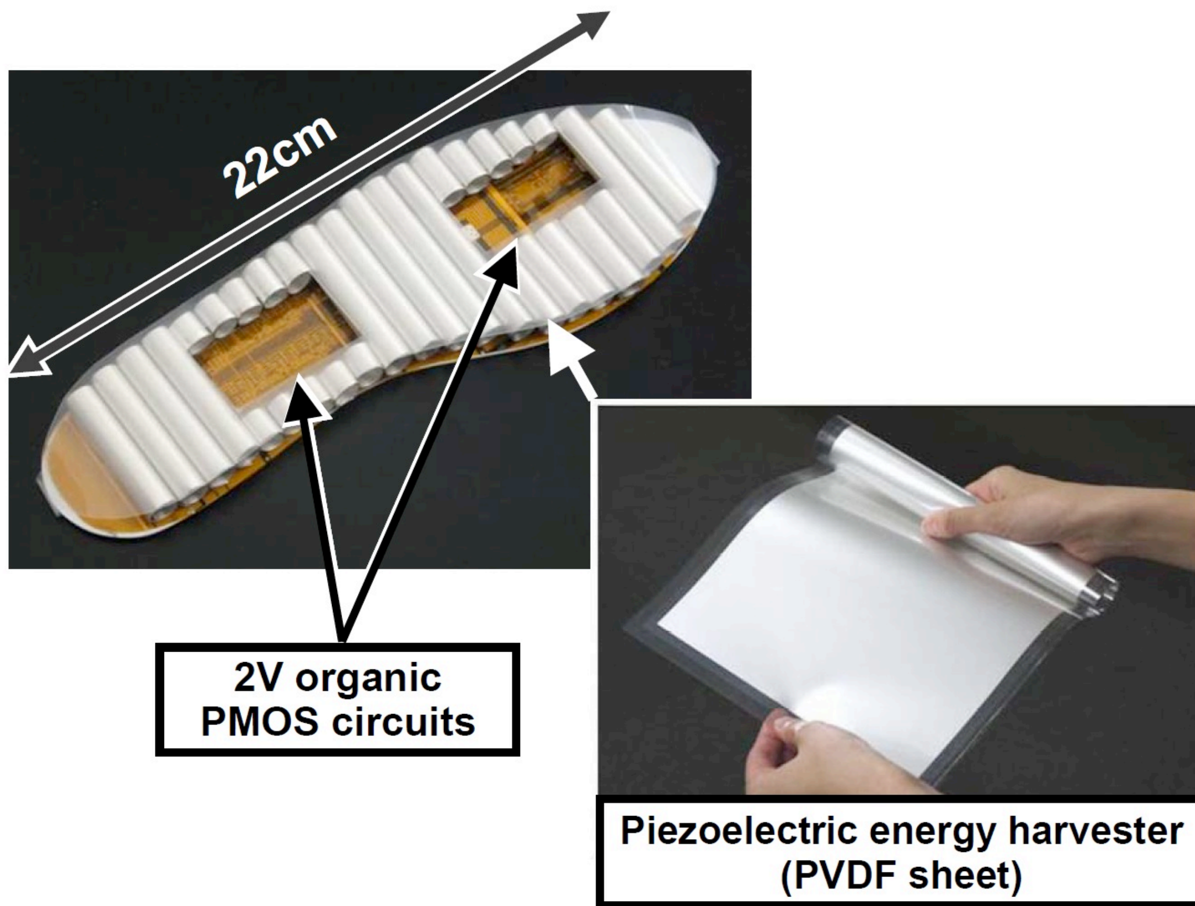

Figure 1. A flexible insole pedometer: a device that counts the steps while being powered by the movement of the foot itself, made with an organic piezoelectric foil (PVDF) coupled to organic p-type circuit (ISSCC 2012 paper 18.1).

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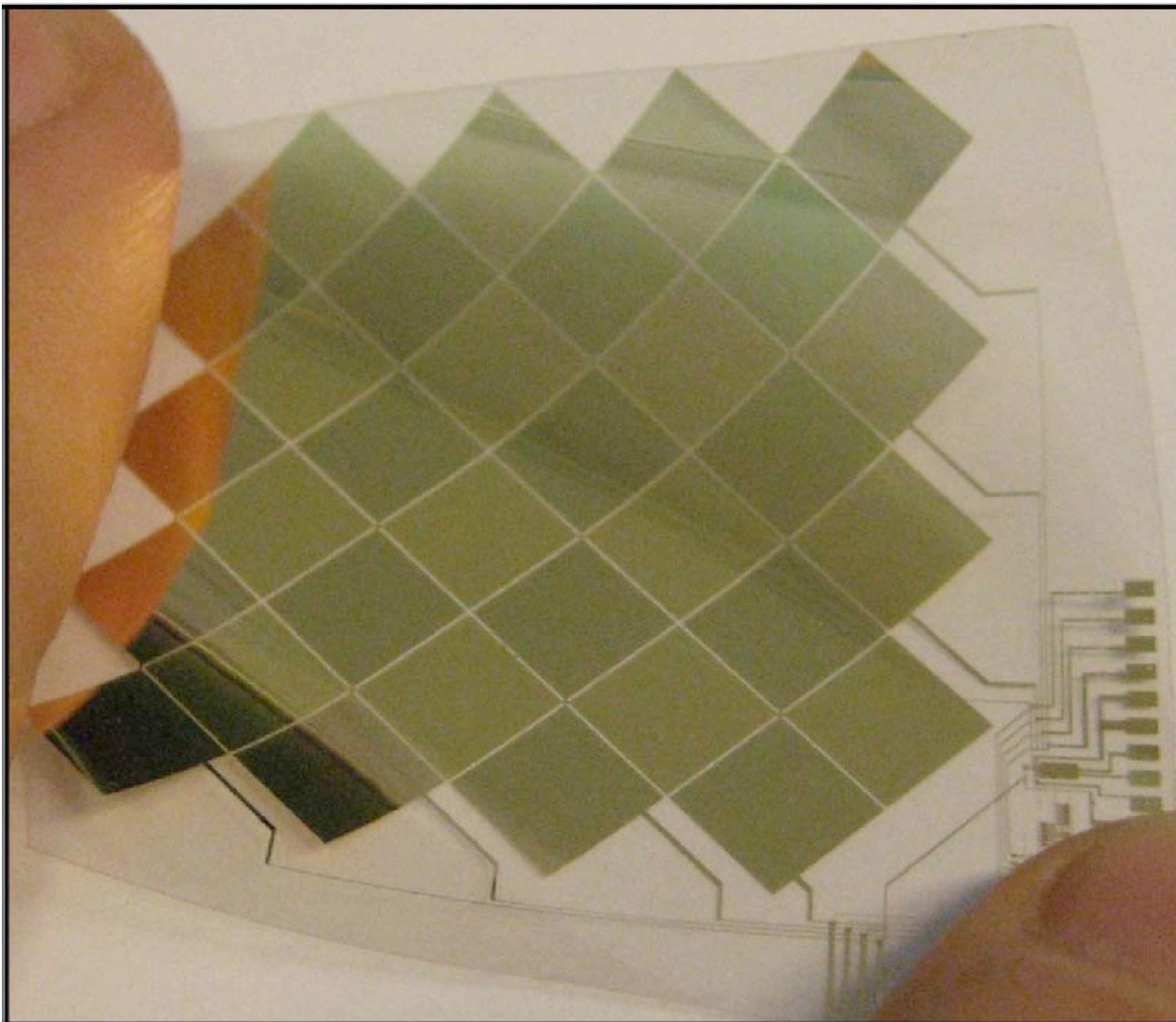

Figure 2. A touch-pad based on a capacitive sensor read-out by organic p-type transistors (ISSCC 2012 paper 18.2).

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Wireless – 2012 Trends

Subcommittee Chair: David Su, Qualcomm Atheros, San Jose, CA

Data rates for modern wireless standards are increasing rapidly and this is evident from the trend of cellular standards (shown in Figure 1). The data rate has increased 100X over the last decade and another 10X is projected in the next five years. This trend is partly contributed by using more complex modulations (e.g. using OFDM – Orthogonal Frequency Division Multiplexing - for better spectral efficiency) at the cost of digital signal processing (DSP). In addition, the expansion of channel bandwidth is also an effective way to achieve the data rate increase. This is seen in the wireless connectivity chart (e.g. 802.11x) shown in Figure 2. The channel bandwidths for the WLAN standards increase from the traditional 20MHz (802.11g), 40MHz (802.11n), 160MHz (802.11ac) and finally >1GHz (802.11ad). Because the available spectrum is limited in the low GHz range, for >1GHz channel bandwidth, the carrier frequency has been moved from 2.4/5GHz (802.11a/b/g/n) to 60GHz (802.11ad) in the mm-Wave range.

With the available spectrum in the 60GHz range, >1Gb/s data rate can be achieved with modest modulation. The initial 60GHz feasibility in CMOS was shown in 2009. A silicon valley start-up, SiBeam, demonstrated a complete end-to-end system that supports a robust wireless link in 60GHz and achieves 3.8Gb/s in 1.76GHz (ISSCC 2011 Paper 9.3). This trend ignites more research and development from both academia and industry in mm-Wave communication.

As described earlier, the spectrum is becoming very crowded because of many licensed and unlicensed wireless applications occupying most of the frequency bands. **Cognitive radio** is one of the more promising solutions to discover and utilize the available white space in existing spectrum in the presence of many wireless applications. Therefore, the current trend for cognitive radio is to design highly linear transceivers that can cover a very wide frequency range and various channel bandwidths. As a consequence of high-linearity and wideband design requirements, distortion cancellation and tunable RF channel-selection techniques are very critical. Most transceivers in this category are adopting digital calibration and analog-feedback techniques to increase the linearity performance for a very tunable front-end to cover a wide range of frequencies.

Wireless Sensor Networks (WSNs) require ultra-low-power radio to increase the life duration of the battery, or better, to eliminate the battery using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. Wake-up radio becomes, then, one of the main building blocks of the WSN node. Once the radio is awake, power efficiency becomes the main target for both high- and low-data-rate communication. Such WSNs will enable electronics for sustainability.

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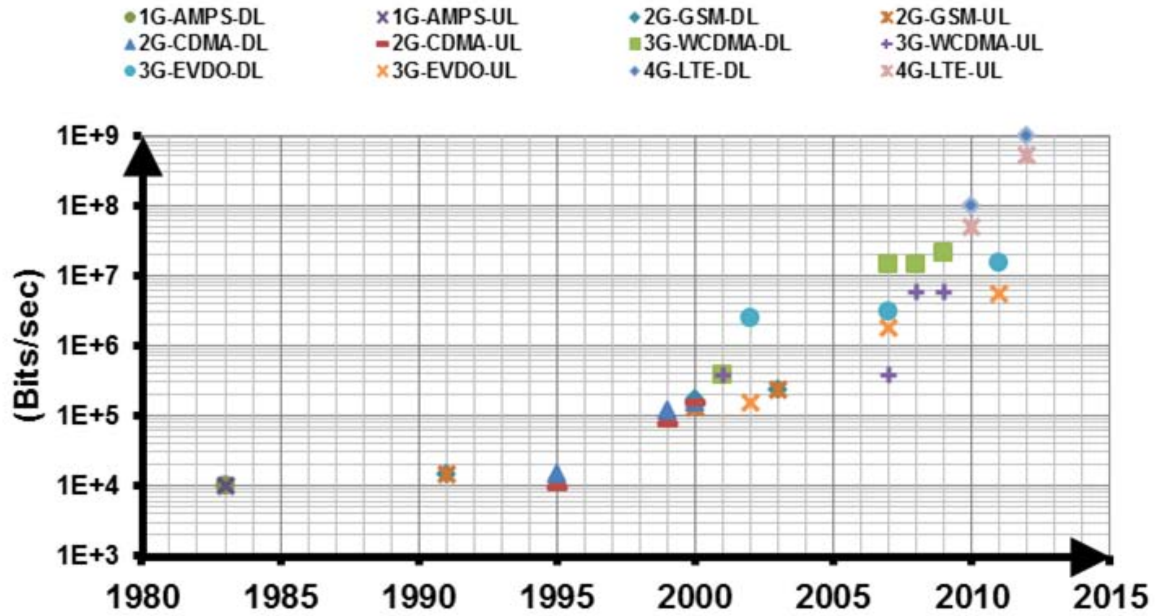

Figure 1: Data Rate Trend of Cellular Standards

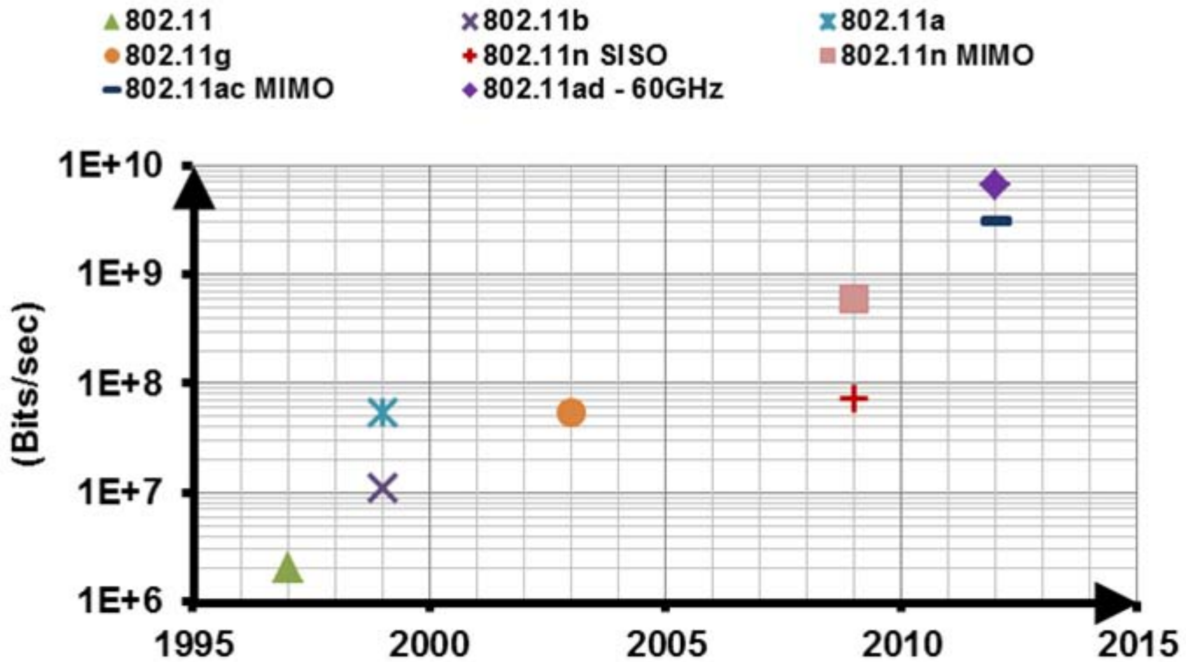

Figure 2: Data Rate Trend of Wireless Connectivity Standards (802.11x)

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Wireline – 2012 Trends

Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY

High-speed I/O bandwidth needs are increasing at about 2× per year as the requirements for data transmission driven by the use of the cloud and data streaming gather momentum. Together with the increase in data rates, the systems are also rapidly approaching power limits that constrain the I/O bandwidths. There is also a need for backward compatibility across legacy interconnect chassis that adds to the development challenges.

Wireline interconnects using serial links have moved from being a niche application in high-speed network routers to now being used in a wide range of applications from high-speed microprocessors to data converters. To meet the integration requirements these serial links need to have lower power while the performance increases. Hence a typical figure of merit is to look at the energy per transmit/receive bit or pJ/bit, which is the same as the power in milliWatts (mW) to the datarate in gigabits per second (Gb/s) or mW/Gb/s.

The past five years have seen serial-link speeds increasing from 1Gb/s but the barrier appears to be approaching fast. Although 40Gb/s has been demonstrated many times in the lab, links at greater than 50Gb/s are conspicuously absent. Hence, although the system challenges require data bandwidth increasing at ~2× per year, the existing technology shows data rates increasing at about 2× every 5 years. At the same time, the need to support a variety of data channels including legacy compatibility with a very large number of parallel links means that equalization techniques are essential for robust data transmission. Two types of receiver equalization are linear equalization, which is used to boost the signals for shorter and less complex channels, and decision feedback equalization, which allows more complex channels with inter-channel crosstalk to be supported. However, these equalization techniques add to the power consumed by the links.

Figure 1 shows the energy efficiency per bit of equalizing receivers reported since 2007. State-of-the-art is around 0.5 pJ/b for these equalizers in the <20Gb/s range. However, at higher data rates the energy efficiency is still >1pJ/b. This years' publications show best-in-class performance in terms of data rate at 16 Gb/s at <0.5 pJ/b, showing the extension of low-power equalizers to higher data rates.

For a combined transmitter and receiver channel, the mW/Gb/s depends on the target application. For short-reach serial links, since the equalization is not as complex, achievable power numbers are of the order of 1mW/Gb/s to 5mW/Gb/s, with today's state-of-the-art power consumption for deployed 10Gb/s links typically between 10 and 50mW. For higher data rates in the 25-to-30Gb/s range, the efficiency is typically lower because of the additional clock and analog performance requirements imposed by the high data rate. State-of-the-art at these data rates is therefore in the 8-to-10mW/Gb/s range.

Long reach and more complex channels such as copper backplanes that include multiple connectors have much higher power consumption and lower efficiency in terms of mW/Gb/s. State-of-the-art published in this conference at 28Gb/s is 693mW for 35dB of channel loss.

These trends in integration, power consumption and applications bring new challenges to wireline communications. New techniques are required to ensure continued scaling of the links, and improvements in equalization techniques, transmitter design, receiver design, and clock distribution are essential. ISSCC 2012 will highlight many of these new techniques that continue to enhance the field.

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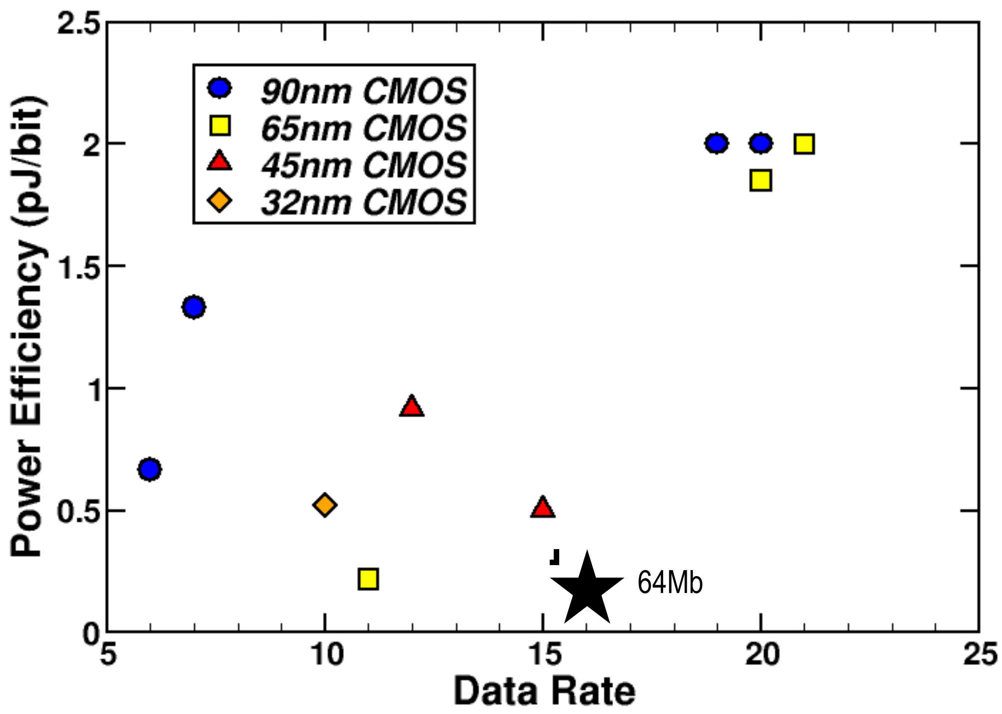

Figure 1 : Power efficiency of equalizing receiver.

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 59th appearance of ISSCC, on February 19th to the 23th, 2011, in San Francisco.

> This and other related topics will be discussed at length at ISSCC 2012, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 19-23, 2011, at the San Francisco Marriott Marquis Hotel.

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