ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2009 Executive Summary

- Activities
- Conference Theme
- Significant Results

EXECUTIVE SUMMARY

ACTIVITIES AT ISSCC 2009

Tutorials presented Sunday, February 8:

- **10** Independent lectures presented by experts from each of the ISSCC 2009 Program Subcommittees: Analog, Data Converters, High-Performance Digital, Imagers, MEMS, Medical and Displays, Low-Power Digital, Memory, RF, Technology Directions, Wireless, and Wireline.

Advanced-Circuit-Design Forums presented Sunday, February 8 and Thursday, February 12:

- Informal all-day interaction in which circuit experts exchange information on their current research.

Student Forum presented Sunday, February 8

- An opportunity for student networking, in which students present brief overviews on their current research.

Short Course presented Thursday, February 12:

- **4** linked 90-minute lectures given by experts in the field

Technical Paper Sessions presented Monday through Wednesday, February 9 to 11:

- **4** presentations in the Plenary Session on Monday morning
- **28** paper sessions beginning Monday afternoon and continuing through Wednesday afternoon
- **155** regular-length papers
- **48** short papers

Evening Sessions presented on Sunday, Monday and Tuesday evening

- **7** Special-Topic Sessions
- **2** Panel Sessions

Social Hour on Monday after paper sessions

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CONFERENCE THEME

ADAPTIVE CIRCUITS AND SYSTEMS

The ISSCC 2009 Conference theme is:

"Adaptive Circuits and Systems"

Technology scaling is enabling the integration of vast systems, encompassing billions of transistors on a single silicon chip. Along with the opportunities of integration, sub-50nm technologies present new challenges of device variability, reliability, and low voltage operation. Environmental constraints on power consumption and cooling are further complicating the design space. Adaptive circuits and systems offer the potential to dynamically optimize operating parameters such as performance and power. Contributions are encouraged from researchers and designers demonstrating novel adaptive circuits and system techniques in the subject areas including, but not limited to the following: digital and analog circuits, memory, imagers, wireless and wireline communications circuits.

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SIGNIFICANT RESULTS

Analog

- A chopper-stabilized current-feedback instrumentation amplifier with a 1mHz 1/f-noise corner and an AC-coupled ripple-reduction loop **[19.1]**
- A sub-1V bandgap voltage reference in 32nm FinFET technology **[19.6]**
- A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and 0.15ps_{rms} jitter in 0.18µm CMOS **[23.2]**
- Single-inductor dual-input dual-output buck-boost fuel-cell-Lithium-ion charging DC-DC converter supply **[26.2]**
- A 460W Class-D output stage with adaptive gate drive **[26.6]**

Data Converters

- The trend towards digital enhancement does not favor any one particular converter architecture. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- Migration down to deep-submicron technologies continues, allowing a more economical implementation of digital enhancement techniques. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- Oversampled converters show a distinct trend toward using continuous-time architectures. **[9.5 to 9.7]**

High-Performance Digital

- Highest ever transistor count (2.3B) for a microprocessor **[3.1]**
- Highest core count (8) and thread count (16) for an x86 processor **[3.1]**
- Reconfigurable memories offer architectural flexibility using a 3D-stacked system with fine-pitch micro-solder **[3.3]**
- Switched-capacitor methods can secure cryptographic engines from power-analysis attacks **[3.5]**
- Off-chip signaling techniques are integrated into on-chip wire drivers to improve bandwidth at low power **[3.6]**

IMMD

- The first backside-illuminated multi-layer 3D-integrated 1Mpixel CMOS image sensor that is four-side abuttable with only 3-pixel-equivalent seam loss and supports a burst digital data output rate of 1Mpixel in 1ms. **[2.1]**
- An image sensor whose random noise is 30% lower than previous CMOS image sensors with sensitivity doubled by a new column-level charge-addition mode. **[2.6]**
- A novel digital driving technique for mobile AMOLED displays using $\Delta\Sigma$ modulation mitigates TFT V_t-shifts and solves the false-contour problem. **[15.4]**
- The first bandgap-based temperature sensor at the 32nm node. **[20.1]**
- The first integrated electrode interface that combines electrical and chemical sensing, allowing researchers to explore the role of both modes of computation in the brain. **[25.2]**

Low-Power Digital

- The first fully-integrated backend SoC for Blu-ray players includes content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3. **[8.4]**
- The first Full-HD SoC available for handsets: 166MHz Mobile Application Processor is implemented in 65nm to support multistandard video codec at Full-HD resolution. **[8.7]**
- First non-coherent receiver allowing faster and lower-energy synchronization **[14.2]**
- First IC to achieve 4x4 64-QAM MIMO detection that is easily scalable to 256-QAM **[14.4]**

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Memory

- First 4Gb DDR3 highest-density DRAM at 1.2V power supply **[7.1]**
- First 8Gb through-silicon-via 4-stacked DDR3 with master/slave separate chips **[7.2]**
- Fastest-data-rate mobile DDR2 DRAM (4.3GB/s) **[7.3]**
- Fastest GDDR5 DRAM with a data rate of 7Gb/s/pin **[7.4]**
- First-reported 32Gb 34nm MLC NAND Flash Memory with 9MB/s write throughput **[13.1]**
- A 113mm^2 32Gb 3b/cell NAND memory that fits into a microSD memory card **[13.4]**
- First-reported 64Gb 4bit/cell Flash NAND memory with 5.6MB/s write throughput **[13.6]**
- The first 32nm high-density and high-performance SRAM in a Hi-k metal-gate technology **[27.1]**
- The 128Mb FeRAM is the largest-capacity in emerging nonvolatile RAM reported and 1.6GB/s bandwidth is 4 to 8× higher than previously reported **[27.5]**

RF

- A single-gate mixer topology with current reuse consumes just 380µW at 0.6V. **[12.5]**
- A 90nm CMOS power amplifier providing 23dBm with 12% power-added efficiency for a 16QAM WiMAX signal, enables long-range high-data low-cost single-chip communications **[22.3]**
- A demonstration of mm-wave power amplifiers at 60GHz to enable Gbit/s communications using low-cost state-of-the-art 65nm and 45nm CMOS at 1V. **[22.4; 22.5]**
- The highest-reported operating frequency (150GHz) for an amplifier in CMOS, enabling new applications from imaging to high-data-rate short-range communications **[29.1]**
- Record gain (26dB) reported for a 100GHz SiGe amplifier using a novel traveling-wave broadband topology **[29.3]**

Technology Directions

- A Spintronic-based oscillator with an operating range of 4GHz to 10GHz co-integrated with a broadband amplifier in 65nm for RF applications **[11.1]**
- 10Mb/s 14µW RFID with 14m operating range based on UWB uplink and UHF downlink in 0.18µm CMOS **[11.2]**
- A 2.5mW pulsed UWB wireless motion control system for a moth. **[11.3]**
- A self-sufficient tire-mounted wireless sensor integrates a Bulk Acoustic Wave-based low-power FSK 2.11GHz transceiver, an energy scavenger and a 3D vertical chip stack. **[17.1]**
- An implantable release-on-demand drug-delivery SoC in CMOS technology monolithically integrates wireless circuitry and 8 addressable 100nl reservoirs fabricated by CMOS-compatible post-IC processing. **[17.2]**
- A stabilized power supply system for low-power 3.3V electronics is realized by monolithically integrated micro fuel cell within an extended CMOS process. **[17.4]**
- A wireless power-transfer system for implanted medical devices uses an antenna area 100 times smaller than previous designs **[17.5]**
- Optical I/O architecture achieves data rate of 10Gb/s/channel at 11pJ/b energy efficiency. This technology projects increased optical integration that will reach 20Gb/s at 1pJ/bit**. [28.1]**
- Close-proximity inductive coupling data link between 3D-stacked 8-core processor and 1MB SRAM that achieves 19.2Gb/s and 1pJ/b. **[28.7]**

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Wireless

- The first multimode single-chip cellular transceivers for 2/2.5G and 3G **[6.2; 6.3; 6.4]**
- First published DOCSIS-3.0 SoC **[6.6]**
- Highest integration UWB WiMedia PHY in 65nm CMOS **[24.2]**
- First completely-integrated radio and baseband at 60GHz in CMOS **[18.5]**

Wireline

- A scalable 3.6-to-5.2mW 5-to-10Gb/s 4-tap DFE in 32nm CMOS **[10.1]**
- A 4-channel 10.3Gb/s backplane transceiver macro with 35dB equalizer and sign-based zero-forcing adaptive control **[10.5]**
- A 40Gb/s multi-data-rate CMOS transceiver with SFI-5 interface for optical transmission systems **[21.1]**
- An 80mW 40Gb/s 7-tap T/2-spaced FFE in 65nm CMOS **[21.4]**

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NOTES

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ISSCC 2009
Conference Overview

- Events
- Paper Statistics
- Plenary Session
- Technical Highlights
- Discussion Sessions
- Short Course
- Tutorials
- Advanced-Circuit-Design Forums

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 8, 2009)

- **10** 90-minute Tutorials, each taught twice, by circuit experts from the Program Committee, serve to meet attendees' needs for introductory material in circuit specialties.

ADVANCED-CIRCUIT-DESIGN FORUMS (SUNDAY, FEBRUARY 8, 2009)

- Circuit experts exchange information on their current research in an all-day informal environment

STUDENT FORUM (SUNDAY, FEBRUARY 8, 2009)

- An opportunity for student networking, in which students present brief overviews on their current research.

TECHNICAL SESSIONS (MON. TO WED., FEBRUARY 9 TO 11, 2009)

- **4 invited talks** presented in the Plenary Session and **203 technical papers** presented in **28** Regular Sessions, highlight the latest circuit developments.

EVENING SESSIONS (SUNDAY, MONDAY & TUESDAY, FEBRUARY8 TO 10, 2009)

- **7** Special-Topic presentations, in which experts provide insight and background on a subject of current importance.
- **2** Panels in which experts debate a selected topic and field audience questions in a semi-formal atmosphere.

SOCIAL HOUR (MONDAY, FEBRUARY 9, 2009)

- Network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; browse the technical-book exhibits!

SHORT COURSE (THURSDAY, FEBRUARY 12, 2009)

- Intensive All-Day Course on a single topic, taught by world-class instructors, can serve to "jump start" a change in an engineer's circuit specialty.

ADVANCED-CIRCUIT-DESIGN FORUM (THURSDAY, FEBRUARY 12, 2009)

- Circuit experts exchange information on their current research in an all-day informal environment.

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PAPER STATISTICS

OVERALL:

- **4** papers invited
- **582** papers submitted to ISSCC 2009
- **203** papers accepted, including:
  - **78** papers from North America, including
    - **31** Industry papers
    - **47** University papers
  - **73** papers from the Far East, including
    - **42** Industry papers
    - **31** University papers
  - **52** papers from Europe, including
    - **23** Industry papers
    - **29** University papers
- **29** Sessions, over 3 days

INTERNATIONAL SCOPE:

	2009	2008	2007
Americas:	**38 %**	**43 %**	**39 %**
Far East:	**36 %**	**28 %**	**31 %**
Europe:	**26 %**	**29 %**	**30 %**

WIDE COVERAGE:

	2009	2008	2007
Analog	**11 %**	**9 %**	**7%**
Data Converters	**7 %**	**10 %**	**7 %**
High-Performance Digital	**4 %**	**7 %**	**13 %**
Imagers, Displays, and MEMs	**12 %**	**11 %**	**12 %**
Low-Power Digital	**6 %**	**5 %**	**4 %**
Memory	**9 %**	**12 %**	**8 %**
RF	**11 %**	**11 %**	**10 %**
Technology Directions	**13 %**	**12 %**	**12 %**
Wireless Communications	**13 %**	**11 %**	**12 %**
Wireline Communications	**14 %**	**11 %**	**13 %**

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PLENARY SESSION

Paper 1.1:
Leaner and Greener: Adapting to a Changing Climate Innovation
René Penning de Vries, *CTO, NXP Semiconductors, Eindoven, The Netherlands*

- The semiconductor industry has been a major driver for change in everyday life.
- Energy efficiency and power management are now a major concern necessitating a new vision to meet the challenges of climate change and limited supplies.
- Solutions will depend on characteristics of particular energy sectors - consumer goods, workplace electronics, and transportation.
- For every 1% saved in the world's electricity consumption, roughly 40 fewer power stations are required!
- A new vision for semiconductor technology change is required.
- This presentation will explore how the semiconductor industry can go beyond the traditional to reduce energy demand in the modern world.

Paper 1.2:
Adaptive Circuits for the 0.5V Nanoscale CMOS Era
Kiyoo Itoh, *Fellow, Hitachi Tokyo, Japan*

- Nanoscale supply reduction leads to serious problems in circuit design.
- Problems originate through two unscalable parameters - the limit of V_t below which leakage begins to dominate, and the increase in variability of V_t with reduced nanoscale dimensions.
- Correspondingly, the minimum supply voltage begins to increase as feature size is reduced!
- This implies a 1V barrier at 45nm features sizes.
- For reducing nanoscale features interconnect resistance increases to provide more problems, which also motivate a higher supply voltage!
- A variety of techniques for the reduction of minimum supply voltage toward 0.5V will be presented.

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PLENARY SESSION

Paper 1.3:
The New Era of Scaling in an SoC World
Mark Bohr, *Senior Fellow, Intel, Hillsboro, OR*

- Simple scaling began to be troublesome earlier this decade.
- An new era of scaling began with innovations in device materials and transistor structure - copper, strained silicon, high-κ dielectrics and metal-gate transistors. .
- Scaling beyond the natural limits of lithography has led to major innovations - optical-proximity correction, phase-shift masks, and gridded layout.
- Analog circuits have particularly suffered in the nanometer era - degraded transistor gain, reduced dynamic range, and transistor mismatch.
- An adaptive-circuit approach must be employed for circuit improvement.
- These and other techniques for use down to 22nm will be discussed.

Paper 1.4:
Kids Today! Engineers Tomorrow!
John Cohn PhD, *Fellow, IBM Systems and Technology Group, Essex Junction, VT*

- A possible crisis exists in engineering education enrolment.
- World engineering-enrolment trends will be examined.
- What are we doing wrong? What do we need to do?
- How can we motivate kids?
- Grand global challenges to motivate young people.
- Your role as engineers in educating society about engineering.

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TECHNICAL HIGHLIGHTS

Analog

- A chopper-stabilized current-feedback instrumentation amplifier with a 1mHz 1/f-noise corner and an AC-coupled ripple-reduction loop **[19.1]**
- A sub-1V bandgap voltage reference in 32nm FinFET technology **[19.6]**
- A 1MHz-bandwidth type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications. **[23.1]**
- A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and $0.15ps_{rms}$ jitter in 0.18μm CMOS **[23.2]**
- Single-inductor dual-input dual-output buck-boost fuel-cell-Lithium-ion charging DC-DC converter supply **[26.2]**
- A 20W/channel Class-D amplifiers with zero common-mode radiated emissions **[26.4]**
- A 460W Class-D output stage with adaptive gate drive **[26.6]**

Data Converters

- Pushing the performance envelope with high-speed DACs: 2.9GS/s with high linearity (<-60dBc IM3) and wide bandwidth (1GHz). **[4.1]**
- Virtually all new data converters are digitally enhanced for performance improvement. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- The trend towards digital enhancement does not favor any one particular converter architecture. **[4.2 to 4.7, 9.1; 9.2; 9.5 to 9.8]**
- Medium-resolution converters, (8 to 10 bits), which are widely used, have migrated upward in speed of conversion. **[4.3; 4.5; 4.6]**
- Migration down to deep-submicron technologies continues, allowing a more economical implementation of digital enhancement techniques. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- Oversampled converters show a distinct trend toward using continuous-time architectures. **[9.5 to 9.7]**

High-Performance Digital

- High-performance processors continue to push performance and the limits of transistor integration **[3.1]**
- Highest ever transistor count (2.3B) for a microprocessor **[3.1]**
- Highest core count (8) and thread count (16) for an x86 processor **[3.1]**
- Novel technologies for power delivery and dissipation include optimized metal layers and microcontroller-based power management **[3.1; 3.2]**
- Reconfigurable memories offer architectural flexibility using a 3D-stacked system with fine-pitch micro-solder **[3.3]**
- Dynamic frequency switching enables power-frequency optimization within the allowed power envelope. **[3.4]**
- Switched-capacitor methods can secure cryptographic engines from power-analysis attacks **[3.5]**
- Off-chip signaling techniques are integrated into on-chip wire drivers to improve bandwidth at low power **[3.6]**

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IMMD

- The first backside-illuminated multi-layer 3D-integrated 1Mpixel CMOS image sensor that is four-side abuttable with only 3-pixel-equivalent seam loss and supports a burst digital data output rate of 1Mpixel in 1ms. **[2.1]**
- An image sensor whose random noise is 30% lower than previous CMOS image sensors with sensitivity doubled by a new column-level charge-addition mode. **[2.6]**
- A piecewise-linear 10b DAC architecture for AMLCD data drivers with drain-current modulation achieves good DNL and excellent channel-to-channel uniformity. **[15.1]**
- A novel digital driving technique for mobile AMOLED displays using $\Delta\Sigma$ modulation mitigates TFT V_t-shifts and solves the false-contour problem. **[15.4]**
- The first bandgap-based temperature sensor at the 32nm node. **[20.1]**
- An interface to a micro-gyroscope that minimizes area and reduces start-up time without compromising performance. **[20.3]**
- The first integrated electrode interface that combines electrical and chemical sensing, allowing researchers to explore the role of both modes of computation in the brain. **[25.2]**
- An integrated multiprocessor IC that extracts information from an array of neural signals for the identification of brain conditions such as epilepsy. **[25.4]**

Low-Power Digital

- The first fully-integrated backend SoC for Blu-ray players includes content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3. **[8.4]**
- A video-encoding chip supporting encoding of multiple views at HD solutions: 1-view (4096 x 2160p), 3-view full-HD (1080p), and 7-view HD (720p) for 3D display applications. **[8.5]**
- The first Full-HD SoC available for handsets: 166MHz Mobile Application Processor is implemented in 65nm to support multistandard video codec at Full-HD resolution. **[8.7]**
- A fully-integrated IR-UWB receiver for communication and sub-cm ranging **[14.1]**
- First non-coherent receiver allowing faster and lower-energy synchronization **[14.2]**
- First IC to achieve 4x4 64-QAM MIMO detection that is easily scalable to 256-QAM **[14.4]**

Memory

- First 4Gb DDR3 highest-density DRAM at 1.2V power supply **[7.1]**
- First 8Gb through-silicon-via 4-stacked DDR3 with master/slave separate chips **[7.2]**
- Fastest-data-rate mobile DDR2 DRAM (4.3GB/s) **[7.3]**
- Fastest GDDR5 DRAM with a data rate of 7Gb/s/pin **[7.4]**
- First-reported 32Gb 34nm MLC NAND Flash Memory with 9MB/s write throughput **[13.1]**
- A 113mm^2 32Gb 3b/cell NAND memory that fits into a microSD memory card **[13.4]**
- Use of inductive coupling for NAND Flash stacking in SSD with 2Gb/s and 15pJ/bit/chip capability **[13.5]**
- First-reported 64Gb 4bit/cell Flash NAND memory with 5.6MB/s write throughput **[13.6]**
- The first 32nm high-density and high-performance SRAM in a Hi-k metal-gate technology **[27.1]**
- The 128Mb FeRAM is the largest-capacity in emerging nonvolatile RAM reported and 1.6GB/s bandwidth is 4 to 8× higher than previously reported **[27.5]**

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RF

- A single-gate mixer topology with current reuse consumes just 380μW at 0.6V. **[12.5]**
- A novel technique to vastly reduce harmonic interference in direct-conversion receivers using an analog Walsh shaper **[12.7]** in the RF front-end with further interference cancelation in the digital domain. **[12.9]**
- An all-CMOS integrated transmitter realized with a power-mixer array in 0.13μm CMOS achieving 26dBm output power with 19% power-added efficiency for 16-QAM **[22.2]**
- A 90nm CMOS power amplifier providing 23dBm with 12% power-added efficiency for a 16QAM WiMAX signal, enables long-range high-data low-cost single-chip communications **[22.3]**
- A demonstration of mm-wave power amplifiers at 60GHz to enable Gbit/s communications using low-cost state-of-the-art 65nm and 45nm CMOS at 1V. **[22.4; 22.5]**
- The highest-reported operating frequency (150GHz) for an amplifier in CMOS, enabling new applications from im aging to high-data-rate short-range communications **[29.1]**
- Record gain (26dB) reported for a 100GHz SiGe amplifier using a novel traveling-wave broadband topology **[29.3]**

Technology Directions

- A Spintronic-based oscillator with an operating range of 4GHz to 10GHz co-integrated with a broadband amplifier in 65nm for RF applications **[11.1]**
- 10Mb/s 14μW RFID with 14m operating range based on UWB uplink and UHF downlink in 0.18μm CMOS **[11.2]**
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- A self-sufficient tire-mounted wireless sensor integrates a Bulk Acoustic Wave-based low-power FSK 2.11GHz transceiver, an energy scavenger and a 3D vertical chip stack. **[17.1]**
- An implantable release-on-demand drug-delivery SoC in CMOS technology monolithically integrates wireless circuitry and 8 addressable 100nl reservoirs fabricated by CMOS-compatible post-IC processing. **[17.2]**
- A stabilized power supply system for low-power 3.3V electronics is realized by monolithically integrated micro fuel cell within an extended CMOS process. **[17.4]**
- A wireless power-transfer system for implanted medical devices uses an antenna area 100 times smaller than previous designs **[17.5]**
- An optically-programmable SoC integrated on a 2.6x2.6mm^2 chip provides the electronics for an autonomous microrobot. **[17.9]**
- Optical I/O architecture achieves data rate of 10Gb/s/channel at 11pJ/b energy efficiency. This technology projects increased optical integration that will reach 20Gb/s at 1pJ/bit**. [28.1]**
- Stretchable circuit sheet using low-voltage CMOS organic technology that enables EMI-distribution measurement by wrapping the flexible surface around electronic equipment with a sensitivity of -70dBm**. [28.3]**
- A proof-of-concept application and methodology based on a cellular-neural-network- contour-generation vision system emulating the processing of part of the brain. **[28.6]**
- Close-proximity inductive coupling data link between 3D-stacked 8-core processor and 1MB SRAM that achieves 19.2Gb/s and 1pJ/b. **[28.7]**

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Wireless

- The first multimode single-chip cellular transceivers for 2/2.5G and 3G **[6.2; 6.3; 6.4]**
- First published DOCSIS-3.0 SoC **[6.6]**
- First completely-integrated radio and baseband at 60GHz in CMOS **[18.5]**
- Advances in 45nm CMOS for wireless connectivity **[24.1; 24.6]**
- Highest integration UWB WiMedia PHY in 65nm CMOS **[24.2]**

Wireline

- Subharmonically injection-locked PLLs for ultra-low-noise clock generation **[5.2]**
- A VDSL2 CPE AFE in 0.15µm CMOS with integrated line driver **[5.10]**
- A scalable 3.6-to-5.2mW 5-to-10Gb/s 4-tap DFE in 32nm CMOS **[10.1]**
- A 4-channel 10.3Gb/s backplane transceiver macro with 35dB equalizer and sign-based zero-forcing adaptive control **[10.5]**
- A 40Gb/s multi-data-rate CMOS transceiver with SFI-5 interface for optical transmission systems **[21.1]**
- An 80mW 40Gb/s 7-tap T/2-spaced FFE in 65nm CMOS **[21.4]**

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EVENING SESSIONS

SUNDAY

SE1: ***Healthy Radios: Radio & Microwave Devices for the Health Sciences***

SE2: ***Is Fabless MEMS Fabulous?***

MONDAY

SE3: ***Will ADCs Overtake Binary Frontends in Backplane Signaling?***

SE4: ***Highlights of IEDM 2008***

E1: ***Forewarned is Four Armed: Classic Analog Misteakes to Avoid***

SE5: ***Things all RFIC Designers Should Know (But are afraid to ask)***

TUESDAY

SE6: ***Interleaving ADC's – Exploiting the Parallelism***

SE7: ***Next-Generation Energy-Scavenging Systems***

E2: ***MID – 'Scaled Down' PC or 'Souped Up' Handheld?***

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SHORT COURSE:

[Thursday, February 12, 2009]

Low-Voltage Analog and Mixed-Signal CMOS Circuit Design

COURSE OBJECTIVE:

The relentless scaling of supply voltage that has accompanied advances in CMOS technology has been great for digital circuits but has made high-performance analog and mixed-signal circuits increasingly challenging to design. Nevertheless, market pressures continue to dictate high levels of integration in mass-market communication and entertainment devices to minimize product cost and size. Increasingly, this necessitates the inclusion of low-noise amplifiers, mixers, filters, and data converters, along with large amounts of digital circuitry in highly-scaled CMOS technology at analog supply voltages of 1.2V or less. Unfortunately, traditional topologies for these analog blocks are not compatible with such low supply voltages, so innovative new techniques for low-voltage analog and mixed-signal CMOS design are required. This short course provides a detailed view of the problems associated with low-voltage analog and mixed-signal design and describes techniques for overcoming these problems. It is intended for both entry-level and experienced analog and mixed-signal circuit designers.

OVERVIEW:

- The Short Course will be offered twice on Thursday, February 12:
  The first offering is scheduled for 8:00AM to 4:30PM.
  The second offering is scheduled for 10:00AM to 6:30PM.

- ***Low-Power Low-Voltage Opamp Design***
  Instructor: Willy Sansen
- ***Low-Voltage Sigma-Delta A/D Converters***
  Instructor: Lucien Breems
- ***The Effect of Technology Scaling on Power Dissipation in Analog CMOS Circuits***
  Instructor: Klaas Bult
- ***Sub-1V RF Design: Challenges and Techniques***
  Instructor: Behzad Razavi

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TUTORIALS:

[Sunday, February 8, 2009]

T1: Continuous-Time Filters

T2: Adaptive Power Management Techniques

T3: Turning Bits into Pictures

T4: Fundamentals of Digitally-Assisted RF

T5: Display and RFID-Tag Design Using Organic Transistors

T6: SAR ADCs

T7: Managing Variations Through Adaptive Design Techniques

T8: Variation-Tolerant SRAM Circuit Designs

T9: Managing Linearity in Radio Front-ends

T10: CMOS Circuit Techniques for High-Speed Wireline Transceivers

FORUMS:

[Sunday, February 8, 2009]

F1: SSD, Memory Subsystem Innovation

F2: Medical Image Sensors

F3: GIRAFE: Towards 4G RF Transceivers

F4: Ultra-Low-Voltage Circuit Design

[Thursday, February 12, 2009]

F5: ATAC: High-Speed Interfaces

F6: Multi-Domain Processors

F7: Clock Synthesis Design

F8: Integrated Neural Interfaces

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STUDENT FORUM

[Sunday , February 8, 2009]

After the successful launching of the ISSCC Student Forum last year, the International Solid-State Circuits Conference (ISSCC) will continue and expand this student activity at ISSCC 2009. One of the goals of the ISSCC Student Forum is to encourage student participation and networking at ISSCC. In particular, it will provide graduate students (Masters and PhD candidates) with:

- A great opportunity to showcase the directions of their work
- An opportunity to experience ISSCC quality
- An opportunity to interact with others in the ISSCC community
- Encouragement for future regular-paper submissions

More particularly, it will provide graduate students with:

- An opportunity for mutual understanding of academic research styles and cultures
- An opportunity to exchange experiences
- An opportunity to improve communication skills

The ISSCC Student Forum is organized as short presentations of work-in-progress. The presentations will NOT be considered as pre-publication in future ISSCC regular-paper submissions. Results with actual silicon implementation are highly encouraged. Papers that have been accepted at ISSCC will not be considered for the student forum presentation. However, papers that significantly extend a prior ISSCC publication will be considered.

STUDENT FORUM COMMITTEE

CHAIR:	**Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
VICE-CHAIR:	**Jan van der Spiegel,** *University of Pennsylvania,Philadelphia, PA*
VICE-CHAIR:	**Chorng-Kuang (C-K) Wang,** *National Taiwan University,Taipei, Taiwan*
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ANALOG SUBCOMMITTEE

- OVERVIEW
- FEATURED PAPERS
- EVENING SESSION
- PANEL
- TUTORIAL
- FORUM
  (co-sponsored by Analog, Data Converters, and RF)

ISSCC 2009 – ANALOG

Subcommittee Chair: ***Bill Redman-White,*** *NXP Semiconductors, Southampton, United Kingdom*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- A chopper-stabilized current-feedback instrumentation amplifier with a 1mHz 1/f-noise corner and an AC-coupled ripple-reduction loop **[19.1]**
- A sub-1V bandgap voltage reference in 32nm FinFET technology **[19.6]**
- A 1MHz-bandwidth type-I ΔΣ fractional-N synthesizer for WiMAX applications. **[23.1]**
- A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and $0.15ps_{rms}$ jitter in 0.18μm CMOS **[23.2]**
- Single-inductor dual-input dual-output buck-boost fuel-cell-Lithium-ion charging DC-DC converter supply **[26.2]**
- A 20W/channel Class-D amplifiers with zero common-mode radiated emissions **[26.4]**
- A 460W Class-D output stage with adaptive gate drive **[26.6]**

APPLICATIONS AND ECONOMIC IMPACT

- Ultra-low-noise-and-offset amplifier for precision-metrology manufacturing equipment **[19.1]**
- Demonstration of analog-circuit techniques in cutting-edge FinFET technologies **[19.6]**
- Elegant circuit architectures are enable the use of Type-I PLLs for high-purity carrier signals in wireless data transmission **[23.1]**
- A practical high-performance sampling phase detector enables simplified clock generation at high frequency **[23.2]**
- A micro-fuel-cell charger enables the use of smaller higher-density Lithium-ion batteries **[26.2]**
- Solving the EMI problem enables the use of highly efficient Class-D amplifier in more audio applications **[26.4]**
- Compact 460W audio amplifier with low EMI is integrated on SOI CMOS **[26.6]**

PANEL

Forewarned is Four-Armed; Classic Analog Misteaks to Avoid. **[E1]**

TUTORIAL

Continuous-Time Filters **[T1]**

FORUM

Clock Synthesis Design **[F7]**
(Co-sponsored by Analog, Data Converters and RF)

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Pushing Analog Amplification to Unprecedented Precision

A Chopper Current-Feedback Instrumentation Amplifier with a 1mHz 1/f Noise Corner and an AC-Coupled Ripple-Reduction Loop [19.1]

TU Delft

A 140dB-CMRR Current-Feedback Instrumentation Amplifier Employing Ping-Pong Auto-Zeroing and Chopping [19.2]

National Semiconductor

PRESENT STATE OF THE ART

- The errors in analog amplifiers, such as offset and 1/f noise, limit performance in ultra high precision metrology instrumentation.
- Chopping and auto-zeroing are proven techniques to address these errors, but are limited by significant ripple and noise-folding problems.

NOVEL CONTRIBUTIONS

- Continuous-time AC-coupled feedback loop drives the ripple down by 1100× to levels below the noise floor **[19.1]**
- Halving the chopping frequency and lowering the auto-zero loop bandwidth reduces noise folding, resulting in a 25× reduction of the noise power **[19.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Ultra-precise amplification enables precision mechatronics for manufacturing equipment such as wafer steppers **[19.1]**
- Low noise and high common-mode rejection (CMRR) enable the extraction of very-small analog sensor outputs such as from strain gauges and thermopiles in very-noisy industrial environments **[19.2]**

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Enhancements in Local-Oscillator Design Enable Next Generation Communication Systems

A 1MHz-Bandwidth Type-I ΔΣ Fractional-N Synthesizer for WiMAX Applications [23.1]

Arizona State University; Intel

A 2.2GHz 7.6mW Sub-Sampling PLL with -126dBc/Hz In-Band Phase Noise and 0.15ps_{rms} Jitter in 0.18µm CMOS [23.2]

University of Twente; National Semiconductor

PRESENT STATE OF THE ART

- ΔΣ PLLs are employed for fine frequency tune-ability in local-oscillator generation
- Type-II PLLs are most commonly used because the simplify the design of the phase detector
- The necessary dividers, for translating the VCO frequency to the reference frequency, typically add noise and are power-hungry
- Phase-detector nonlinearities create reference and ΔΣ spur problems
- DACs have been employed to correct spur sources

NOVEL CONTRIBUTIONS

- This wide-bandwidth low-power Type-I ΔΣ fractional-N synthesizer utilizes an inherently linear phase/frequency detector (PFD). **[23.1]**
- Discrete-time sample-and-hold loop filter and noise-cancelling charge-pump-DAC results in 100× reduction in quantization noise. **[23.1]**
- Using a sampling phase detector with a novel gain control eliminates the use of a divider. **[23.2]**
- Lower jitter and 4× lower in-band phase noise with 5× lower power **[23.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Higher-data-rate and higher-performance communications systems **[23.1]**
- Lower power and longer battery life in nomadic applications **[23.2]**

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Putting the BOOM in the Box!

A 20W/channel Class-D Amplifiers with Significantly Reduced Common-Mode Radiated Emissions [26.4]

Texas Instruments

A 460W Class-D Output Stage with Adaptive Gate Drive [26.6]

NXP Semiconductors

PRESENT STATE OF THE ART

- Class-D switching amplifiers are the most-efficient solution for high-power audio applications
- High efficiency allows amplifiers with hundreds of Watts of output power to be integrated in quarter-sized packages
- Ubiquitous adoption of switching amplifiers is limited due to generated electro-magnetic interference (EMI)

NOVEL CONTRIBUTIONS

- Smart-gate-drive control enables higher power and reduced EMI by eliminating overshoot voltages in the system **[26.6]**
- A practical 3-level modulation scheme delivers low EMI while maintaining high efficiency **[26.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Widespread adoption of Class-D in applications where reduced EMI is required **[26.4, 26.6]**
- More energy efficient systems **[26.4, 26.6]**
- Lighter smaller less-expensive and higher-quality audio systems **[26.4, 26.6]**

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Panel

Forewarned is Four-Armed: Classic Analog Misteakes to Avoid

Organizer: ***Jed Hurwitz,*** *Gigle Semiconductor, Edinburgh, United Kingdom*
Moderator: ***Chris Mangelsdorf,*** *Analog Devices, Tokyo, Japan*

OBJECTIVE

- To discuss why and how mistakes in analog IC design occur, and how they can be avoided.
- To provide examples from experience that the audience can learn from.
- To provide entertainment to encourage those who attend to remember the event and the motivation.

CHALLENGE

- Analog IC design is still seen by many as a black art, or at the very least, an area where experience counts. Why? Because experienced individuals avoid the traps, both the subtle and obvious mistakes that novices make.
- Timelines and costs of IC design are increasing as we go down to deep submicron technologies; There is a need to reduce the risk of implementing analog design.
- Our ultimate challenge is to get experts to share their experience in a light-hearted manner.

CONTROVERSY

- Not many conferences talk about mistakes. There is not a culture for this in this industry: It would be good to im prove this aspect of our culture.
- Not many people admit to mistakes, yet we all make them! The question is whether we learn by them.
- Even if we intend to create an entertaining evening, our topic is a serious one.

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Tutorial

Continuous-Time Filters

William Redman-White, *NXP Semiconductors and Southampton University UK*
(with input from Bram Nauta, University of Twente, Netherlands)

OVERVIEW

Filters are used everywhere in integrated systems. While it is true that precision filtering at low-to-moderate frequencies is best done in the digital domain, the need for continuous-time analog filters has not gone away. Anti-aliasing and reconstruction is always present even for moderate frequency signals, and at high frequencies, analog filters still offer advantages in power. With pressure on the curriculum in all universities, there is less coverage of filter techniques in EE courses, and engineers must pick up the tools on the job. This tutorial aims to lay out the groundwork theory and illustrate the mainstream strategies for integrated continuous-time filters. Topics to be covered include:

- Filter applications and system demands
- Filter specifications and approximations
- Filter realizations and topologies: single-amplifier, biquad, leapfrog
- Integrated implementations: opamp-RC, g_m-C
- Tuning strategies: variable elements, digital tuning

SPEAKER BIOGRAPHY

Bill Redman-White is currently a fellow with NXP Semiconductors, UK. He has also worked in France and California on optical storage, cellular radio, WLAN, digital audio, TV, and satellite baseband. He was previously with Motorola Geneva, GEC Marconi, and British Telecom, UK. Concurrently with NXP, he is also a Professor at Southampton University undertaking teaching and research in analog, RF, and SOI CMOS.

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DESIGN FORUM

Clock Synthesis Design

OBJECTIVE

One of the most critical and challenging functions present in almost every electronic system is clock generation or frequency synthesis. High-performance clocks or precise frequency references are needed in digital systems, data converters, serial data communications and wireless transceivers, to just name a few examples. Wireless systems heavily rely on the phase-locked-loop, but recent shifts into nanometer CMOS processes for RF SoCs open new architectural opportunities for all-digital and digitally-intensive implementations, both for carrier frequency synthesis and for phase-modulated transmission schemes. Data converter performance has improved so much that ADC performance is now limited as much by the clock-path noise and jitter, as by the quantization or thermal noise of the input signal path. That, of course, has led into new challenges for clock-generation systems with sub-ps or even sub-100fs rms jitter performance. The objective of this Forum is to present an overview of recent state-of-the-art developments in this crucial field, by leading experts.

AUDIENCE

Attendance is limited, and pre-registration is required. This all-day Forum encourages open information exchange. The targeted participants are circuit designers and system engineers who need to learn how the latest advances in high-performance clock generation and frequency synthesis will impact their future designs.

SCOPE

Clock-generation building blocks, such as phase-locked loops (PLL), have been around for many decades, and still form the core of most frequency-synthesis solutions. Increased performance and functionality requirements are driving significant innovations to the basic PLL structure and implementation. Continued scaling of semiconductor devices is further leading toward more digital-oriented realizations with significant circuit and architectural innovations. This Forum will present recent developments in frequency synthesis and clock generation by leading experts in this field.

PROGRAM

The Forum will begin with two talks that describe advanced techniques for the design of fractional-N PLLs that allow phase modulation and accurate methods for spur and noise suppression. Ian Galton (UCSD) will discuss phase-noise cancellation and fast calibration techniques for use in wireless communication systems. Satoshi Tanaka (Renesas) also shows loop calibration methods, aiming for two-point modulation schemes for transmitters.

The next three talks will focus on all-digital PLLs, focusing on critical building-block implementations as well as on full system performance for wireless-communication applications. Mike Perrot (SiTime) will show novel time-to-digital converter (TDC) structures that achieve sub-ps resolution, and PLL implementations exploiting that feature. Francesco Svelto (University of Pavia) focuses on the impact of TDC non-idealities on in-band spurious performance and the appropriate mitigation techniques. Recent trends in requirements and architectures for wireless systems will be covered by Bogdan Staszewski (Texas Instruments). The last two presentations will cover the challenge of low-jitter clock generation for data-converter applications. Robert Neff (Agilent Technologies) will discuss clock architectures for GS/s time-interleaved ADCs that require sub-ps rms jitter and calibrated timings. Finally, Ahmed Ali (Analog Devices) will show methods to analyze and simulate sub-100 fs jitter clocks for high-resolution high-speed ADCs, including an implementation reaching that target.

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NOTES

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Data Converters Subcommittee

- Overview
- Featured Papers
- Panel
- Special-Topic Session
- Tutorial
- Forum
  (co-sponsored by Analog, Data Converters, and RF)
- Trends

ISSCC 2009 – DATA CONVERTERS

Subcommittee Chair: *Venu Gopinathan, Ayusys, Bangalore, India*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Pushing the performance envelope with high-speed DACs: 2.9GS/s with high linearity (<-60dBc IM3) and wide bandwidth (1GHz). **[4.1]**
- Virtually all new data converters are digitally enhanced for performance improvement. **[4.2 to 4.7, 9.1, 9.2, 9.5 to 9.8]**
- The trend towards digital enhancement does not favor any one particular converter architecture. **[4.2 to 4.7, 9.1, 9.2, 9.5 to 9.8]**
- Medium-resolution converters, (8 to 10 bits), which are widely used, have migrated upward in speed of conversion. **[4.3, 4.5, 4.6]**
- Migration down to deep-submicron technologies continues, allowing a more economical implementation of digital enhancement techniques. **[4.2 to 4.7, 9.1, 9.2, 9.5 to 9.8]**
- Oversampled converters show a distinct trend toward using continuous-time architectures. **[9.5 to 9.7]**

APPLICATIONS AND ECONOMIC IMPACT

- Very-high-speed ADCs and DACs are being applied to a variety of broadband communication applications including cellular communication systems, UWB, WPAN, and wireline communication, as well as high-speed data acquisition. **[4.1 to 4.7]**
- Power consumption is being further reduced by using new approaches, such as a capacitive charge-pump combined with a source follower which allows for the elimination of amplifiers, or by using asynchronous conversion. **[9.2, 9.5]**
- Some new conversion techniques which have emerged during the past few years are now developing into more mature forms. **[9.3, 9.4]**

SPECIAL-TOPIC SESSION

Interleaving ADCs - Exploiting the Parellelism [SE6]
Several circuit solutions and calibration techniques are explored in this Session, reviewing the merits of the interleaving ADC architecture.

TUTORIAL

SAR ADCs [T6]
Opampless low-power ADC architectures are gaining importance in scaled CMOS technologies. Successive-approximation-register (SAR) ADCs exploit this concept. This Tutorial will cover the basics of this architecture along with recent very-high-efficiency implementations.

FORUM

Clock Synthesis Design (Co-organized by Analog, Data Converters and RF) [F7]
This Forum will present recent developments in frequency synthesis and clock generation by leading experts in this field.

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Expanding the Bandwidth-Resolution Product

A 12b 2.9GS/s DAC with IM3 <-60dBc Beyond 1GHz in 65nm CMOS [4.1]

Broadcom

A16b 125MS/s 385mW 78.7dB SNR CMOS Pipeline ADC [4.7]

Analog Devices

PRESENT STATE OF THE ART (THE PROBLEM)

- The Shannon theorem teaches that the channel capacity is determined by speed and resolution. Whereas last year's converters concentrated on lowering power, this year gives another push toward achieving high speed and high resolution at the same time.
- For high-speed / high-resolution applications, high linearity is a key issue. Otherwise mixing products would significantly lower the achievable SNDR. The key parameters that characterize linearity at high speed are THD (Total Harmonic Distortion), IM (Inter Modulation), and SFDR (Spurious-Free Dynamic Range). Consequently the featured designs try to improve these characteristics.
- For large-scale integration, a standard CMOS process is mandatory. Compared to bipolar or Si-Ge processes even more emphasis on thorough design techniques is necessary, a reality which will be disclosed in the contents of these papers.

NOVEL CONTRIBUTIONS

- Thorough analog design enables both high speed and high resolution in standard CMOS processes. **[4.1, 4.7]**
- Calibration techniques give another push to expanding the speed-resolution product. **[4.2, 4.3, 4.5, 4.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Whereas it is obvious that faster data converters enable higher conversion speeds, it is also crucial to maintain the low-frequency performance over the whole band of interest. This enables digital pre- and post-processing to enhance communication quality.
- This year's Conference demonstrates advanced calibration algorithms. While they promise a move toward increased performance, they are still not completely integrated. Bringing these algorithms into silicon will allow for power and cost-efficient SoC integration enabling further extensions in communication standards.

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Analog-to-Digital Converters Exploit Advantages in CMOS Technology

A 130mW 100MS/s Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction [9.1]

University of California, San Diego

A 0.13μm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer [9.5]

Massachusetts Institute of Technology

PRESENT STATE OF THE ART (THE PROBLEM)

- The low intrinsic gain of sub-100-nm CMOS makes it difficult to design amplifiers with sufficient open-loop gain for high-resolution applications.
- High digital density and low energy per gate-transition allow much more sophisticated calibration techniques than were available in the past.
- Higher speed enables new architectures that trade time resolution for amplitude.

NOVEL CONTRIBUTIONS

- Digital background calibration used to compensate for nonlinearities. **[9.1]**
- The first implementation of such compensation on-chip and in the background. **[9.1]**
- High-resolution and low-power performance. **[9.1]**
- Conversion of amplitude to time using a VCO. Uses the integrating nature of the VCO phase for noise shaping, where the nonlinearity of the VCO transfer function is mitigated by putting the VCO inside a continuous-time DS feedback loop. **[9.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Nonlinear calibration is expected to become more widespread. The DSP circuitry scales with technology so that more complex algorithms can be implemented in small area with low power dissipation. **[9.1]**
- Converting amplitude information to the time domain is also a technique that is naturally aligned with CMOS scaling, and is expected to be more prevalent in future applications. **[9.5]**

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SPECIAL-TOPIC SESSION

Interleaving ADCs - Exploiting the Parallelism

Organizer: ***Raf Roovers,*** *NXP Semiconductors, Eindhoven, Netherlands*
Chair: ***Kong-Pang Pun,*** *Chinese University of Hong Kong, Hong Kong, China*

OVERVIEW

Why have interleaving ADCs become more and more popular in recent years? Are other ADC architectures running out of steam, such that interleaving ADCs will become the standard in the near future, just as multi-core microprocessors are replacing single core? In this Session, an overview of recent developments in interleaving ADCs is shown. Due to the shrinking area of a single converter, many slices can be integrated in parallel resulting in a new degree of freedom for ADC designers, one providing higher speeds, better efficiency, and more flexibility. In order to exploit the potential of interleaving, a number of issues have to be solved related to the sampling and the matching of the different slices. Several circuit solutions and calibration techniques are explored in this Session, reviewing the merits of the interleaving ADC architecture.

OBJECTIVE

- Since time-interleaved analog-to-digital converters (ADC) might soon become a dominating ADC architecture, as they exploit the parallelism offered by modern IC technologies, the objective is to discuss the main challenges in interleaved ADCs.
- To present solutions to the time interleaving challenges, and to look into the future.

CHALLENGE

- How to solve the problems of gain, offset, timing, and bandwidth mismatches between parallel ADCs.
- How to build wide-bandwidth samplers.

STRUCTURE

- "Time-Interleaved Analog-to-Digital converters: an Algorithmic Melting Pot," by Kostas Doris (NXP Semiconductors)
- "Ultra-High-Speed Calibrated Time-Interleaved ADCs," by Pier Andrea Francese (National Semiconductor)
- "Blind Identification Solves the Interleaving Problem," by Jan-Erik Eklund (SP Devices)
- "Time-Interleaved ADCs, Past and Future," by Ken Poulton (Agilent Laboratories)

RECAP

- Four experts in the converter area will share their insights on various tradeoffs, advantages, and disadvantages of time-interleaving ADCs, and will present their solutions to the problems that arise from time-interleaving.

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TUTORIAL

SAR ADCs

Andrea Baschirotto, *University of Milano-Bicocca, Milano, Italy*

OVERVIEW

For a long time, Successive-Approximation-Register (SAR) ADCs have been the standard architecture for very-low-power applications. Recently, in scaled CMOS technologies, transistors feature higher speed but lower gain. In this scenario, ADC topologies have to be re-evaluated in consideration of their performance sensitivity with decreasing opamp gain. Thus, alternative ADC topologies, which are able to trade higher operation speed for low opamp-gain sensitivity, have to be developed. SAR topologies are a very good option, since in several SAR algorithm implementation schemes an opamp is not necessary. This reduces the performance sensitivity to the dc-gain reduction. For this reason, in recent years, SAR-ADCs have become the subject of a lot of research activity, and new solutions improving the SAR-ADC performance have been produced.

In this Tutorial, the basic concepts of SAR-ADC are presented, the most popular implementations are addressed (Charge redistribution, Resistive DAC, Charge sharing, etc…), the recent developments, which allow SAR-ADCs to become the record breaker in the ADC Figure-of-Merit race, are introduced (Redundancy, Comparator noise tolerance, etc…).

SPEAKER BIOGRAPHY

Andrea Baschirotto is an Associate Professor at University of Milano-Bicocca (Italy). His main research interests are in the design of mixed analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He participated in several research collaborations (coordinating some of them), funded by National and European projects. He has collaborated with several companies on the design of mixed-signal ASICs. He has (co)-authored more than 190 papers in international journals and presentations at international conferences, 1 book, 6 book chapters, and holds 29 US patents. Baschirotto has been Associate Editor for the IEEE Transactions on Circuits & Systems (Part II), and for the IEEE Transactions on Circuits & Systems (Part I). He has been the Technical Program Committee Chairman for ESSCIRC 2002. Andrea Baschirotto is a Senior Member of the IEEE. He has served on the ISSCC Data-Converter Program Subcommittee since 2005 and ESSCIRC TPC since 2001. He was the co-recipient of the ESSCIRC2006 Best Paper Award.

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FORUM

Clock Synthesis Design

OBJECTIVE

One of the most critical and challenging functions present in almost every electronic system is clock generation or frequency synthesis. High-performance clocks or precise frequency references are needed in digital systems, data converters, serial data communications and wireless transceivers, to just name a few examples. Wireless systems heavily rely on the phase-locked-loop, but recent shifts into nanometer CMOS processes for RF SoCs open new architectural opportunities for all-digital and digitally-intensive implementations, both for carrier frequency synthesis and for phase-modulated transmission schemes. Data converter performance has improved so much that ADC performance is now limited as much by the clock-path noise and jitter, as by the quantization or thermal noise of the input signal path. That, of course, has led into new challenges for clock-generation systems with sub-ps or even sub-100fs rms jitter performance. The objective of this Forum is to present an overview of recent state-of-the-art developments in this crucial field, by leading experts.

AUDIENCE

Attendance is limited, and pre-registration is required. This all-day Forum encourages open information exchange. The targeted participants are circuit designers and system engineers who need to learn how the latest advances in high-performance clock generation and frequency synthesis will impact their future designs.

SCOPE

Clock-generation building blocks, such as phase-locked loops (PLL), have been around for many decades, and still form the core of most frequency-synthesis solutions. Increased performance and functionality requirements are driving significant innovations to the basic PLL structure and implementation. Continued scaling of semiconductor devices is further leading toward more digital-oriented realizations with significant circuit and architectural innovations. This Forum will present recent developments in frequency synthesis and clock generation by leading experts in this field.

PROGRAM

The Forum will begin with two talks that describe advanced techniques for the design of fractional-N PLLs that allow phase modulation and accurate methods for spur and noise suppression. Ian Galton (UCSD) will discuss phase-noise cancellation and fast calibration techniques for use in wireless communication systems. Satoshi Tanaka (Renesas) also shows loop calibration methods, aiming for two-point modulation schemes for transmitters.

The next three talks will focus on all-digital PLLs, focusing on critical building-block implementations as well as on full system performance for wireless-communication applications. Mike Perrot (SiTime) will show novel time-to-digital converter (TDC) structures that achieve sub-ps resolution, and PLL implementations exploiting that feature. Francesco Svelto (University of Pavia) focuses on the impact of TDC non-idealities on in-band spurious performance and the appropriate mitigation techniques. Recent trends in requirements and architectures for wireless systems will be covered by Bogdan Staszewski (Texas Instruments). The last two presentations will cover the challenge of low-jitter clock generation for data-converter applications. Robert Neff (Agilent Technologies) will discuss clock architectures for GS/s time-interleaved ADCs that require sub-ps rms jitter and calibrated timings. Finally, Ahmed Ali (Analog Devices) will show methods to analyze and simulate sub-100 fs jitter clocks for high-resolution high-speed ADCs, including an implementation reaching that target.

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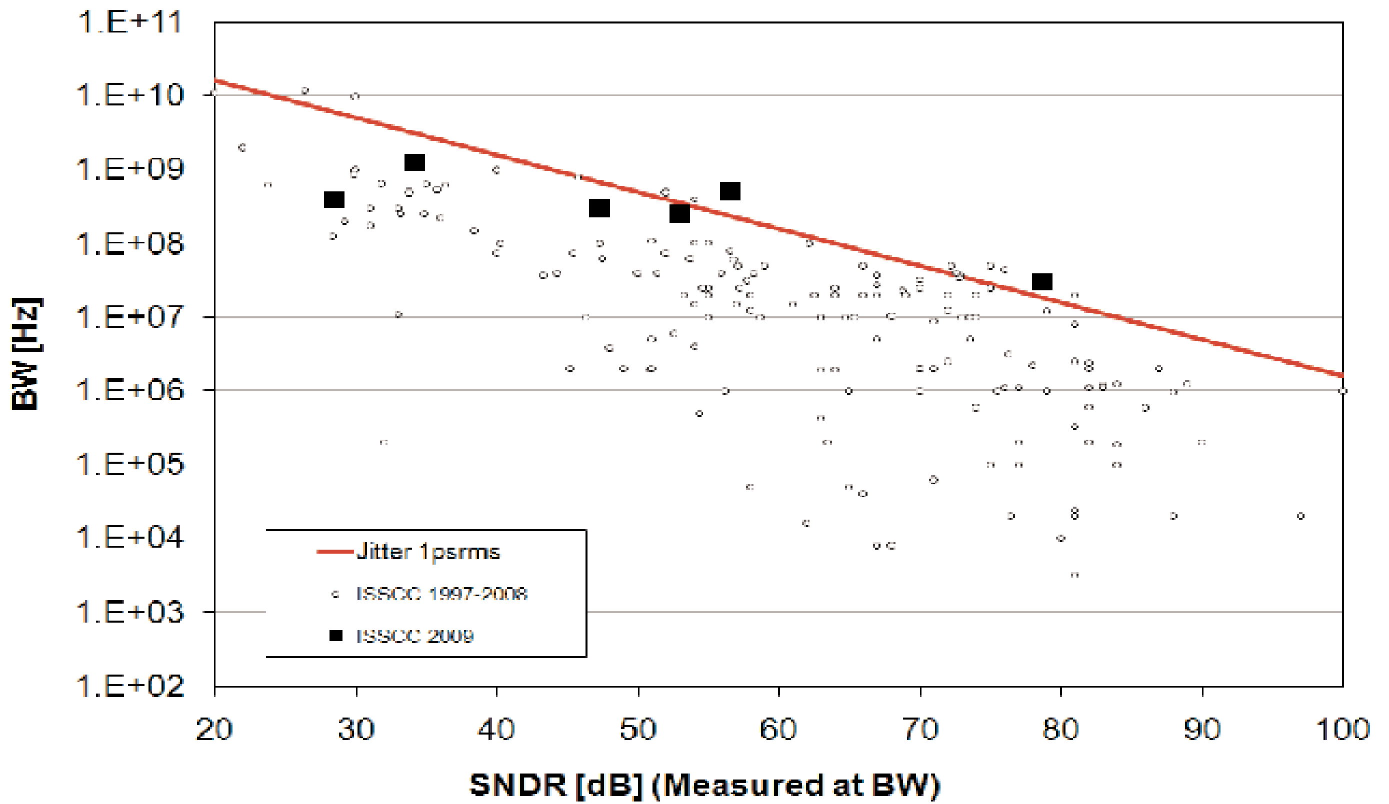
Trends in ADCs

The bandwidth and the signal-to-noise-and-distortion ratio (SNDR) of an ADC are two key performance metrics for ADCs. This year, designers have pushed both metrics to a whole new level, dramatically advancing data-conversion technology. The plot shows bandwidth versus SNDR. In general, there is a trade-off between these two metrics, as indicated by the straight line which corresponds to $1ps_{rms}$ aperture sampling jitter. The squares correspond to the performance of the papers presented in session 4. In particular, the work discussed on Paper 4.3 and 4.7 are represented by the two data points above the previously-mentioned $1ps_{rms}$ line.



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NOTES

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High-Performance Digital Subcommittee

- Overview
- Featured Papers
- Tutorial
- Forum
- Trend Charts

ISSCC 2009 – HIGH-PERFORMANCE DIGITAL

Subcommittee Chair: *Sam Naffziger, AMD, Fort Collins, CO*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- High-performance processors continue to push performance and the limits of transistor integration **[3.1]**
- Highest ever transistor count (2.3B) for a microprocessor **[3.1]**
- Highest core count (8) and thread count (16) for an x86 processor **[3.1]**
- Novel technologies for power delivery and dissipation include optimized metal layers and microcontroller-based power management **[3.1, 3.2]**
- Reconfigurable memories offer architectural flexibility using a 3D-stacked system with fine-pitch micro-solder **[3.3]**
- Dynamic frequency switching enables power-frequency optimization within the allowed power envelope. **[3.4]**
- Switched-capacitor methods can secure cryptographic engines from power-analysis attacks **[3.5]**
- Off-chip signaling techniques are integrated into on-chip wire drivers to improve bandwidth at low power **[3.6]**

APPLICATIONS AND ECONOMIC IMPACT

- High-performance systems continue to deliver performance improvements through higher levels of integration, high-speed source-synchronous I/O, optimized power delivery and management, and high-reliability techniques **[3.1, 3.2]**
- Fully integrated systems-on-a-chip can optimally separate memory from logic into two separate chips with the architectural flexibility of reconfigurable and networked memory tiles **[3.3]**
- Cryptographic engines that enable electronic commerce and data integrity can be made more secure against sophisticated power analysis attacks **[3.5]**
- On-chip networks can extend performance beyond conventional schemes by applying off-chip techniques to RC-dominated on-chip wires **[3.6]**

TUTORIAL

- Managing Variations Through Adaptive Design Techniques **[T7]**

FORUM

- Multi-Domain Processors **[F6]**

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Highly Integrated Processor Cores

A 45nm 8-Core Enterprise Xeon® Processor [3.1]

Intel

A Family of 45nm IA processors [3.2]

Intel

PRESENT STATE OF THE ART (THE PROBLEM)

- Computer-system performance is limited by off-chip communication, reliability, clocking, and power delivery.
- Continued progress in transistor scaling offers breakthrough levels of silicon integration

NOVEL CONTRIBUTIONS

- Highest transistor count (2.3B) ever reported in a microprocessor **[3.1]**
- Optimized source-synchronous high-speed serial I/O links for off-chip communication running at 6.4 GT/s **[3.1, 3.2]**
- Customized thick top-metal layer for power delivery and power gating **[3.1, 3.2]**
- Double error-correction and triple error-detection in data caches **[3.1, 3.2]**
- Microcontroller-based power management responds to environmental, operating, and workload conditions **[3.1, 3.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- The integration of dual-threaded cores and on-die large shared L3 caches (up to 24MB) continues industry trends in system integration **[3.1, 3.2]**
- Extended focus on power management to enable high-performance systems within a limiting thermal-power envelope **[3.1, 3.2]**
- Employment of point technologies, such as a 7μm-thick top-metal layer, to enable optimized power gating and distribution **[3.1, 3.2]**

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3D Integrated SRAM Lifts SoC Area and Latency Constraints

A Chip-Stacked Memory for On-Chip SRAM-rich SoCs and Processors [3.3]

NEC

PRESENT STATE OF THE ART (THE PROBLEM)

- SoCs need large integrated SRAM memories in functional blocks
- Integrating these memories within the blocks has area and latency overheads, and, in general makes inefficient use of memory resources—especially in the presence of processor cores and blocks that are either unused or asleep.
- Static allocations of memory to logic in such a 3D-integrated system limit performance gains across a wide range of applications.

NOVEL CONTRIBUTIONS

- Memory is placed on a separate die is stacked on top of SoC inside the package **[3.3]**
- High-density inter-chip electrodes replace micro-bumps (10μm pitch vs. 50μm pitch) **[3.3]**
- Latency is reduced due to the close memory proximity to IP core (using the 3D arrangement) **[3.3]**
- Memory arrays are reconfigurable in order to adaptively reallocate memory resources based on core needs **[3.3]**
- Reconfiguration scheme takes bandwidth requirements into account **[3.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Cheaper and more-power-efficient SoCs **[3.3]**
- Potential for more products and applications can be enabled from a single design due to reconfiguration capabilities **[3.3]**

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TUTORIAL

Managing Variations Through Adaptive Design Techniques

David Blaauw, *University of Michigan, Ann Arbor, MI*

OVERVIEW

CMOS technology scaling has given rise to increased sensitivity of design to process, voltage and temperature (PVT) variations, as well as to aging effects. These uncertainties have led to ever-larger design margins intended to ensure correct operation under all conditions which result in substantial performance and power losses. In this context, a new trend in adaptive design techniques has emerged where circuits are dynamically adjusted at runtime to compensate for PVT and aging effects. This Tutorial will review the sources of uncertainty and their classification, and describe techniques for dynamic compensation and adaptive control. Particular emphasis will be given to so-called canary circuits, PVT monitors, and adaptive voltage and frequency synthesis. The discussion will examine current industrial practice as well as highlighting future trends coming from industrial and academic research.

SPEAKER BIOGRAPHY

David Blaauw received his BS in Computer Science and Physics from Duke University and his Ph.D. in Computer Science from the University of Illinois, Urbana-Champaign. He worked for Motorola for 8 years as a manager in the Advanced Design Technology group. Since 2001, he has been on the faculty at the University of Michigan, Ann Arbor. His research interests include low power and high performance design. He has authored over 250 papers and holds 25 patents. He is a member of the ISSCC Technical Program Committee and has served as chair of the International Symposium on Low Power Electronic Design (ISLPED) and as an executive committee member of the Design Automation Conference.

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MICROPROCESSOR FORUM

Multi-Domain Processors

OBJECTIVE

Multiple clock and power domains are widely used to manage power in modern nanoscale designs. This Forum will present the latest design techniques in multiple-domain clock and power management for high-performance processors, as well as low-power systems-on-chip (SoC). Topics include clock and data synchronization, power gating, floorplan and layout implications, clock and power grids, test requirements, modular design techniques. Practical examples will be presented from both industry and academia.

AUDIENCE

This forum is intended for circuit designers and engineering students looking to understand the latest design techniques in multiple-domain clock and power management for high-performance processors and low power systems-on-chip (SoC).

SCOPE

Researchers from industry and academia will present an overview of multiple-domain clock and power design techniques, including examples from real implementations.

PROGRAM

The Forum starts with an introduction from **Stefan Rusu** (Intel) who will summarize the trends and challenges in using multiple clock and power domains in modern processors. **Phil Restle** (IBM) will discuss several practical implementations that illustrate how the strong desire for more power and clock domains must in practice be tempered with the realities of design complexity, finite wiring resources and the critical importance of high-quality power and clock distributions. **Stephen Kosonocky** (AMD) will focus on low V_{MIN} circuit design methods (like 8T SRAM cells), power gating techniques for high performance systems, on-die regulation for cache design, proper start-up power sequencing and voltage translation for signals between voltage planes. **Elad Alon** (UC Berkeley) will show that the slow adoption of multi-supply designs can largely be attributed to the impedance degradation caused by heavily partitioned package power planes and discuss possible approaches to alleviate these impedance concerns by using on-die noise suppression or active regulation to lower the impedance of each of the power grids. **Radu Marculescu** (CMU) will address the issue of energy optimization in multiprocessor systems-on-chip using voltage-frequency islands and a network-on-chip communication approach. A globally asynchronous, locally synchronous (GALS) design methodology is used to achieve low power consumption and design modularity. **Masayuki Ito** (Renesas) will present a multi-power domain implementation for a mobile WCDMA/GPRS processor. He will cover isolation techniques, layout topology examples, power-on rush current reduction, design flow for multi-power-domain and CAD tool support. **Rob Aitken** (ARM) will describe homogeneous and heterogeneous core systems, cache architectures and methods for voltage scaling. Silicon results for several design approaches at the 40nm node are compared and their implications for both hard and soft IP delivery are discussed. The forum concludes with a 40-minute question and answer session with all seven of the presenters in a panel format with an opportunity to discuss the proposed solutions. This all-day Forum encourages open exchange in a closed workshop. Attendance is limited and pre-registration is required. Coffee breaks and an in-room lunch will be provided, to allow a chance for participants to interact with the forum presenters.

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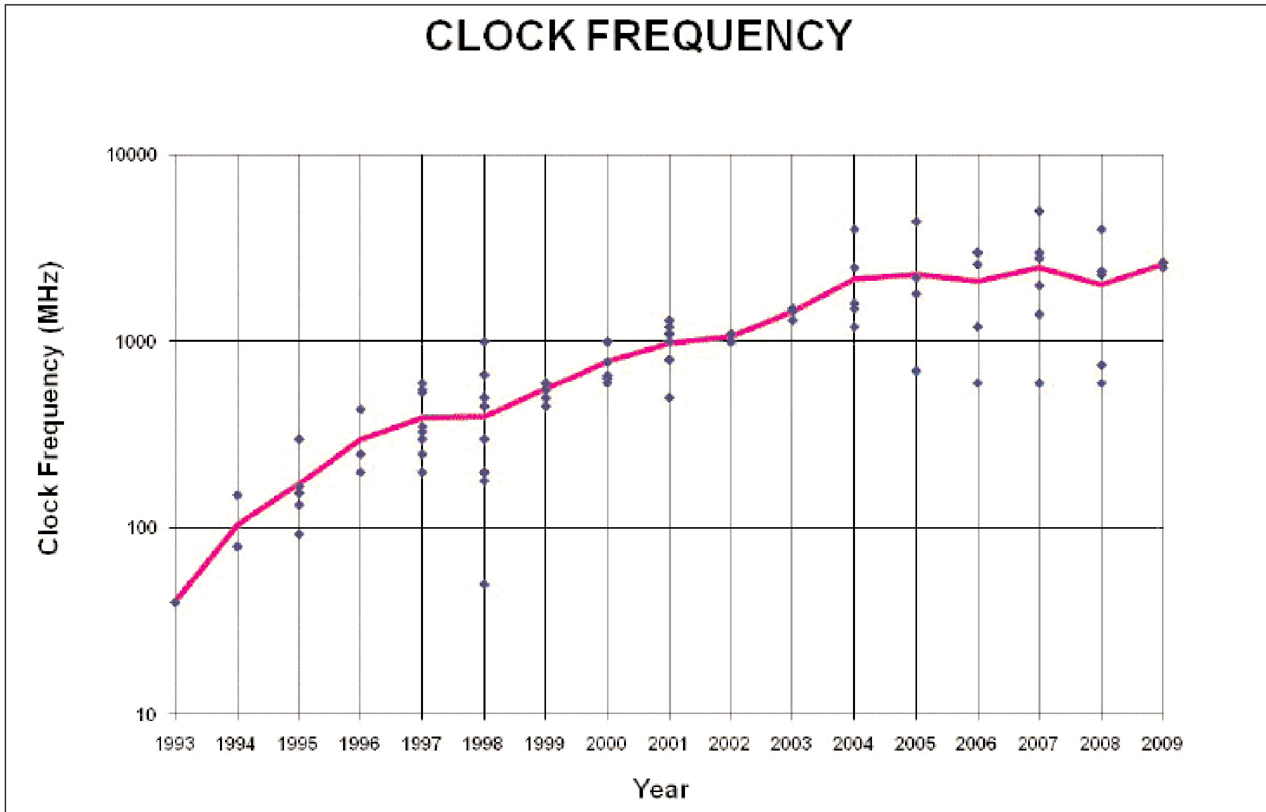

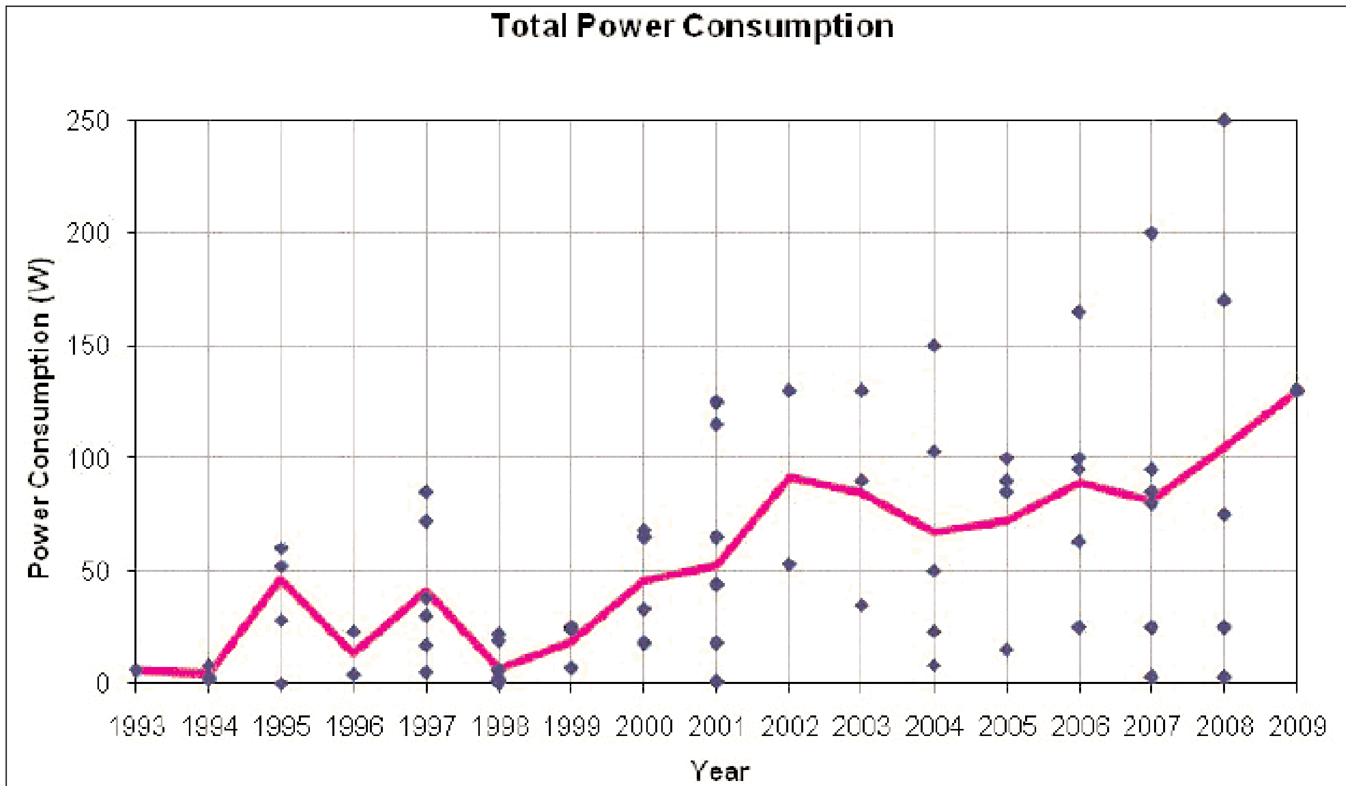

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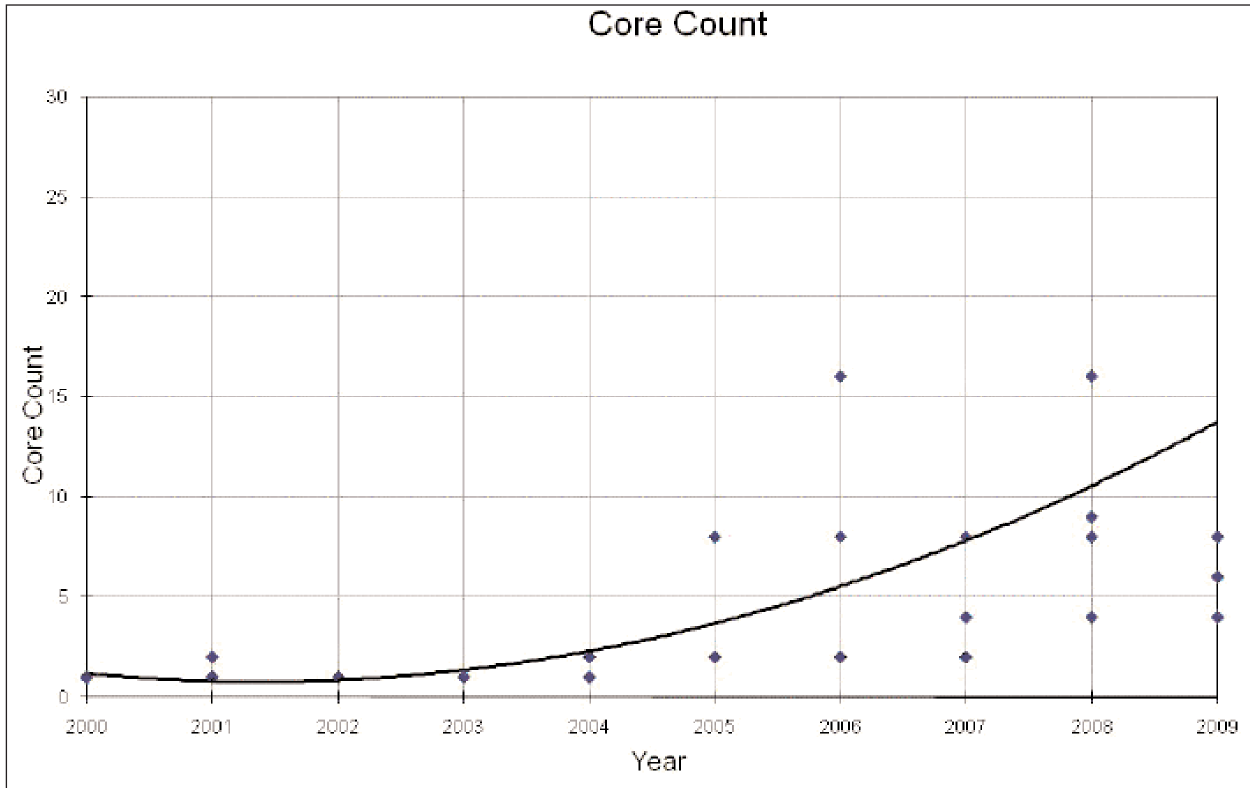

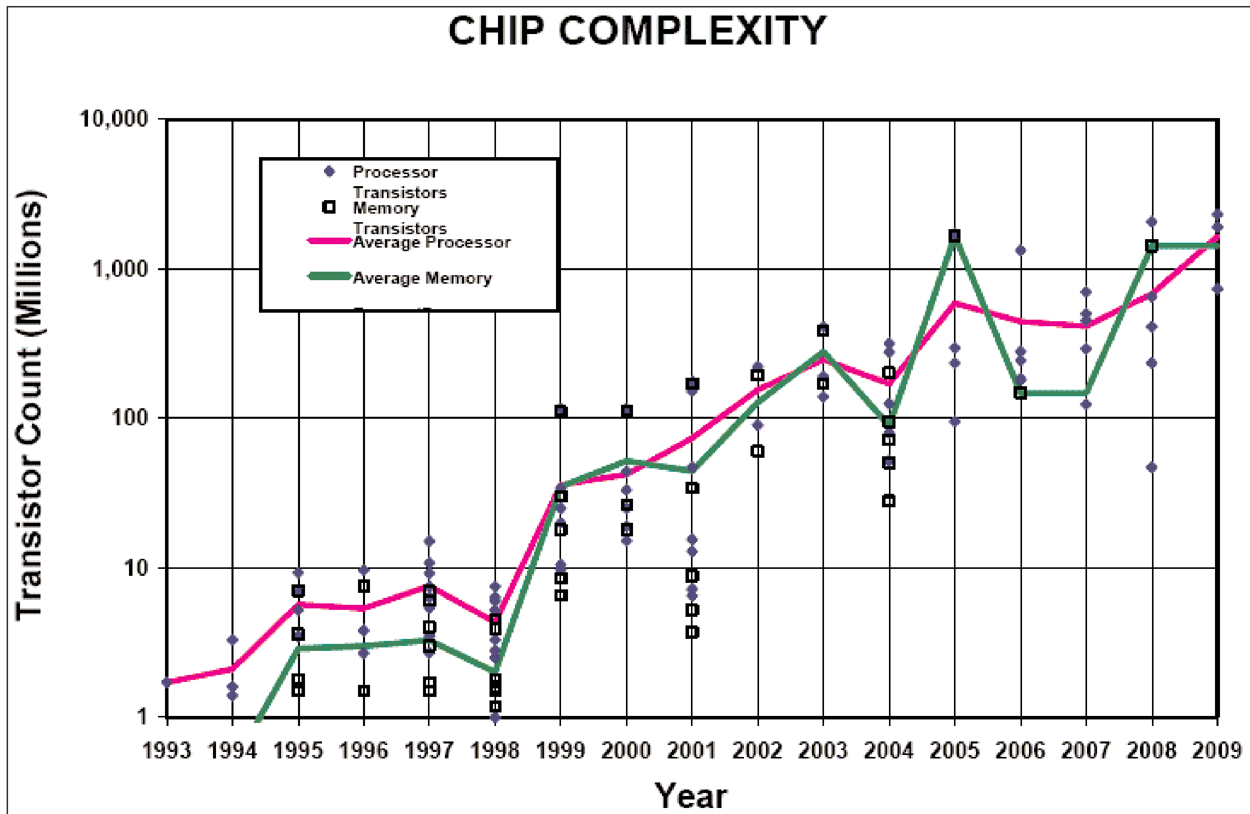

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NOTES

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Imagers, MEMS, Medical & Displays Subcommittee

- Overview
- Featured Papers
- Special-Topic Sessions
- Tutorial
- Forums
- Trends

ISSCC 2009 – IMAGERS, MEMS, MEDICAL & DISPLAYS

Subcommittee Chair: *R. Daniel McGrath, Eastman Kodak, Rochester, NY*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- The first backside-illuminated multi-layer 3D-integrated 1Mpixel CMOS image sensor that is four-side abuttable with only 3-pixel-equivalent seam loss and supports a burst digital data output rate of 1Mpixel in 1ms **[2.1]**
- An image sensor whose random noise is 30% lower than previous CMOS image sensors with sensitivity doubled by a new column-level charge-addition mode **[2.6]**
- A piecewise-linear 10b DAC architecture for AMLCD data drivers with drain-current modulation achieves good DNL and excellent channel-to-channel uniformity **[15.1]**
- A novel digital driving technique for mobile AMOLED displays using $\Delta\Sigma$ modulation mitigates TFT V_t-shifts and solves the false-contour problem **[15.4]**
- The first bandgap-based temperature sensor at the 32nm node **[20.1]**
- An interface to a micro-gyroscope that minimizes area and reduces start-up time without compromising performance **[20.3]**
- The first integrated electrode interface that combines electrical and chemical sensing, allowing researchers to explore the role of both modes of computation in the brain **[25.2]**
- An integrated multiprocessor IC that extracts information from an array of neural signals for the identification of brain conditions such as epilepsy **[25.4]**

APPLICATIONS AND ECONOMIC IMPACT

- Four-side-abuttable CMOS image sensors will enable ultra-large-format image sensors for scientific applications **[2.1]**
- Lower-noise CMOS image sensors will enable better video and still imaging in consumer digital still cameras, mobile phones, and camcorders **[2.6]**
- 10b AMLCD driver IC with small DAC area will enable lower-cost and higher-quality TVs for consumer applications **[15.1]**
- A novel digital driving method for mobile AMOLED displays will enable low-cost high-quality color displays for cell phones **[15.4]**
- On-chip local temperature sensors for thermal management are crucial elements of any microprocessor in advanced technologies beyond the 45nm node **[20.1]**
- Cost-reduction for integrated micro-gyroscopes is a key enabling factor for widespread application in consumer electronics **[20.3]**
- The combined measurement of electrical and chemical processes can help to develop new understanding of the origins of neurological disease, and lead to therapies such as deep-brain stimulation **[25.2]**
- The processing of neural waveforms with a power-efficient IC will help to bring neuroprosthetics and closed-loop therapeutic systems to market **[25.4]**

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SPECIAL-TOPIC SESSION

Is Fabless MEMS Fabulous? **[SE2]**
Highlights of IEDM 2008 **[SE4]**

TUTORIAL

Turning Bits into Pictures **[T3]**

FORUMS

Medical Image Sensors **[F2]**
Integrated Neural Interfaces **[F8]**

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3D-Stacked and Low-Noise Image Sensors

A 4-Side Tileable Back-Illuminated 3D-Integrated Mpixel CMOS Image Sensor [2.1]

MIT Lincoln Laboratory; Irvine Sensors; Forza Silicon

A 1/3.2-inch 3.3Mpixel CMOS Image Sensor with a Column-Signal-Addition Method Using a PMOS Column Amplifier [2.6]

Canon

PRESENT STATE OF THE ART (THE PROBLEM)

- Today's image sensors are fabricated using a standard 2D semiconductor process, which limits the amount of circuitry that can be implemented.
- Photodetectors and readout electronics must be implemented on the same size-constrained chip, which limits sensor performance.
- Shrinking pixel sizes limits the amount of light that can be collected by the photodetectors, and increases the sensor read noise.
- Small pixels have high noise and low sensitivity, which limit the signal-to-noise ratio of digital pictures.

NOVEL CONTRIBUTIONS

- The first backside-illuminated multi-layer 3D-integrated 1Mpixel CMOS image sensor that is four-side-abuttable with only 3 pixel-equivalent seam loss providing a burst digital data output rate of 1Mpixel in 1ms **[2.1]**
- An image sensor whose random noise is 30% lower than previous CMOS image sensors uses new column readout circuits. Sensitivity is doubled by a new column-level charge-addition mode **[2.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- 3D CMOS image sensors will enable lower-cost and higher-performance cameras for mobile imaging applications **[2.1]**
- Four-side-abuttable CMOS image sensors will enable ultra-large-format image sensors for scientific applications **[2.1]**
- Lower-noise CMOS image sensors will enable better video and still imaging in consumer digital still cameras, mobile phones, and camcorders **[2.6]**

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Display and Imager Electronics

A Digital Driving Technique for an 8b QVGA AMOLED Display Using ΔΣ Modulation [15.4]

Purdue University; LG Electronics

A Piecewise-Linear 10b DAC Architecture with Drain-Current Modulation for Compact AMLCD Driver ICs [15.1]

KAIST; Samsung Electronics

PRESENT STATE OF THE ART *(THE PROBLEM)*

- AMOLED displays suffer from V_t-shifts requiring compensation techniques for analog voltage drivers. Digital driving techniques can mitigate image degradation caused by V_t-shifts, but digital driving leads to false-contour noise. In order to address false-contour noise, a novel digital driving technique that does not increase the number of bit planes is required.
- Mobile displays using amorphous silicon (a-Si) backplanes have so far been limited to 6b color depth due to area constraints. The increasing demand for high-resolution mobile displays with more than 8b color depth on a-Si backplanes requires compact high-resolution DAC architectures.
- The demand for LCD TVs with multiple 10b data driver ICs is increasing. Compact 10b DACs with precise chip-to-chip matching are required to achieve highly-uniform image quality.

NOVEL CONTRIBUTIONS

- A piecewise-linear 10b DAC architecture for AMLCD data drivers with drain-current modulation achieves good DNL and excellent channel-to-channel uniformity **[15.1]**
- A compact linear 10b data-driver IC for mobile TFT-LCD displays **[15.2]**
- A novel digital driving technique for mobile AMOLED displays using ΔΣ modulation mitigates TFT V_t-shifts and solves the false-contour problem **[15.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- A 10b AMLCD-driver IC with small DAC area will enable lower-cost and higher-quality TVs for consumer applications **[15.1]**
- A novel digital driving method for mobile AMOLED display will enable low-cost high-quality color displays for cellphones **[15.4]**

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Sensors & MEMS

A 1.05V 1.6mW 0.45°C 3σ-Resolution ΔΣ-Based Temperature Sensor with Parasitic-Resistance Compensation in 32nm CMOS [20.1]

Intel

An Interface for a 300°/s Capacitive 2-axis Micro-Gyroscope with Pseudo-CT Readout [20.3]

Helsinki University of Technology; ELMOS Semiconductor

PRESENT STATE OF THE ART (THE PROBLEM)

- The standard (bandgap-based) way of measuring temperature on-chip exploits the temperature dependence of a pn-junction. Scaling of these sensors to more advanced technologies is commonly believed to be difficult, because of reduced supply voltage and increased leakage currents **[20.1]**
- Thermal management on microprocessors requires small integrated temperature-sensors with a resolution of better than 1ºC **[20.1]**
- Present interface circuits for capacitive microgyroscopes suffer from limited performance, long start-up times, and large silicon area **[20.3]**

NOVEL CONTRIBUTIONS

- First bandgap-based temperature sensor at the 32nm node **[20.1]**
- Novel techniques address scaling issues **[20.1]**
- An interface to a micro-gyroscope that minimizes area and reduces start-up time without compromising performance **[20.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- On-chip local temperature sensors for thermal management are a crucial component of any new microprocessor in advanced technologies beyond the 45nm node **[20.1]**
- Cost-reduction for integrated micro-gyroscopes is a key enabling factor for widespread application in consumer electronics **[20.3]**

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Medical

A Wireless IC for Time-Share Chemical and Electrical Neural Recording [25.2]

Case Western Reserve University; Illinois State University

A Biomedical Multiprocessor SoC for Closed-Loop Neuroprosthetic Applications [25.4]

National Taiwan University; University of California, Santa Cruz

PRESENT STATE OF THE ART (THE PROBLEM)

- The brain uses both electrical and chemical signal transduction to perform signal processing and computation.
- Most modern sensing methods focus on electrical sensing, missing out on the chemical signals that are present, and ignoring their role in computation.
- Decoding neural signals is a difficult problem, which makes it hard to build feedback loops and algorithms for neuroprosthetics, closed-loop epilepsy correction, and other neurological systems.

NOVEL CONTRIBUTIONS

- The first integrated electrode interface that combines electrical and chemical sensing, allowing researchers to explore the role of both modes of computation in the brain **[25.2]**
- An integrated multiprocessor IC that extracts information from an array of neural signals for the identification of brain conditions such as epilepsy **[25.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- The combined measurement of electrical and chemical processes will help elucidate the fundamental processing of neural circuits. This could help to develop new understanding of the origins of neurological disease, and in turn, develop improved therapies such as deep-brain stimulation. **[25.2]**
- The processing of neural codes with a power-efficient IC could help to bring neuroprosthetics and closed-loop therapeutic systems to market faster. **[25.4]**

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SPECIAL-TOPIC SESSION

Is Fabless MEMS Fabulous?

Organizer: ***Farrokh Ayazi,*** *Georgia Institute of Technology, Atlanta, GA*
Moderator: ***Christoph Hagleitner,*** *IBM, Rüschlikon, Switzerland*

OBJECTIVE

- To discuss the pros and cons of being a fabless MEMS company.
- To understand and discuss the maturity level of pure-play MEMS foundries.
- To debate whether today's MEMS are low-cost enough to compete and survive in consumer markets.

CHALLENGE

- How can the cost of MEMS manufacturing and calibration be reduced?
- Given the smaller mask count and larger feature sizes of micromechanical devices, can MEMS die cost become less than basic CMOS die cost?
- Currently MEMS processes are customized for each device, preventing standardization.
- Lack of a generic process flow that can address 80-to-90% of the MEMS market.
- Success stories are sparse amongst MEMS start-ups.
- Process intellectual property (IP) issues.

CONTROVERSY

- Is fabless a viable business model for MEMS start-ups or is in-house fab a necessity?
- MEMS foundries are growing, but the shipping volumes are not high.
- Are major MEMS manufacturers going to outsource their MEMS fabrication or expand their internal foundry capability?
- What are the killer applications that will make pure-play MEMS foundries flourish?

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SPECIAL-TOPIC SESSION

Highlights of IEDM 2008

Organizer: ***Roland Thewes,*** *Qimonda, Munich, Germany*
Chair: ***Ralf Brederlow,*** *Texas Instruments, Freising, Germany*

OVERVIEW

- The design of high-performance circuitry and entire systems requires access to related devices, technologies, and (last but not least) adequate packaging and assembly solutions. To gain maximum system performance, technology developers need to understand the needs of the design community. As well, circuit designers must be aware of what technology is capable of achieving and has to offer, but also understand where physical, manufacturing-related, or cost-related challenges arise.
- In this Session, four outstanding papers from IEDM 2008 are presented to the ISSCC design community. They cover several areas. These include advanced CMOS platforms with 32nm design rules that enable high performance as well as low-power operation; recent achievements in multi-chip module assembly techniques that allow the combination of various technologies and functionalities; and ultra-high-frequency RF transistors that open the way to THz applications.

OBJECTIVE

- To give an overview of the latest achievements within the area of devices and technologies that enable increased circuit and system performance.

CHALLENGES

- To understand options and restrictions presented by future CMOS platforms.
- To understand and handle transistor behaviors in the THz regime.
- To understand how to efficiently merge various devices and technologies, that cannot easily be integrated into CMOS, within one module, as a means of providing novel or increased functionality.

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TUTORIAL

Turning Bits into Pictures

Ian Underwood, *University of Edinburgh, Edinburgh, United Kingdom*

OVERVIEW

Electronic displays are deployed in a variety of applications, each of which prioritizes particular performance criteria (e.g. image quality, size, definition, brightness) whilst imposing its own constraints (e.g. cost, power, robustness). The performance criteria must be met by innovations in electro-optic technology (e.g. LCD, OLED), electronic technology (e.g. LTPS, a-Si) and electronic design. Attendees should leave this Tutorial with an understanding of the electronic architectures and circuits that contribute to meeting user expectations in modern display systems.

SPEAKER BIOGRAPHY

Ian Underwood carried out pioneering research and development in LC microdisplays between 1983 and 1999 when he co-founded MicroEmissive Displays Ltd (MED) as co-inventor of its P-OLED microdisplay technology. He was a Fulbright Fellow (1991) at the University of Colorado, Photonics Spectra Circle of Excellence designer (1994), British Telecom Fellow (1997), Ben Sturgeon Award winner (1999), Ernst & Young Emerging Entrepreneur of the Year (2003), Fellow of the Royal Society of Edinburgh (2004), Gannochy Medal winner (2004), Fellow of the Institute of Physics (2008), and Fellow of the Royal Academy of Engineering (2008). Now, he is Professor of Electronic Displays at the University of Edinburgh, Associate Editor of JSID, a member of the Program Committees of ISSCC 2009, SID Displays Week 2009, and Eurodisplay/IDRC 2009. He is co-author of the book Introduction to Microdisplays (2006), and is recognized worldwide as an authority on microdisplay technology, systems, and applications.

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FORUM

Medical Image Sensors

Organizer: **Boyd Fowler,** *Fairchild Imaging, CA*

Committee:
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Hirofumi Sumi, *Sony, Kanagawa, Japan*
Jan Bosiers, *Dalsa, Eindhoven, Netherlands*
Johannes Solhusvik, *Aptina, Oslo, Norway*
Daniel McGrath, *Eastman Kodak, Rochester, NY*

Although image sensors in medical and biotech applications are ubiquitous, new technologies and applications are being developed every year. CCD, CMOS and TFT image-sensor technologies are fueling these applications, and enabling lower-cost and higher-performance systems. These sensors are challenging to design because they have widely varying requirements, including tolerance to X-rays, ultra-small pixels, low read noise, and bio-compatibility. This Forum is focused on presenting the newest image-sensor technologies and applications for the medical and biotech markets. The goal of this Forum is to give engineers and their management an in-depth view of these technologies and their future directions.

Forum Agenda:

Time	Topic
8:00am	Breakfast
8:30am	**Welcome and overview** **Boyd Fowler**, *Fairchild Imaging, Milpitas, CA*
8:40am	**Medical Image Sensor Technology Overview** **Keishi Kitamura**, *Shimadzu Medical Systems Division, Kyoto, Japan*
9:50am	**Dental Radiography** **Chiao Liu**, *Fairchild Imaging, Milpitas, CA*
11:00am	Break
11:10am	**Medical Radiography** **Tim Tredwell**, *Carestream Health, Rochester, NY*
12:20pm	Lunch
1:10pm	**Endoscopy** **Jeffrey Adair**, *Micro-Imaging Solutions, San Clemente, CA*
2:20pm	**Luminescence and Fluorescence Imaging** **Mark Schnitzer**, *Stanford University, Stanford, CA*
3:30pm	Break
3:40pm	**Retinal Implants** **Jun Ohta**, *Nara Institute of Science & Technology, Nara, Japan*
4:50pm	Conclusions

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FORUM

Integrated Neural Interfaces

Organizer: **Reid Harrison,** *University of Utah, Salt Lake City, UT*
Committee: **Timothy Denison,** *Medtronic Neuromodulation Technology, Minneapolis, MN*
Roland Thewes, *Qimonda, Munich, Germany*
Albrecht Rothermel, *University of Ulm, Ulm, Germany*

While interfaces to the brain were recently confined to science fiction, cochlear implants and deep-brain stimulators are now becoming commonplace. This Forum covers circuit and material technologies used to stimulate and record signals from the nervous system. Issues familiar to many circuit designers – low-noise design, micropower design, and partitioning between digital and analog circuits – are recurring themes throughout this all-day Forum. It is designed to be accessible to circuit designers of any background; previous experience in biology or medical devices is not necessary.

The Forum begins with an introduction to the burgeoning field of brain-machine interfaces. **Krishna Shenoy** (Stanford U) describes state-of-the-art electrophysiological techniques and signal-processing algorithms used to extract control signals from the brain for guiding prosthetic devices. The next talk, by **Stuart Cogan** (EIG Laboratories), explores the nature of electrodes used to record electrical activity from neural tissue. The properties of the electrode-tissue interface have important consequences on circuit design for both recording and stimulation applications. Conversely, circuit design for biomedical applications requires careful attention to safety issues. **Maurits Ortmanns** (U Ulm) discusses the design of integrated circuits for the stimulation of the retina, with a focus on safety considerations. The design of electronics for implantable medical devices poses many constraints (e.g. size, power and telemetry bandwidth) for circuit designers. **Reid Harrison** (U Utah) outlines several prominent design trade-offs that result from these unique challenges, including the trade-off between power and noise in biosignal amplifiers, and the optimization of wireless inductive power links. In addition to electrical recording and stimulation, modern microsystems are beginning to incorporate microfluidics for a complete electrochemical interface to the nervous system. **Ken Wise** (U Michigan) describes recent advances in MEMS devices, integrated electronics, and biocompatible packaging, for a wide range of therapeutic applications. Miniaturization may also be facilitated through the use of wafer-level integration. **Chris Van Hoof** (IMEC) presents packaging and integration technologies for wearable and implantable health-care devices, as well as ultra-low-power front-end electronics for microwatt biopotential recording. While some neural-interface technologies are still in the research and development stages, others are mature medical products that routinely improve the lives of thousands of people. **Timothy Denison** (Medtronic) describes commercial deep-brain stimulation (DBS) technology that provides therapy for the treatment of movement disorders such as Parkinson's disease. While current clinical systems operate in a closed-loop manner, there is ongoing research to create a closed-loop system by adding sensing capabilities and on-board algorithms to the stimulator, with the goal of helping physicians provide more optimized therapy. A survey of solutions being explored in early-stage research devices is presented.

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Forum Agenda:

Time	**Topic**
8:00	Breakfast
8:30	**Welcome and Overview** **Reid Harrison**, *University of Utah, Salt Lake City, UT*
8:40	**High-Performance Cortically-Controlled Prosthesis Design** **Krishna Shenoy**, *Stanford University, Stanford, CA*
9:30	**Electrode and Electrode-Tissue Interface Properties Relevant to the Design of Implanted Microelectronic Devices** **Stuart Cogan**, *EIC Laboratories, Norwood, MA*
10:20	Break
10:35	**Safety Issues and Circuit Implementation for Retinal Stimulators** **Maurits Ortmanns**, *University of Ulm, Ulm, Germany*
11:25	**Wireless Neural Recording Systems: Design Trade-Offs at the Circuit and System Levels** **Reid Harrison**, *University of Utah, Salt Lake City, UT*
12:15	Lunch
1:30	**Wireless Implantable Microsystems: Electronic Interface to the Nervous System** **Ken Wise**, *University of Michigan, Ann Arbor, MI*
2:20	**Ultra-Low-Power Biopotential Circuits and Their Integration in Wearable and Implantable Interfaces** **Chris Van Hoof**, *IMEC, Leuven, Belgium*
3:10	Break
3:30	**Technology Considerations for Adaptive Neuromodulation Systems** **Timothy Denison**, *Medtronic Neuromodulation Technology, Minneapolis, MN*
4:20	Panel Discussion All speakers and committee members
4:50	Conclusion

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TRENDS IN IMAGE SENSORS

- The CMOS-image-sensor business is a fast-growing segment of the semiconductor industry that is driven by a yearly cellphone camera growth-rate of approximately 20%. Growth is also seen in other digital-imaging applications such as DSLR, DSC, camcorders, and emerging markets including Web cameras, security cameras, automotive cameras, and gaming.
- In order to maintain market growth in these industries, many barriers must be overcome. These include better image quality, higher sensor resolution (the megapixel race is still ongoing), smaller chip size, higher data-transfer rates, lower power consumption, lower cost, and higher system-level integration. The number of technology barriers in each market depends on the target application.
- The resolution and miniaturization races continue, and, while the performance requirements stay constant, the pixel size is scaling down. In order to compete in this race, new innovative technologies are continuously being developed. These include: digital optics, wafer-level cameras, and backside illumination processes. Another trend is toward 3D integration, i.e. stacking readout and processing chips underneath the imager array.
- The importance of digital-signal-processing technology in digital cameras also continues to grow. This processing is used to mitigate noise, and to compensate for optical limitations. The level of computation-per-pixel is increasing to thousands of operations per pixel, and this requires high-performance and low-power digital signal processing. In addition, there is a parallel trend pushing the industry toward higher levels of system integration.
- At ISSCC 2009, new techniques for lowering read noise are presented, even extending to photon-counting capabilities. This means that the fundamental noise limit has already been reached, and the sensor is essentially noise-free since input photon shot noise dominates at all light levels.
- The trends in emerging markets include: wider dynamic range and faster read-out speed. Therefore, the complexity and performance of CMOS image sensors are growing at an exponential rate, while cost and size constraints are remaining constant.

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TRENDS IN DISPLAYS

- TFT-LCD remains the dominant technology for large-format and mobile displays. High image quality and low cost are the main factors pushing the limits of the driving electronics. The former requires an increase in the number of gray levels, faster settling time, and precise channel-to-channel and chip-to-chip matching. The latter (cost reduction) is accomplished by area shrinkage.

- Active-matrix OLED (AMOLED) is an emerging technology that promises better image quality, lower power, and lower manufacturing cost. Currently, AMOLED displays suffer from random variations in V_t, requiring compensation techniques within the pixel. Digital driving techniques can mitigate image degradation caused by V_t shifts with two-transistor pixels, but common pulse-width-modulation digital driving leads to false contour noise.

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TRENDS IN SENSORS AND MEMS

Sensor and MEMS development continues with emphasis on smaller size, increased functionality, and improved performance. In particular, developments include:

- Sensors are getting smarter because of reconfigurability, and integration of processing
- Temperature sensors for thermal management and process compensation will be everywhere
- Low-noise low-power batteryless passive interfaces
- Low-power at low-cost is driven by cellphones
- Low-cost is driven by cell phones and electronic compasses
- A need for innovative integration with increased functionality is driving two-chip solutions
- Nanosensors require integrated interfaces for biochemical applications
- MEMS resonators scale to frequencies exceeding 100MHz
- Energy scavenging becomes more common
- Commercialization of sensor and MEMS is increasing
- Development of all-axis motion sensing proceeds with three-axis accelerometers and multi-axis gyroscopes
- Increased use of image stabilization in digital cameras and gaming consoles
- Increased emphasis on microphones
- Silicon micromechanical resonators are set to replace quartz crystals
- Increasing use of MEMS switches, filters and tunable passives for radio applications
- Appearance of gravimetric biochemical sensor arrays
- Growing importance of electronic compasses
- Increased appearance of implantable sensors

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TRENDS IN MEDICAL

- Biomedical applications of electronic circuits and systems involve many sensing paradigms, ranging from extracting the electrical signals in the brain, to sensing pressure in blood vessels, to molecular detection of DNA.

- Recently, the field has focused on monitoring biological parameters for healthcare applications, both in the clinic and as support for fundamental research. In these systems, the optimization of sensor sensitivity and specificity must be balanced with other requirements such as the provision of power and telemetry, and the overhead of external circuitry. Recent trends in the scaling of circuits and the use of wireless and batteryless architectures, in combination with novel sensing and circuit architectures, are enabling the next generation of medical electronics with a positive impact on health care. This progress is made by enabling medical research through provision of better tools for in-vitro monitoring, by facilitating diagnosis through lab-on-chip systems, and by clinical electronics used directly by the patient.

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Low-Power Digital Subcommittee

- Overview
- Featured Papers
- Panel
- Tutorial
- Forum

ISSCC 2009 – LOW-POWER DIGITAL

Subcommittee Chair: *Wanda Gass, Texas Instruments, Dallas, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- The first fully-integrated backend SoC for Blu-ray players includes content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3 **[8.4]**
- A video-encoding chip supporting encoding of multiple views at HD solutions: 1-view (4096 x 2160p), 3-view full-HD (1080p), and 7-view HD (720p) for 3D display applications **[8.5]**
- The first Full-HD SoC available for handsets: 166MHz Mobile Application Processor is implemented in 65nm to support multistandard video codec at Full-HD resolution **[8.7]**
- A fully-integrated IR-UWB receiver for communication and sub-cm ranging **[14.1]**
- First non-coherent receiver allowing faster and lower-energy synchronization **[14.2]**
- First IC to achieve 4x4 64-QAM MIMO detection that is easily scalable to 256-QAM **[14.4]**

APPLICATIONS AND ECONOMIC IMPACT

- Blu-ray player will be less expensive and become more affordable **[8.4]**
- Display resolution is no longer limited to Full-HD, with Quad Full-HD appearing to realize multiple- and 3D-display applications **[8.5]**
- Handset with Full-HD video recording and playback capability can be introduced to market in 2009 ~ 2010 **[8.7]**
- Lighting and temperature control and room localization, let the music follow you through your home **[14.1]**
- Industrial monitoring and construction monitoring. Improve safety **[14.2]**
- Very-low-power consumption enables longer battery life in handheld devices employing advanced MIMO wireless communication capability **[14.4]**

PANEL

MID – "Scaled-Down" PC or "Souped-Up" Handheld? **[E2]**

TUTORIAL

Adaptive Power-Management Techniques **[T2]**

FORUM

Ultra-Low-Voltage Circuit Design **[F4]**

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HD Video

A Multi-Format Blu-ray Player SoC in 90nm CMOS [8.4]

MediaTek

A 212Mpixel/s 4096x2160 Multiview-Video-Encoder Chip for 3D/Quad HDTV Applications [8.5]

National Taiwan University

A 342mW Full-HD (1080p30) Mobile-Application Processor with a Multi-Standard Video Codec and Tile-based Address-Translation Circuit Implemented on an IP-MMU [8.7]

Renesas Technology

PRESENT STATE OF THE ART (THE PROBLEM)

- An HD-video solution is still unable to target the 2009 handset market due to its high power consumption and memory bandwidth.
- Blu-ray players are still expensive and bulky due to the complexity of the system and the diversity of disc formats.

NOVEL CONTRIBUTIONS

- The first fully-integrated backend SoC is introduced for Blu-ray players including content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3 **[8.4]**
- The Blu-ray SoC achieves a 14.36% area reduction by sharing the computation resources **[8.4]**
- A Blu-ray SoC integrates HDMI 1.3 outputs by applying a direct digital synthesizer (DDS) and a new transition-minimized differential signaling (TMDS) structure to reduce the additional external capacitor and to improve jitter performance **[8.4]**
- A video encoding chip supporting encoding of multiple views at HD resolution: 1-view (4096 x 2160p), 3-view Full-HD (1080p), and 7-view HD (720p) for 3D-display applications **[8.5]**
- The highest encoding resolution (Quad Full-HD) is achieved by using a cache-based prediction core, resulting in 79% reduction in system bandwidth and 94% reduction in on-chip SRAM capacity **[8.5]**
- The first Full-HD SoC available to handsets, the 166MHz Mobile-Application Processor is implemented in 65nm to support a multi-standard video codec at Full-HD resolution **[8.7]**
- 342mW is achieved while playing H.264 video at Full-HD resolution suitable for battery-powered handset systems **[8.7]**
- A Full-HD SoC consumes only 55% of the power of the media processor that appeared at ISSCC2008 **[8.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Blu-ray players will be less expensive and more affordable **[8.4]**
- Display resolution is no longer limited to Full-HD, but extending to Quad Full-HD for multiple- and 3D-display applications **[8.5]**
- Handsets with Full-HD-video recording and playback capability can be introduced to the market in 2009 to 2010 **[8.7]**

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Multiple-Input Multiple-Output (MIMO) Detection

A 0.13µm CMOS 655Mbs, 4x4 64-QAM K-Best MIMO Detector [14.4]

University of Toronto

PRESENT STATE OF THE ART (THE PROBLEM)

- MIMO detection is a critical part of the receivers of future wireless communication systems that use spatial multiplexing to multiply achievable data rate without mandating more precious spectrum resources, such as needed by IEEE 802.11n WiFi, IEEE 802.16e/m WiMAX, and 3GPP LTE.
- As the antenna number and the modulation order get higher, MIMO detection becomes exponentially more complicated.

NOVEL CONTRIBUTIONS

- First IC to achieve 4x4 64-QAM MIMO detection that easily scales to 256-QAM **[14.4]**
- Scalable and pipelined design **[14.4]**
- Throughput more than 5X previous design **[14.4]**
- Highest power efficiency in terms of mW/Mb/s **[14.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- This area-efficient MIMO detector design allows easy integration into future low-cost high-throughput wireless-communication receivers **[14.4]**
- Very low power consumption enables long battery life in handheld devices with MIMO-wireless-communication capability **[14.4]**

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Ultra-Wide-Band

A Reconfigurable, 0.13µm CMOS 110pJ/pulse Fully-Integrated IR-UWB Receiver for Communication and Sub-cm Ranging [14.1]

Katholieke Universiteit Leuven

A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with ±1ns Synchronization Accuracy [14.2]

Massachusetts Institute of Technology

PRESENT STATE OF THE ART (THE PROBLEM)

- Ultra-Wide-Band Impulse Radio (IR-UWB): Its first standard was defined in 802.15.4a. As a competitor for Bluetooth and Zigbee wireless standards, IR-UWB provides better energy efficiency in terms of J/bit for communication
- Power-efficient communication remains a hot issue. Even further, improvements are needed in the future.
- Both papers are not standard (802.15.4a) compliant **[14.1; 14.2]**

NOVEL CONTRIBUTIONS

- Combining the RF frontend and baseband to reach a higher integration level and better energy performance **[14.1; 14.2]**
- Ranging and localization in the cm-range **[14.1]**
- First non-coherent receiver allowing faster and lower-energy synchronization **[14.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Lighting and temperature control and room localization, let the music follow you through your home. **[14.1]**
- Saving “flying wires”: control lights, music, and video wirelessly from your seat **[14.1]**
- Improves comfort **[14.1]**
- Industrial monitoring and construction monitoring to improve safety. **[14.1; 14.2]**

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PANEL

MID – "Scaled-Down PC or Souped Up" handheld?

Co-organizer: Yiwan Wong, *Samsung Electronics, Yongin, Korea*

Co-organizer: Raney Southerland, *ARM, Austin, TX*

Chair: Jan Rabaey, *UC Berkeley, Berkeley, CA*

OBJECTIVE

- Explore dynamics of the Mobile Internet Device ecosystem and its technology web

CHALLENGE

- To define systems that addresses multiple needs in a single handset/device.
- To deliver solutions that integrate hardware and software to fulfill consumers' expectations.
- To develop mobile standards that make transparent portability commonplace.

CONTROVERSY

- Can the high performance requirements be achieved while maintaining ultra-low-power for longer battery life?
- What are the applications of an MID device – smart phones, multimedia players, netbooks/ personal computers, etc.?
- What will be the gap, if any, between a laptop-focused and a phone-focused MID device?
- What hardware architecture and software platform will be the most effective enablers for the MID market?

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TUTORIAL

Adaptive Power Management Techniques

Alice Wang, *Texas Instruments, Dallas, TX*

OVERVIEW

As highlighted by the Conference theme "Adaptive Circuits and Systems", increasingly adaptive techniques are used to manage the power dissipation of SoCs. These SoCs are integrating more transistors per die, facing worsening leakage dissipation with each process node, and are operating at ever-higher processor frequencies. State-of-the-art adaptive power management techniques such as adaptive voltage scaling, body bias, power gating, dynamic voltage-frequency scaling, and sleep modes, are discussed both in theory and through examples of implementations found in practice.

SPEAKER BIOGRAPHY

Alice Wang is currently Senior Member of Technical Staff at Texas Instruments in Dallas, Texas. She is involved in the design of SoCs in the Wireless-Terminal Business Unit for application in digital baseband and application processors in cellular phones, focusing on low-power techniques and enhancing battery lifetime. She received her PhD in Electrical Engineering from the Massachusetts Institute of Technology, in 2004. Part of her PhD thesis work demonstrated the first-ever 180mV sub-threshold FFT processor.

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FORUM

Ultra-Low-Voltage-Circuit Design

Organizer: **Raj Amirtharajah,** *University of California, Davis, CA*

Committee: **Tzi-Dar Chiueh,** *National Taiwan University, Taipei, Taiwan*
Ram Krishnamurthy, *Intel, Hillsboro, OR*
Jos Huisken, *IMEC, Eindhoven, Netherlands*
Siva Narendra, *Tyfone, Portland, OR*
Steffen Paul, *Universität Bremen, Bremen, Germany*
Pascal Urard, *STMicroelectronics, Crolles, France*
Alice Wang, *Texas Instruments, Dallas, TX*

OBJECTIVE

Low-power CMOS design has relied heavily on V_{DD} scaling in the past to exploit the quadratic dependence of dynamic power and the exponential dependence of leakage power on voltage. Today, leading-edge low-voltage designs are pushing FET operation into the weak inversion and subthreshold regimes. Investigators around the world are reporting circuits at voltages between 180mV and 700mV that offer performance which could support a range of applications in wireless sensors, mobile phones, biomedical devices, and ultra-mobile PCs. However, these circuits are highly sensitive to variations in temperature and process. Ultra-low-voltage circuits will be increasingly challenging to design as feature sizes shrink. Current trends indicate nominal supply voltages are unlikely to be reduced much below 1V, transistor threshold voltages will likely remain between 0.3 and 0.4V to manage subthreshold leakage, and effects such as random- dopant fluctuation will increase the spread in transistor parameters, all of which create difficulties in designing robust circuits at low V_{DD}. This Forum brings together leading experts to describe future challenges in ultra-low-voltage design, to explore ultra-low-voltage circuit techniques, and to stimulate thinking about prospects for future ultra-low-voltage high-volume products.

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Forum Agenda:

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Raj Amirtharajah**, *University of California, Davis, Davis, CA*
8:30	**Motivation for Ultra-Low Voltage / Low Power Designs** **Christian Piguet**, *CSEM, Neuchatel, Switzerland*
9:10	**Technology Scaling and Challenges for Ultra-Low-Voltage Design** **Kaushik Roy**, *Purdue University, West Lafayette, IN*
9:50	Break
10:10	**Device Sizing for Variability in Energy Constrained Systems** **Dennis Sylvester**, *University of Michigan, Ann Arbor, MI*
10:50	**Variability and Ultra-Low Voltage Logic Design** **Takayasu Sakurai**, *University of Tokyo, Tokyo, Japan*
11:30	**Ultra-Low-Voltage Microprocessor Design: Challenges and Solutions** **Ram Krishnamurthy**, *Intel, Hillsboro, OR*
12:10	Lunch
1:00	**Challenges and Opportunities for Scaled Low Voltage SRAM** **Ben Calhoun**, *University of Virginia, Charlottesville, VA*
1:40	**Ultra-Low-Voltage Analog Circuit Design** **Christian Enz**, *EPFL, Lausanne, Switzerland*
2:20	**Probabilistic CMOS (PCMOS) Logic for Nanoscale Circuit Design** **Krishna Palem**, *Rice University, Houston, TX*
3:00	Break
3:20	**Panel Discussion:** **Future Prospects for Ultra-Low Voltage Design in Commercial Products**
4:10	Conclusion

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MEMORY Subcommittee

- Overview
- Featured Papers
- Tutorial
- Forum
- Trend Charts

ISSCC 2009 – MEMORY

Subcommittee Chair: *Hideto Hidaka, Renesas Technology, Itami, Japan*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- First 4Gb DDR3 highest-density DRAM at 1.2V power supply **[7.1]**
- First 8Gb through-silicon-via 4-stacked DDR3 with master/slave separate chips **[7.2]**
- Fastest-data-rate mobile DDR2 DRAM (4.3GB/s) **[7.3]**
- Fastest GDDR5 DRAM with a data rate of 7Gb/s/pin **[7.4]**
- First-reported 32Gb 34nm MLC NAND Flash Memory with 9MB/s write throughput **[13.1]**
- A 113mm^2 32Gb 3b/cell NAND memory that fits into a microSD memory card **[13.4]**
- Use of inductive coupling for NAND Flash stacking in SSD with 2Gb/s and 15pJ/bit/chip capability **[13.5]**
- First-reported 64Gb 4bit/cell Flash NAND memory with 5.6MB/s write throughput **[13.6]**
- The first 32nm high-density and high-performance SRAM in a Hi-k metal-gate technology **[27.1]**
- The 128Mb FeRAM is the largest-capacity in emerging nonvolatile RAM reported and 1.6GB/s bandwidth is 4 to 8× higher than previously reported **[27.5]**

APPLICATIONS AND ECONOMIC IMPACT

- Today's highest volume of use of DRAMs in PCs in 1Gb format. The new 4Gb DRAM will boost the main memory capacity by 4×, providing up to 4GB per module, or 1GB per module at a lower price **[7.1]**
- By using through-silicon-via technology and stacking of four 2Gb die, the 8Gb memory in one package raises productivity by using less-expensive assembly and interconnect technologies, thus resulting in lower cost to migrate DRAM modules to 8GB **[7.2]**
- Mobile DRAM saves power and moves bits at higher DDR2 speeds for improved performance of mobile appliances including cell-phones and PDAs **[7.3]**
- The 7Gb/s DDR5 DRAM chip provides more lively graphics and images, thus accelerating acceptance by consumers using the most advanced displays **[7.4]**
- All of these DRAM enhancements will benefit consumers, providing lower-cost, faster, and popular electronic devices with more memory capacity.
- This year, papers have focused on increasing density and lowering cost of the NAND Flash memories. Some push lithography, as in paper **[13.1].**
- Some use design techniques to increase the number of bits per cell as in paper **[13.6).**
- Availability of advanced technologies lowers the cost of NAND Flash and associated devices resulting in wider adoption of technologies in other storage applications.
- The new 32nm SRAM illustrates an overall SRAM scaling trend. It continues to follow Moore's Law, and provides significant power, performance, and density benefits, enabling SRAMs to meet future product applications **[27.1]**
- The FeRAM with a 400MHz DDR2 interface is fully compatible with commodity DRAMs and can easily replace conventional DRAM, enhancing computer and memory-system performance **[27.5]**

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TUTORIAL

Variation-Tolerant SRAM Circuit Designs [T8]
This Tutorial will discuss how SRAM has been scaled down in size and operating voltage, showing future directions for change.

FORUM

SSD Memory Subsystem Innovation [F1]
This Forum highlights system and circuit approaches to high-capacity data-storage systems employing NAND flash memory. The Forum will present a wide range of emerging memory prospects.

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DRAM Achieves 4Gb Density at DDR3 Speed

1.2V 1.6Gb/s 56nm $6F^2$ 4Gb DDR3 SDRAM with Hybrid-I/O Sense Amplifier and Segmented Sub-Array Architecture [7.1]

Samsung

PRESENT STATE OF THE ART (THE PROBLEM)

- 1Gb is the highest density ever published (at ISSCC 2007)
- 2Gb monolithic DDR3s commercially available in the market

NOVEL CONTRIBUTIONS

- The first DDR3 developed at 1.2V **[7.1]**
- A hybrid-type I/O sense amplifier for an open-bitline architecture **[7.1]**
- Standby and operating current are reduced by more than half **[7.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- PC memory gets a higher bandwidth without consuming extra power **[7.1]**
- Smaller chip size occupies less space on the system board **[7.1]**

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DRAM Goes 3-Dimension Using Through-Silicon Vias

8Gb 3D DDR3 DRAM Using Through-Silicon-Via Technology [7.2]

Samsung

PRESENT STATE OF THE ART (THE PROBLEM)

- DRAM has been stacked through external interconnections that jump over the packaged chips
- 8Gb is the highest stack chip configuration yet published

NOVEL CONTRIBUTIONS

- Master and slave type of DRAM, each connected through silicon via **[7.2]**
- Power-supply noise has been reduced by providing extra power pads **[7.2]**
- First demonstrated through-silicon-via (TSV) check and repair scheme **[7.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- A major roadblock in DRAM scaling could be resolved using 3D techniques **[7.2]**
- Wider I/O in DRAM will be possible with through-silicon-via (TSV) technology **[7.2]**

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Mobile DRAM Reaches 4.3GB/s

A 1.35V 4.3GB/s 1Gb LPDDR2 DRAM with Controllable Repeater and On-the-Fly Power-Cut Scheme for Low-Power and High-Speed Mobile Applications [7.3]

Hynix

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 2GB/s is the fastest data rate for mobile DRAM
- Conventional DDR3 SDRAM uses a 1.5V power supply

NOVEL CONTRIBUTIONS

- First 1.35V LPDDR2 SDRAM chip developed **[7.3]**
- 4.3GB/s data-rate is achieved with only 110mW power dissipation **[7.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- High-end mobile DRAM can be used to enhance mobile-system performance **[7.3]**
- Battery life of multimedia devices can be significantly increased **[7.3]**

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GDDR5 Graphics DRAM Boosted to 7Gb/s/pin

A 75nm 7Gb/s/pin 1Gb GDDR5 Graphics Memory Device with Bandwidth-Improvement Techniques [7.4]

Qimonda

PRESENT STATE OF THE ART (THE PROBLEM)

- 6Gb/s/pin is fastest published data rate (at ISSCC 2008)

NOVEL CONTRIBUTIONS

- Fastest GDDR5 DRAM developed to date (with data rate of 7Gb/s/pin) **[7.4]**
- Multiple power domains limit on-chip power noise to 10mV **[7.4]**
- Boosted transmitter opens data eye by 100mV **[7.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Enhancing performance in high-end graphic cards and game consoles **[7.4**]
- DRAM enables higher data rates and improves signal integrity **[7.4]**

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NAND Flash Memory Boosts Storage

A 172mm^2 32Gb MLC NAND Flash Memory with 34nm CMOS [13.1]

Intel; Micron

A 2Gb/s 15pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking [13.5]

Keio University; University of Tokyo

A 5.6MB/s 64Gb 4-Bit/Cell NAND Flash Memory on 43nm CMOS Technology [13.6]

Sandisk; Toshiba

PRESENT STATE OF THE ART (THE PROBLEM)

- Cost-per-bit for NAND Flash is currently higher than the cost-per-bit of magnetic storage
- 32Gb on 43nm is the highest density reported to date
- SSD has significant performance advantages over HDD, but the cost differential is limiting adoption to certain markets
- Significant technical challenges exist in stacking many NAND chips in an SSD for high-density storage

NOVEL CONTRIBUTIONS

- NAND Flash achieves 32Gb in 34nm, the most advanced lithography yet reported to date **[13.1]**
- High speed low power with reduced packaging cost for improved stacking of NAND in SSD **[13.5]**
- First reported 64Gb NAND Flash Memory featuring a 4b/cell solution with a 5.6MB/s program throughput **[13.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- High storage capacity and reduced cost per bit will enable wide adoption of NAND in solid-state storage applications in the coming years **[13.1; 13.6]**

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First Fully Functional 291Mb SRAM in 32nm High-κ Metal-Gate Technology

A 4.0GHz 291Mb Voltage-Scalable SRAM in 32nm High-κ Metal-Gate CMOS Technology with Integrated Power Management [27.1]

Intel

PRESENT STATE OF THE ART (THE PROBLEM)

- SRAM faces severe challenges in cell stability for low-voltage operation.
- SRAM leakage power has grown significantly as transistor scaling continues beyond 45nm.

NOVEL CONTRIBUTIONS

- The co-optimization of technology and design has achieved excellent performance over a wide operating range of voltage scaling. **[27.1]**
- Advanced power-management schemes are seamlessly integrated into the design to provide more than 2× power reduction, while maintaining high performance. **[27.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- The new 32nm SRAM demonstrates an overall SRAM scaling trend that continues to follow Moore's Law and provides significant power, performance, and density benefits. **[27.1]**
- The combination of advanced high-κ metal-gate technology and advanced circuit design enables high-performance and low-power SRAMs to meet future product needs. **[27.1]**

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Ferroelectric RAM Reaches 1.6GB/s Era

A 1.6GB/s DDR2 128Mb Chain FeRAM with Scalable Octal Bitline and Sensing Schemes [27.5]

Toshiba

PRESENT STATE OF THE ART (THE PROBLEM)

- Previous emerging memories such as FeRAM and MRAM are limited to 64Mb, which is not enough for cache applications with nonvolatile needs.
- The maximum read and write bandwidths in previous nonvolatile memories are limited to 400MB/s and 200MB/s, respectively, which are not high enough to replace DRAM with nonvolatile RAM for cache applications.

NOVEL CONTRIBUTIONS

- The 128Mb FeRAM has the largest capacity reported for emerging nonvolatile RAMs. **[27.5]**
- The 1.6GB/s read/write bandwidth is 4×/8× higher than previously published emerging nonvolatile memories. **[27.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- The FeRAM with 400MHz DDR2 interface is fully compatible with commodity DRAMs, and can easily replace conventional DRAM**. [27.5]**
- High-density and high-bandwidth nonvolatile RAM enhances computer and memory-system performance**. [27.5]**

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TUTORIAL

Variation-Tolerant SRAM Circuit Designs

Hiroyuki Yamauchi, *Fukuoka Institute of Technology, Fukuoka, Japan*

OVERVIEW

This Tutorial starts with a discussion of the basic understanding of SRAMs, challenges and some of the key circuits required for a robust designer. Threshold-voltage variation is a critical factor in designing memories at 45nm and below, due to process variation. Various circuit techniques to enable further area and voltage scaling will be shared in this Tutorial. Comparison of the circuit techniques presented at leading conferences for design at 65nm and beyond will be discussed, and an overview presented.

Statistical design methods along with circuit-based margin-assist techniques and their impact on process/voltage/temperature (PVT) variations are discussed in detail.

- Overview of SRAM applications and scaling
- Operating-voltage and area scaling trends and key challenges
    - Static noise margin (SNM)
    - Write margin (WRM)
    - Cell current margin (Icell)
- Statistical-margin analysis methods
- Circuit-design techniques
- Discussion of the scalability of circuit techniques

SPEAKER BIOGRAPHY

Hiroyuki Yamauchi is a Professor at the Fukuoka Institute of Technology in Fukuoka, Japan. Previously, he worked for Panasonic in Japan for 20 years and had responsibility as a general manager for developing embedded SRAM, DRAM, and nonvolatile memories. He has invented and developed various SRAM and DRAM circuit design techniques, such as a charge-recycling data bus architecture and a control scheme that elevates SRAM source line potential for leakage reduction and variability tolerance. He holds 87 US patents and has published over 40 papers in the area of memory design. He received his PhD in Engineering from the University of Kyushu, in Fukuoka, Japan, in 1997.

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FORUM

Memory Subsystem Innovation

OBJECTIVE
Solid-state disks (SSDs) and emerging memories such as fusion memories, PCRAM, FeRAM, and MRAM have enabled innovations in various nano-scale VLSI memory systems for personal computers, multimedia applications, and enterprise servers. The full-day Forum is intended to provide a comprehensive review of various state-of-the-art memory architectures, as well as memory technologies.

AUDIENCE
This Forum is intended for both practicing engineers in industry and graduate students in VLSI-related disciplines. This audience will gain state-of-the-art knowledge of a wide range of VLSI memory systems, related emerging memories, and SSDs.

SCOPE
This Forum will cover a wide variety of new memory applications enabled by various memories such as NAND Flash memories, fusion memories, PCRAM, FeRAM, and MRAM. Many critical system- and circuit-design techniques for various application requirements will be presented.

PROGRAM
The Forum will address a broad range of key technical challenges facing designers of today's VLSI memory systems. The Forum starts an the overview on the microprocessor memory architectures. It will explore the challenges, implications, and options available to remove the traditional memory bottlenecks such as memory latency, memory bandwidth, and off-package bandwidth in the Moore's-law-driven multi- and many-core systems. Next, the system-level memory architecture is addressed. The widespread use of NAND Flash memories in SSDs and caches has opened new avenues of innovation for the enterprise and client computing segments. System-wide architectural changes are required to make full use of the advantages of SSDs in terms of performance, reliability and power. Circuit-design and reliability challenges of NAND-Flash-memory-based SSDs will also be discussed. In emerging multimedia applications, a higher bandwidth and therefore a faster-random-access memory is required. NAND flash memory is also playing a more important role because the write-performance improvement of the memory improves user experience of high-speed wireless downloads. This Forum will also discuss the fusion memory where innovative memory designs provide flexibility to hand-set manufacturers allowing them to better balance cost and performance of many types of multimedia handset designs. In addition, in the Forum, three key emerging nonvolatile memories (PCRAM, FeRAM and MRAM) and their memory systems will be examined. Nonvolatile random-access memory is becoming a viable alternative to commonly used volatile and nonvolatile memories in the marketplace. Being bit-alterable like DRAM and nonvolatile like a flash memory together with a CMOS-process compatibility, the nonvolatile random access memory has a potential to revolutionize many aspects of the computing platform architectures. Further, the Forum will discuss leading edge emerging memories and their applications to the computing and storage architectures. The Forum will also provide an excellent opportunity for the attendees to interactively engage with the speakers on any key technical issues they may face in their product development.

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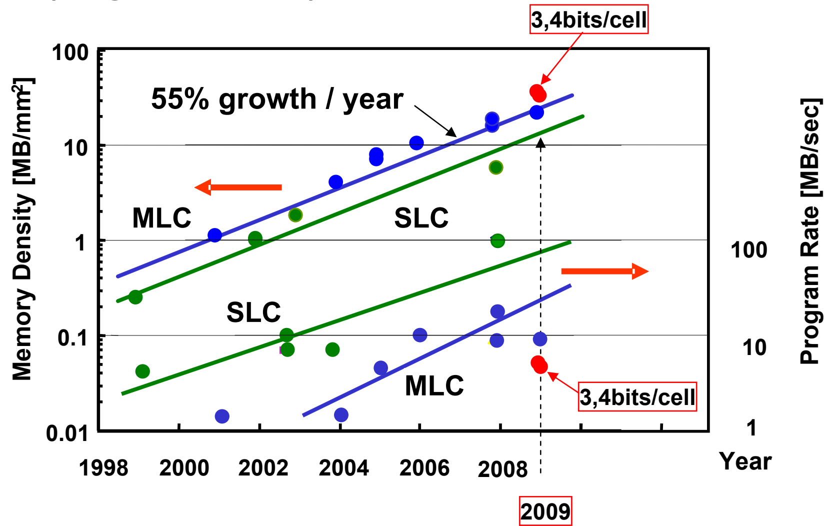
NAND Flash Trend (1)

ISSCC paper
- MLC (Multi-Level Cell) : 2bits/cell
- SLC (Single-Level Cell) : 1bit/cell



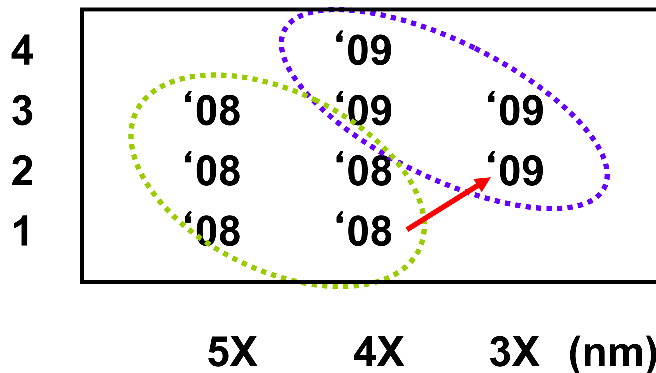
NAND Flash Trend (2)

NAND Flash Memory@ISSCC

'08 : Paper presented

'09 : Paper to be presented

(bits/cell)



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RF Subcommittee

- Overview
- Featured Papers
- Special-Topic Session
- Tutorial
- Forums
  (co-sponsored by RF and Wireless)
  (co-sponsored by Analog, Data Converters, and RF)
- Trend chart

ISSCC 2009 – RF

Subcommittee Chair: *John R. Long, Delft University of Technology, Netherlands*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- A single-gate mixer topology with current reuse consumes just 380μW at 0.6V. **[12.5]**
- A novel technique to vastly reduce harmonic interference in direct-conversion receivers using an analog Walsh shaper **[12.7]** in the RF front-end with further interference cancelation in the digital domain. **[12.9]**
- An all-CMOS integrated transmitter realized with a power-mixer array in 0.13μm CMOS achieving 26dBm output power with 19% power-added efficiency for 16-QAM **[22.2]**
- A 90nm CMOS power amplifier providing 23dBm with 12% power-added efficiency for a 16QAM WiMAX signal, enables long-range high-data low-cost single-chip communications **[22.3]**
- A demonstration of mm-wave power amplifiers at 60GHz to enable Gbit/s communications using low-cost state-of-the-art 65nm and 45nm CMOS at 1V. **[22.4; 22.5]**
- The highest-reported operating frequency (150GHz) for an amplifier in CMOS, enabling new applications from imaging to high-data-rate short-range communications **[29.1]**
- Record gain (26dB) reported for a 100GHz SiGe amplifier using a novel traveling-wave broadband topology **[29.3]**

APPLICATIONS AND ECONOMIC IMPACT

- Interference-robust receivers for handheld digital TV will enable ubiquitous news and entertainment in mobile terminals. **[12.1]**
- Integration of a larger number of wireless standards and services within a smaller footprint using software-defined broadband radio receivers, will ultimately allow communication anywhere, anytime. **[12.8; 12.9]**
- Improved power-amplifier efficiency will lead to a greener tomorrow. **[22.2; 22.3]**
- Deep submicron CMOS is unlocking millimeter-wave frequency bands (e.g., 60GHz band worldwide) promising gigabit wireless in portable consumer electronics. **[22.4; 22.5], [29.6; 29.7].**
- Low-cost silicon-based technologies enabling medical imaging at 100GHz can promote applications from early tumor detection to improved homeland security. **[29.1; 29.2; 29.3].**

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SPECIAL-TOPIC SESSION

Healthy Radios: Radio & Microwave Devices for the Health Sciences [SE1]
With an aging population, the demand for innovative low-cost solutions to problems in medical diagnosis and outpatient monitoring has vastly increased. Researchers have been exploring new techniques which utilize RF circuits in biomedical applications. This Special Evening Topic (SET) session will highlight some of the recent advances in the area of RF circuits for "Healthy Radios". Speakers in this SET will describe work being done to develop wireless transceivers to communicate biological and medical information for applications ranging from implantable devices to Body-Area Networks (BAN). In addition, some presentations will describe the use of RF circuits to either diagnose or analyze medical information.

TUTORIAL

Fundamentals of Digitally-Assisted RF [T4]
RF circuits implemented in nanoscale CMOS suffer from poor linearity, device mismatch, low V_{dd} headroom, high leakage, high flicker and substrate noise, etc. At the same time, digital gates and memory are "free" and powerful, so that digital techniques can be used to mitigate the RF circuit imperfections and match (or possibly exceed) that of traditional RF circuits. This Tutorial examines opportunities for digital assistance of RF, and presents case studies of calibration, compensation, performance tuning, automatic reconfigurability, and built-in self-test.

FORUM

Clock Synthesis Design [F7] ***(co-sponsored by Analog and Data converters)***
One of the most critical and challenging functions present in almost every electronic system is clock or frequency generation. High-performance clocks or precise frequency references are needed in digital systems, data converters, serial data communications and wireless transceivers, to just name a few examples. Wireless systems rely heavily on the phase-locked loop, but recent forays into nanometer CMOS processes for RF SoCs open new architectural opportunities with all-digital and digitally-intensive implementations, both for carrier-frequency synthesis and for phase-modulated transmission schemes. Data converter performance has improved so much that ADC performance is now limited as much by the clock-path noise and jitter, as by the quantization or thermal noise of the input-signal path. That of course has led to new challenges for clock-generation systems with sub-ps or even sub-100fs rms-jitter performance. The objective of this Forum is to present an overview of recent state-of-the-art developments in this crucial field, by leading experts.

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Low-Power Low-Voltage RF Building Blocks

A 0.6V 380μW -14dBm LO-Input 2.4GHz Double-Balanced Current-Reusing Single-Gate CMOS Mixer with Cyclic Passive Combiner [12.5]

Toshiba

A 0.75V 325μW 40dB-SFDR Frequency-Hopping Synthesizer for Wireless Sensor Networks in 90nm CMOS [12.7]

Eindhoven University of Technology; Broadcom; Holst Centre

PRESENT STATE OF THE ART (THE PROBLEM)

- Low-power operation is required for autonomous networking of sensors.
- Low-voltage operation is mandatory for deep-submicron SoCs.
- Low-voltage power supply limits linear and high-speed operation.

NOVEL CONTRIBUTIONS

- A single-gate mixer topology with current-reuse technique consumes just 380μW at and 0.6V operation.**[12.5]**
- A frequency-hopping baseband synthesizer incorporates Walsh-shaping and SSB mixing to reach μW power levels from a sub-1V supply.**[12.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- A sub 1V deep-submicron mixed-signal SoC stimulates various wireless applications **[12.5, 12.7]**
- Low-power operation is essential for enabling sensor-network applications. **[12.5, 12.7]**

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Software-Defined Radio

A Software-Defined Radio-Receiver Architecture, Robust to Out-of-Band Interference [12.8]

University of Twente

A 400-to-900 MHz Receiver with Dual-Domain Harmonic Rejection Exploiting Adaptive Interference[12.9]

University of Twente

PRESENT STATE OF THE ART (THE PROBLEM)

- For interference cancellation, conventional systems require a harmonic-rejection filter preceding the LNA.
- Analog mismatch limits stable interference cancellation.

NOVEL CONTRIBUTIONS

- An analog Walsh shaper helps reduce harmonic interference in direct-conversion receivers. **[12.7]**
- Digital domain interference cancelation improves interference reduction. **[12.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- New software-definable radio-receiver architecture minimizes RF-band filtering, thereby improving flexibility and reducing size and cost. **[12.8]**
- Digitally-assisted RF adds robustness despite process variation of deep sub-micron CMOS **[12.9]**

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Advances in RF Power Generation

An Octave-Range Watt-Level Fully Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off Efficiency Improvement [22.2]

California Institute of Technology; Toshiba

A Single-Chip Highly Linear 2.4GHz 30dBm Power Amplifier in 90nm CMOS [22.3]

University of California, Berkeley; Intel

PRESENT STATE OF THE ART (THE PROBLEM)

- High-efficiency power generation for non-constant envelope applications is difficult to achieve, especially in standard CMOS processes.
- Previous work relies on difficult-to-implement polar modulation approaches.
- Integration of deep-submicron CMOS power amplifiers with sufficient linearity for advanced wireless applications has not been possible to date

NOVEL CONTRIBUTIONS

- Replacing the need for a separate power amplifier, a 0.13µm CMOS power mixer array provides 26dBm with 19% power-added efficiency for a 16-QAM signal **[22.2]**
- Without predistortion, a 90nm CMOS power amplifier provides 23dBm with 12% power-added efficiency for a 16-QAM WiMAX signal **[22.3]**
- Additionally, two V-band mm-wave power amplifiers push the 60GHz state-of-the-art with 65nm and 45nm CMOS at 1V. **[22.4, 22.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- High-efficiency RF power generation in standard CMOS enables ever higher levels of integration for lower cost in handheld communication devices **[22.2, 22.3]**
- Deep-submicron CMOS power amplifiers for 60GHz wireless systems enable short-range networks with extremely high data rates such as wireless HDMI **[22.4, 22.5]**

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Silicon Millimeter-Wave Circuits Exceeding 100GHz Operation

A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS using Dummy-Prefilled Microstrip Lines [29.1]

University of California, Santa Barbara; IBM VT, IBM France

W-Band CMOS Amplifiers Achieving +10dBm Saturated Output Power and 7.5dB NF [29.2]

Helsinki University of Technology

A 26dB-Gain, 100GHz Si/SiGe Cascaded Constructive-Wave Amplifier [29.3]

University of California, San Diego

PRESENT STATE OF THE ART (THE PROBLEM)

- Radio applications beyond 100GHz, including high-data-rate communication links, medical imaging, weapons, explosives and chemical sensors, need a low-cost enabling technology.
- Realization of mm-wave-radio front-ends in CMOS is constrained by low available transistor gain and strict metal-density rules that alter passive-component characteristics.

NOVEL CONTRIBUTIONS

- 150GHz amplifier in baseline digital CMOS using dummy-prefilled microstrip lines has record low-power consumption **[29.1]**
- Slow-wave CPW-based CMOS amplifier operates from 85GHz to 100GHz. **[29.2]**
- Highest published gain (26dB) achieved in SiGe at 100GHz uses a novel traveling-wave broadband topology **[29.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- 150 GHz is the highest-ever-reported operating frequency in 65nm CMOS for an amplifier that boasts wide bandwidth and 35% lower power consumption than previous silicon implementations. **[29.1]**
- CMOS enables low-cost and higher system integration with low power consumption for millimeter-wave applications including medical imaging, broadband communications, security imaging, and chemical sensing **[29.1; 29.2]**
- The cascaded Constructive-Wave Amplifier (CCWA) in SiGe combines features of traveling-wave and cascaded amplifiers for broadband applications **[29.3]**

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SPECIAL-TOPIC SESSION

Healthy Radios: Radio & Microwave Devices for the Health Sciences

Organizer: ***Jacques C. Rudell,*** *Intel, Redwood City, CA*
Co-Organizer: ***Ali Hajimiri,*** *Caltech, Pasadena, CA*

Chair: ***Jacques C. Rudell,*** *Intel, Redwood City, CA*

OVERVIEW

More than a century ago, Guglielmo Marconi made the first transatlantic radio transmission which forever changed the way people communicate with one another. Scientists and engineers have spent the last century developing more efficient radio circuits, systems and software for wireless communication applications. Recently, engineers have begun to explore the use of radio-frequency circuits for biomedical applications. The use of “Healthy Radio” can be categorized into two sub-topics. The first is the use of radios to communicate sensed information from the body to the outside world. The second is the use of traditional radio circuits for medical analysis. The first two speakers in the “Healthy Radio” session will explore the use of radio circuits for early cancer detection and the analysis of DNA. The next two speakers will describe current work on communication with radio links for body-area networks (BAN) and implantable devices. This Session will conclude with a presentation on the state-of-the-art in the area of CMOS medical imaging.

OBJECTIVE

- To give an overview of the RF circuits used for biomedical applications.
- To introduce the audience to some example applications of RF circuits for bio applications.

CHALLENGE

- How are RF circuits used to communicate medical information using a secure wireless link, and how are RF circuits used for analysis and imaging?
- How will RF circuits be used in future bio and medical applications?

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STRUCTURE

CMOS RF Biosensor Utilizing Nuclear Spin Resonance – An RF Designer's Approach to Early Cancer Detection
Donhee Ham, *Harvard University, Cambridge, MA*

Integrated Radio-Frequency Biosensors for POC Applications
Ali Hajimiri, *Caltech, Pasadena, CA*

BANning Low Power Radio Design
Brian P. Otis, *University of Washington, Seattle, WA*

Wireless Telemetry Plays a Significant Role in Orchestrated Care:
Concerto™/Virtuoso™ with MICS Frequency Band
Javaid Masoud, *Medtronic, Minneapolis, MN*

Medical Imaging: RF Radio Design to the Rescue
Kris Iniewski, *CMOS Emerging Technologies., Vancouver, BC, Canada*

RECAP

The RF Subcommittee is pleased to present a Special-Topic-Session-format overview on how Radio-Frequency Circuits are used in biomedical applications. This Special Evening Topic (SET) will explore the use of RF circuits to communicate bio-sensed information and the use of radio circuits for medical diagnosis and analysis.

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TUTORIAL

Fundamentals of Digitally-Assisted RF

Bogdan Staszewski, *Texas Instruments, Dallas, TX*

OVERVIEW

RF circuits, when implemented in nanoscale CMOS, especially when integrated in an SoC, suffer from numerous issues, such as poor linearity, device mismatch, low V_{dd} headroom, high leakage, high flicker and substrate noise, etc. At the same time, digital gates and memory are ”free” and powerful, so the logical step is to use digital means to mitigate the RF circuit imperfections so that their “adjusted” performance can match or exceed that of traditional RF circuits. This Tutorial first examines opportunities for digital assistance of RF, and then presents case studies of calibration to overcome process spread, compensation due to environmental changes, performance tuning, automatic reconfigurability, and built-in self-test.

SPEAKER BIOGRAPHY

Robert Bogdan Staszewski received his PhD from the University of Texas at Dallas in 2002 for his research on RF frequency synthesis in digital deep-submicron CMOS. From 1991 to 1995, he worked at Alcatel Network Systems in Richardson, TX. He joined Texas Instruments in Dallas, TX, in 1995 where he holds an elected title of Distinguished Member of Technical Staff for his pioneering work on the Digital RF Processor (DRP™) architecture. He is currently a Chief Technical Officer (CTO) of the DRP system and design development group. He has authored and co-authored 80 journal and conference publications and holds 40 issued and 60 pending US patents.

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GIRAFE DESIGN FORUM

Towards 4G RF Transceivers

Objective

Digital cellular standards have emerged over the last 20 years. Today, 2G systems like GSM/EDGE are providing worldwide coverage for voice and basic data services. The increasing demand for true-mobile users for high-speed data services has forced the development of 3G toward HSPA. The next step in this evolution is the adoption of OFDM for cellular application in systems like WiMAX and LTE. The user equipment should be compatible to all standards from 2G up to 4G in order to provide the best possible experience to the end user. Therefore, the integration of RF transceivers has to cope with multiple frequency bands, multiple modulation schemes as well as MIMO techniques.

Audience

Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange.
The targeted participants are circuit designers and concept engineers working on wireless systems, who want to learn about the impact of 4G on the circuit and system design of RF transceivers.

Scope

Nanoscale CMOS provides the flexibility to integrate reconfigurable circuits, which are enhanced or assisted by elaborate digital techniques such as calibration, pre-distortion and modulation. Moreover, the speed of nanoscale CMOS will open the opportunity for new "Digital RF" techniques. Last but not least, the RF transceiver must address the issue of an increasing number of frequency bands in order to keep the phone form-factor constant. The elimination of bulky frontend filters and the reduction in the number of required power amplifiers will be a future challenge.

Program

The Forum will begin with a talk by **Atsushi Murase** (NTT DOCOMO) giving the operator's point-of-view of the evolution from 3G to 4G and beyond. The next speaker, **Stefan Heinen** (RWTH Aachen University), will translate the system requirements into performance parameters of the RF part of the radio as a common base for following presentations in the Forum.

The second part of the morning will be focused on the industry's view of the next generation of RF transceivers for cellular and nomadic applications. **Sven Mattisson** (Ericsson) will discuss the trends from 3G toward LTE. The presentation by **Chris Hull** (Intel) will give insight into the requirements of the RF transceiver for OFDM-based systems.

The first part of the afternoon will move the topic from the general transceiver requirements into a more-detailed discussion of the components and building blocks. The achievable figure-of-merit for the passive filters and diplexers has a major influence on the overall architecture of the radio. The newest developments in the field will be addressed by **Pasi Tikka** (EPCOS). The current trends in the reconfigurable ADCs will be covered by **Yiannos Manoli** (IMTEK).

The second presentation part of the afternoon will be devoted to the application of SDR in RF transceivers. **Asad Abidi** (UCLA) will share his view on SDR RF frontends. Finally, a more short-term industry view on real SDR soft transceivers will be presented by **Geof Dawe** (Bitwave Semiconductor). The Forum will conclude with a panel discussion addressing the question "4G Introduction: Revolution or Evolution?", where the attendees have the opportunity to ask questions of all presenters, and to share their own views.

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DESIGN FORUM

Clock Synthesis Design

Objective

One of the most critical and challenging functions present in almost every electronic system is clock generation or frequency synthesis. High-performance clocks or precise frequency references are needed in digital systems, data converters, serial data communications and wireless transceivers, to just name a few examples. Wireless systems heavily rely on the phase-locked-loop, but recent shifts into nanometer CMOS processes for RF SoCs open new architectural opportunities for all-digital and digitally-intensive implementations, both for carrier frequency synthesis and for phase-modulated transmission schemes. Data converter performance has improved so much that ADC performance is now limited as much by the clock-path noise and jitter, as by the quantization or thermal noise of the input signal path. That, of course, has led into new challenges for clock-generation systems with sub-ps or even sub-100fs rms jitter performance. The objective of this Forum is to present an overview of recent state-of-the-art developments in this crucial field, by leading experts.

Audience

Attendance is limited, and pre-registration is required. This all-day Forum encourages open information exchange. The targeted participants are circuit designers and system engineers who need to learn how the latest advances in high-performance clock generation and frequency synthesis will impact their future designs.

Scope

Clock-generation building blocks, such as phase-locked loops (PLL), have been around for many decades, and still form the core of most frequency-synthesis solutions. Increased performance and functionality requirements are driving significant innovations to the basic PLL structure and implementation. Continued scaling of semiconductor devices is further leading toward more digital-oriented realizations with significant circuit and architectural innovations. This Forum will present recent developments in frequency synthesis and clock generation by leading experts in this field.

Program

The Forum will begin with two talks that describe advanced techniques for the design of fractional-N PLLs that allow phase modulation and accurate methods for spur and noise suppression. **Ian Galton** (UCSD) will discuss phase-noise cancellation and fast calibration techniques for use in wireless communication systems. **Satoshi Tanaka** (Renesas) also shows loop calibration methods, aiming for two-point modulation schemes for transmitters.
The next three talks will focus on all-digital PLLs, focusing on critical building-block implementations as well as on full system performance for wireless-communication applications. **Mike Perrot** (SiTime) will show novel time-to-digital converter (TDC) structures that achieve sub-ps resolution, and PLL implementations exploiting that feature. **Francesco Svelto** (University of Pavia) focuses on the impact of TDC non-idealities on in-band spurious performance and the appropriate mitigation techniques. Recent trends in requirements and architectures for wireless systems will be covered by **Bogdan Staszewski** (Texas Instruments). The last two presentations will cover the challenge of low-jitter clock generation for data-converter applications. **Robert Neff** (Agilent Technologies) will discuss clock architectures for GS/s time-interleaved ADCs that require sub-ps rms jitter and calibrated timings. Finally, **Ahmed Ali** (Analog Devices) will show methods to analyze and simulate sub-100 fs jitter clocks for high-resolution high-speed ADCs, including an implementation reaching that target.

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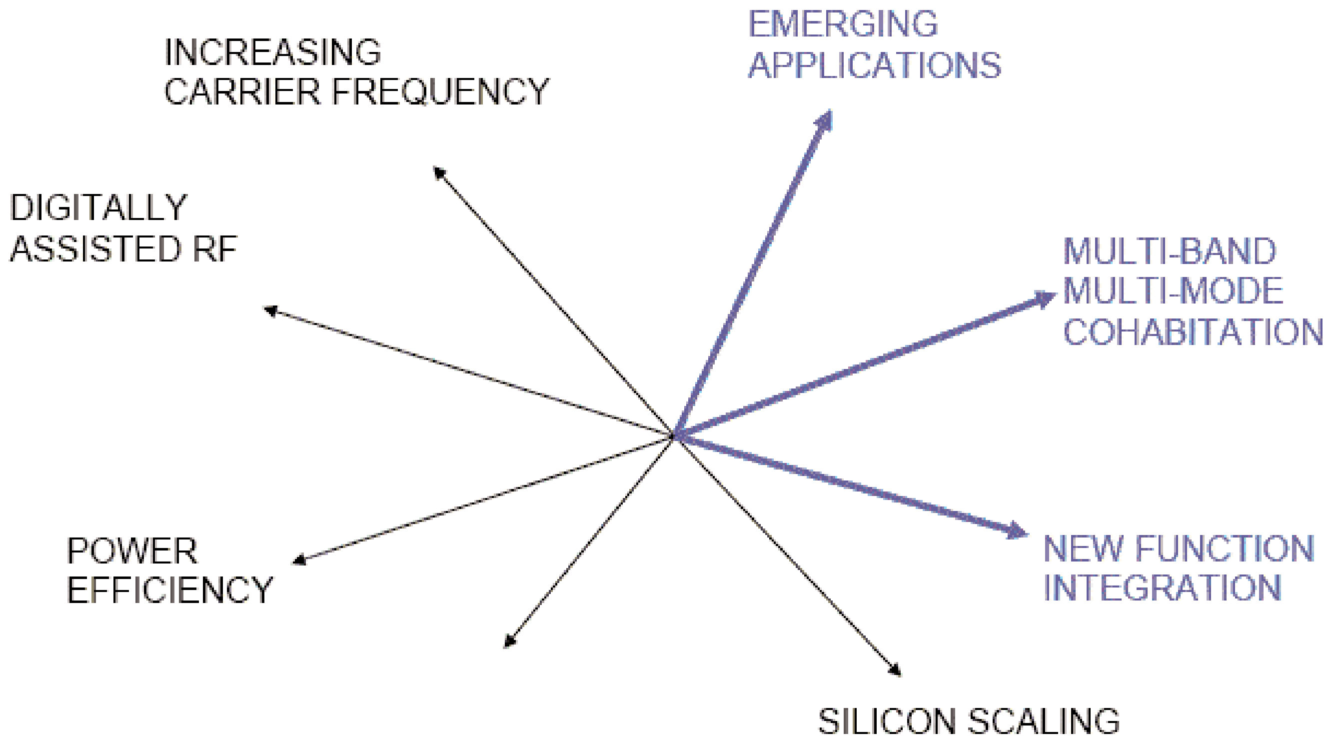
TRENDS IN RF INTEGRATED CIRCUITS



This "Spider" illustrates the expanding space of wireless applications (heavy lines) and technologies (thin lines). Silicon scaling increases the packing density of circuits in a system on a chip (e.g., multiband cellular radio transceivers) and enables new technologies such as digitally-assisted RF (the subject of a Tutorial at ISSCC 2009). Digitally-assisted RF also becomes a necessity due to the increased variability of analog/RF circuits on-chip as scaling to smaller feature size proceeds. Faster circuits permit the use of data-rate-efficient modulation schemes at higher carrier frequencies, supporting new wireless applications. Power efficiency is always critical for battery-operated devices, such as cellular phones and "push" e-mail terminals. Emerging applications (e.g, wireless HDMI via mm-wave bands, or smart dust), improved robustness for multimode/multiband communications cohabiting the same handset, and integration of new functions relies upon many of the innovations now making their way onto silicon RF circuits.

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Technology Directions Subcommittee

- Overview
- Featured Papers
- Special-Topic Session
- Tutorial

ISSCC 2009 – TECHNOLOGY DIRECTIONS

Subcommittee Chair: ***Anantha Chandrakasan***, *Massachusetts Institute of Technology, Cambridge, MA*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- A Spintronic-based oscillator with an operating range of 4GHz to 10GHz co-integrated with a broadband amplifier in 65nm for RF applications **[11.1]**
- 10Mb/s 14μW RFID with 14m operating range based on UWB uplink and UHF downlink in 0.18μm CMOS **[11.2]**
- A 2.5mW pulsed UWB wireless motion control system for a moth. **[11.3]**
- A self-sufficient tire-mounted wireless sensor integrates a Bulk Acoustic Wave-based low-power FSK 2.11GHz transceiver, an energy scavenger and a 3D vertical chip stack. **[17.1]**
- An implantable release-on-demand drug-delivery SoC in CMOS technology monolithically integrates wireless circuitry and 8 addressable 100nl reservoirs fabricated by CMOS-compatible post-IC processing. **[17.2]**
- A stabilized power supply system for low-power 3.3V electronics is realized by monolithically integrated micro fuel cell within an extended CMOS process. **[17.4]**
- A wireless power-transfer system for implanted medical devices uses an antenna area 100 times smaller than previous designs **[17.5]**
- An optically-programmable SoC integrated on a 2.6x2.6mm^2 chip provides the electronics for an autonomous microrobot. **[17.9]**
- Optical I/O architecture achieves data rate of 10Gb/s/channel at 11pJ/b energy efficiency. This technology projects increased optical integration that will reach 20Gb/s at 1pJ/bit**. [28.1]**
- Stretchable circuit sheet using low-voltage CMOS organic technology that enables EMI-distribution measurement by wrapping the flexible surface around electronic equipment with a sensitivity of -70dBm**. [28.3]**
- A proof-of-concept application and methodology based on a cellular-neural-network-contour-generation vision system emulating the processing of part of the brain. **[28.6]**
- Close-proximity inductive coupling data link between 3D-stacked 8-core processor and 1MB SRAM that achieves 19.2Gb/s and 1pJ/b. **[28.7]**

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APPLICATIONS AND ECONOMIC IMPACT

- Low-cost low-power wireless system that supports multiple RF bands **[11.1]**
- Very-high-data-rate (10Mb/s) remote-powered RFID system with an operating range of 14m has potential to open up novel remote-processing applications **[11.2]**
- By extending the wireless range that interfaces electronic systems to the neuronal system one could envision processing and actuation of prosthetic devices. **[11.9]**
- Tire-pressure-monitoring systems open a future significant application area in automobile convenience. **[17.1]**
- Novel implantable drug-delivery devices have the potential to increase the efficacy of drug therapy. **[17.2]**
- Printable circuits on fabric and open-air wireless technology are very useful to realize health monitoring systems. **[17.3]**
- Several kinds of energy-harvesting technologies, such as, thermal, vibration, piezoelectric and fuel cell will extend ubiquitous application. **[17.4; 17.6; 17.7; 17.8]**
- Low-power and low-cost testing solution via inductive-coupling that achieves 25% total-chip cost saving. **[28.2]**
- Computing with field-coupled nanomagnets with an energy-efficient programmable ferromagnetic device with less than 10aJ/switching event at 300K that eliminates interconnect, is nonvolatile and provides radiation immunity. **[28.4]**
- CMOS image sensor with TSV technology reduces volume by 55% and footprint by 36%, that achieves cost reduction of 25% in a single-chip camera product. **[28.5]**
- An architecture which takes steps toward 3D-integration multi-chip brain-like computing**. [28.6]**

SPECIAL-TOPIC SESSION

Next-Generation Energy-Scavenging Systems **[SE7]**

TUTORIAL

Display and RFID-Tag Design Using Organic Transistors **[T5]**

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Trends in Wireless Communications

A GHz Spintronic-Based RF Oscillator [11.1]

CEA-LETI; Hitachi; STMicroelectronics

A Pulsed-UWB Receiver SoC for Insect-Motion Control [11.3]

Massachusetts Institute of Technology; University of Arizona

A 500μW Neural Tag with 2μV_{rms} AFE and Frequency Multiplying MICS/ISM FSK [11.9]

University of Washington

PRESENT STATE OF THE ART (THE PROBLEM)

- With integration of multiple wireless standards, present single-frequency RF oscillators result in several standalone solutions leading to increase in area and power requirements
- Cybernetic organisms have been primarily a vision in the minds of engineers, scientists and story tellers. If they can be realized, their potential as a bio-electronic interface can be tremendous.
- Electronic-neural interfaces thus far have typically focused on short-range inductive links for power and data.

NOVEL CONTRIBUTIONS

- A Spintronic oscillator with co-integrated broadband amplifier is presented that is capable of operating from 4GHz to 10GHz is demonstrated. **[11.1]**
- For the first time, a wireless system that controls the motion of a moth while consuming less than 3mW is presented. **[11.3]**
- A 500μW fully-integrated wireless neural data transmission interface that can communicate over 15m is presented. **[11.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- A wide range oscillator has potential to reduce cost and system power leading to more energy efficient multi-purpose wireless systems **[11.1]**
- The potential for extending motion control to flight control and other intelligent activities are foreseeable in the future **[11.3]**
- By extending the wireless range of the interface electronic systems to the neuronal system one could envision processing and actuation of prosthetic devices. **[11.9]**

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Ubiquitous Sensing

A Robust Wireless Sensors Node for In Tire-Pressure Monitoring [17.1]

Infineon

A 5.2mW Self-Configured Wearable-Body-Sensor-Network Controller and a 12mW 54.9% Efficiency Wireless Powered Sensor for Continuous Health Monitoring System [17.3]

KAIST

PRESENT STATE OF THE ART (THE PROBLEM)

- Rim based tire-pressure monitoring system
- Pressure monitoring only
- Demand for a second generation sensor system with more relevant features
- Bulky heavy wired sensors and high power, high interference, inconvenient wireless sensors

NOVEL CONTRIBUTIONS

- In-tire pressure monitoring **[17.1]**
- Besides pressure, information about behavior of automobile and road conditions can be provided **[17.1]**
- Low weight (5 grams) extremely-low-power (only 30μC per reporting event), high temperature range (-40°C to +125°C), high robustness (up to 3000g) **[17.1]**
- Wireless patch-type sensors and jacket-like sensor-reader **[17.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- A major step in tire-pressure monitoring **[17.1]**
- Continuous health monitoring anywhere on your body is possible **[17.3]**

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Energy Awareness Coming of Age

An integrated Power Supply System for Low-Power 3.3V Electronics using On-Chip Fuel Cells [17.4]

University of Freiburg

An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor [17.6]

Massachusetts Institute of Technology

An Energy-Aware Multiple-Input Power Supply with Charge Recovery for Energy Harvesting Applications [17.7]

University of California, Davis

Integrated Capacitive Power-Management Circuit for Thermal Harvesters with Output Power 10 to 1000µW [17.8]

IMEC

PRESENT STATE OF THE ART (THE PROBLEM)

- Bulky and separated fuel cell
- Multiple passives (inductors, capacitors) in rectifier and DC/DC converters
- Today, power-management circuits for single-input (vibration, temperature, and light)
- Thermal power-management circuits with 58% peak efficiency

NOVEL CONTRIBUTIONS

- Monolithically integrated micro fuel cell **[17.4]**
- Shared inductor for reduced system footprint **[17.6]**
- Multi-input power-management circuits for vibration and solar energy **[17.7]**
- 0.9µW controller power consumption **[17.7]**
- Thermal power-management circuits with 70% peak efficiency over a broad input range 10 to 1000µW **[17.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost and green electronics **[17.6; 17.7; 17.8]**
- Extended operating lifetime **[17.7; 17.8; 17.9]**
- Increasing functionality for implantable and wearable ISS application **[17.7; 17.8; 17.9]**

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Directions in Computing and Signaling

Optical I/O Technology in Tera-Scale Computing [28.1]

Intel

Field-Coupled Nanomagnets for Interconnect-Free Nonvolatile Computing [28.4]

Technical University of Munich; University of Notre Dame

An Inductive-Coupling Link for 3D Integration of a 90nm CMOS Processor and a 65nm CMOS SRAM [28.7]

Keio University; Renesas; Hitachi

PRESENT STATE OF THE ART (THE PROBLEM)

- Current state of I/O signaling uses electrical signals over copper interconnect lines. The optical I/O extends the boundary.
- Current compute engines use charge-based devices that create charging and discharging currents to implement Von Neumann machines
- Inter-chip communications uses hard connections either through bond wires, C4 bumps, PCB boards or TSVs.

NOVEL CONTRIBUTIONS

- An optical I/O architecture integrated in a packaged system achieves a data rate of 10Gb/s/channel at 11pJ/b energy efficiency. Increased integration will reach the potential of this technology to 20Gb/s at 1pJ/bit **[28.1]**
- An energy-efficient field-coupled nanomagnet with radiation-immune interconnect-free non-volatile computing device consuming less than 10aJ/switching event at 300K **[28.4]**
- Demonstrating for the first time communication channels between 3D-stacked microprocessor and memory chips with contactless inductive coupling link technology. The authors show a close-proximity inductive-coupling data link between 3D-stacked 8-core processor and 1MB SRAM that achieves 19.2Gb/s and 1pJ/b. The communication channels are area-efficient at 0.15mm^2/Gb/s. These results are significantly better than conventional DDR2. They show that the microprocessor and SRAM can be from different technologies running at their respective optimized power supply voltages while communicating in close proximity via inductive coupling **[28.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- All of these technologies highlighted above, if transitioned into high volume manufacturing, could significantly impact the future of high-performance systems **[28.1; 28.4; 28.7]**

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SPECIAL-TOPIC SESSION

Next-Generation Energy-Scavenging Systems

Organizer: ***Anantha Chandrakasan,*** *MIT, Cambridge, MA*
Chair: ***Uming Ko,*** *Texas Instruments, Dallas, TX*
Co-Chair: ***Christian Enz,*** *CSEM SA, Neuchâtel, Switzerland*

OVERVIEW

- A decade of research and development in the area of energy scavenging has resulted in micro-generators based on photovoltaic, vibration, and thermal mechanisms that produce 10s to 100s of microwatts of power. These generators will power ultra-low-power portable devices ranging from sensors and embedded processors to MP3 players, medical electronics, and so on. More recently, there has also been a push towards wireless power transfer that can provide energy to higher power portable equipment or appliances.

OBJECTIVE

- To design 2nd-generation, practical energy scavenging systems that optimize the generators, the conversion circuits, as well as, the load electronics.
- To improve energy-storage elements of 2nd-generation energy-scavenging systems needed to "buffer" the variations in scavenged energy.

CHALLENGE

- How to make energy-scavenging systems pervasive, starting with ultra-low-power portable devices?
- The challenges will be power efficiency, versatility, miniaturization, weight, and cost, in order to meet the ultimate goal of energy-scavenging systems in achieving "autonomous operation", or "green portable" operation.

STRUCTURE

- **Contents include**:
  1. Advancements in various state-of-the-art micro-generators from photovoltaic, vibration, and thermal mechanism with improvements in generator efficiency, output-power density (per volume or weight) for ultra-low-power portable devices.
  2. Latest development in practical wireless power transfer that can provide power to higher power portable equipments or appliances, or for ubiquitous electronic systems such as sensor networks.
- **Speakers include:**
  1. Chris Van Hoof, IMEC, Leuven, Belgium
  2. Marc Baldo, MIT, Cambridge, MA
  3. Burkhard Habbe, Micropelt, Freiburg, Germany
  4. Takayasu Sakurai, University of Tokyo, Tokyo, Japan
- **Topics include:**
  1. State-of-Art in Vibration and Thermo-Electric Generators, Circuits and Systems
  2. Organic Photovoltaics and Solar Concentrators
  3. Thermal-Energy Scavenging Using Thin-Film TEG Devices
  4. Wireless Power

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RECAP

To advocate the latest advancement of 2nd-generation, state-of-the-art micro-generators using photovoltaic, vibration, and thermal mechanisms, with improvements in generator efficiency. To improve the output-power density through the co-optimization of conversion circuits, load electronics and storage elements, with the net result of being one step closer toward the goal of "fully-autonomous operation", or "green portable" ultra-low-power electronics. Furthermore, to acheive the goal of ubiquitous electronic systems, wireless transmission of power must advance to a new level of power density for high-power portable equipment.

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TUTORIAL

Display and RFID-Tag Design Using Organic Transistors

Eugenio Cantatore, *Eindhoven University of Technology, Netherlands*

OVERVIEW

Electronics based on organic semiconductors has demonstrated its potential to enable printing of complex electronics functions on large-area paper-like flexible surfaces. Using high-speed throughput printing instead of the conventional lithography-based manufacturing technology should also enable low-cost products. Typical organic-electronics applications are flexible displays, solar cells, light-emitting surfaces, RFIDs and physical, chemical or bio sensors. This Tutorial provides the attendee with up-to-date training on:

- basic modeling of thin-film transistors manufactured with organic semiconductors (OTFTs)
- design of organic TFT backplanes for displays
- design techniques for organic digital electronics
- design tradeoffs in RFID radios based on organic semiconductors

SPEAKER BIOGRAPHY

E. Cantatore received his PhD in Electrical Engineering from Politecnico di Bari, Italy in 1998. After a postdoctoral position at CERN, Geneva, Switzerland, where he worked on radiation-hard electronics for particle sensors, he joined Philips Research, Eindhoven, Netherlands. At Philips he designed some of the first displays based on organic-transistor backplanes and strongly contributed to the development of organic RFIDs. His research interests cover as well ultra-low-power analog CMOS design and biomedical applications. In 2007 he joined the Electrical Engineering Department of Eindhoven University of Technology. He has published more than 70 papers in international conferences and journals, has 10 patents and patent applications, and has presented invited talks on organic electronics at ESSDERC, DATE, ESSCIRC, BCTM and E-MRS. He serves in the ITPC of ESSDERC and ISSCC, which granted him in 2006 the Beatrice Winner Award for Editorial Excellence.

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NOTES

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Wireless Subcommittee

- Overview
- Featured Papers
- Special-Topic Session
- Tutorial
- Forum
  (co-sponsored by RF, and Wireless)

ISSCC 2009 – WIRELESS

Subcommittee Chair: *Trudy Stetzler, Texas Instruments, Stafford, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- The first multimode single-chip cellular transceivers for 2/2.5G and 3G **[6.2; 6.3; 6.4]**
- First published DOCSIS-3.0 SoC **[6.6]**
- First completely-integrated radio and baseband at 60GHz in CMOS **[18.5]**
- Advances in 45nm CMOS for wireless connectivity **[24.1; 24.6]**
- Highest integration UWB WiMedia PHY in 65nm CMOS **[24.2]**

APPLICATIONS AND ECONOMIC IMPACT

- Advances in 3G implementations will inspire new applications beyond Internet surfing and wireless gaming **[6.2; 6.3; 6.4]**
- DOCSIS-3.0 based cable modems will enable greater than 300Mb/s downloads by consumers **[6.6]**
- Advances in automotive radar for increased safety **[18.1; 18.2; 18.3]**
- Wireless high-speed file transfer and high-definition video will enable new markets **[18.5; 18.6]**
- Reductions in chip area and accompanying architecture with 45nm and 65nm solutions will significantly reduce cost for consumers **[24.1; 24.2; 24.6]**

SPECIAL-TOPIC SESSION

Things All RFIC Designers Should Know (But Are Afraid To Ask) **[SE5]**

TUTORIAL

Managing Linearity in Radio-Receiver Frontends **[T9]**

FORUM

GIRAFE: Towards 4G RF Transceivers **[F3]**
(co-sponsored by RF and Wireless)

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Cellular and Tuner

A SAW-Less Multiband WEDGE Receiver [6.2]

ST-NXP Wireless; Ericsson Mobile Platforms

Single-Chip Multiband WCDMA/HSDPA/HSUPA/EGPRS Transceiver with Diversity Receiver and 3G DigRF Interface Without SAW Filters in Transmitter / 3G Receiver Paths [6.3]

Skyworks Solutions; Spectra-Linear

Single-Chip RFCMOS UMTS/EGSM Transceiver with Integrated Receive Diversity and GPS [6.4]

Qualcomm

An Embedded 65nm CMOS Low-IF 48MHz-to-1GHz Dual Tuner for DOCSIS-3.0 [6.6]

Broadcom

PRESENT STATE OF THE ART (THE PROBLEM)

- Mobile devices are no longer just phones or PDAs, but rather, data-centric multimedia computers with Internet access for consumer and business applications. High-speed access is needed not only in urban areas but as a continuous wireless service. This is enabled only by using advanced third- generation cellular-access technologies having several Mbit/s data rate and capability of operating in multiple bands to achieve global coverage. Also, the technology is able to support seamless high-speed access in portable computers.
- Packet data traffic in mobile networks is growing rapidly and drives the capacity requirements of mobile cellular networks. Once the networks have been upgraded to the most modern 3G technologies, that is. HSPA (high-speed packet access), the mass market for chipsets supporting all legacy cellular-operation modes is established.
- Frequency allocations for second- and third-generation systems are globally fragmented. To support consumers on all continents, the chipsets must support more than 10 different frequency-band combinations.
- The need for even higher-speed Internet connections for consumers is not yet satisfied. Cable data services are advancing to data rates up to 300Mb/s with DOCSIS-3.0.

NOVEL CONTRIBUTIONS

- Highest integration level reported for cellular 2G/3G multi-mode transceivers **[6.2; 6.3; 6.4]**
- Several Mb/s downlink data rates for cellular communications **[6.2; 6.3; 6.4]**
- First highly integrated tuner for DOCSIS-3.0 cable modem **[6.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Multiband chipsets enable seamless mobile high-speed Internet access with global coverage **[6.2; 6.3; 6.4]**
- Mobile Internet facilitates ultimate independence of physical location in business and leisure **[6.2; 6.3; 6.4]**
- Ultra-high-speed data services will bring the experience of home Internet into a new era **[6.6]**

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Ranging and Gb/s Communication

A Fully-Integrated 24GHz UWB Radar Sensor for Automotive Applications [18.1]
University of Catania; STMicroelectronics

A Single-Chip Dual-Band 22-to-29GHz/77-to-81GHz BiCMOS Transceiver for Automotive Radar [18.2]
University of California, Irvine

A 77GHz Transceiver in Standard 90nm CMOS [18.3]
Fujitsu Laboratories

A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry [18.5]
University of California, Berkeley

A Low-Power Fully-Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly [18.6]
National Taiwan University

PRESENT STATE OF THE ART (THE PROBLEM)

- Commercial-grade automotive radars typically implemented in GaAs
- Radars deployed at 24 and 77GHz use separate solutions
- Components for Gb/s wireless communications are available, but no complete integrated radios exist in CMOS.
- Digital-baseband processing, (for example, equalization for channel impairments), are not currently employed for 60GHz systems.

NOVEL CONTRIBUTIONS

- Dual-band car radar for worldwide operation **[18.2]**
- Low-cost CMOS technology is used for the 77GHz radar **[18.3]**
- Integration of complete 60GHz radio transceiver in CMOS includes transmitter, receiver, frequency synthesizer and baseband **[18.5]**
- High-speed baseband time-domain equalizer to counter channel impairments **[18.5]**
- Assembly technique for CMOS radio and low-cost antenna at 60GHz **[18.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost silicon-based radar modules **[18.1; 18.2; 18.3]**
- Safety improvement for cars **[18.1; 18.2; 18.3]**
- Will enable low-cost CMOS transceivers for wireless high-definition video and quick file transfers **[18.5; 18.6]**
- Antenna assembly approach for low-cost, manufacturable 60GHz module **[18.6]**

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Wireless Connectivity

A 2mm^2 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS [24.1]

IMEC; KU Leuven

A 65nm CMOS Inductorless Triple-Band-Group WiMedia UWB PHY [24.2]

NXP Semiconductors; ST-NXP Wireless

A 1.1V 5-to-6GHz Reduced-Component Direct-Conversion Transmit Signal Path in 45nm CMOS [24.6]

University of Washington; Intel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- The number of wireless applications with their corresponding standards is increasing continuously. Customers want evermore functionality from their handheld devices
- The latest multimedia applications come with ever-increasing data-rate requirements. The connection of these multimedia devices without cables requires high wireless-transmission rates.
- The pressure to reduce the price of products is continuous. This results in the need for new circuits and architectures for development in advanced CMOS processes.

NOVEL CONTRIBUTIONS

- High level of re-configurability addressing multiple standards in a single receiver **[24.1]**
- High-speed wireless data-communication up to 480Mb/s **[24.2]**
- Low area by using novel architectures and/or avoiding coils [**24.1; 24.2; 24.6]**
- Use of the most-advanced commercially-available CMOS technology **[24.1; 24.6 (45nm), 24.2 (65nm)]**
- High-linearity and low-noise receiver eases the coexistence of multiple transceivers on a chip **[24.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Seamless connectivity to various 2G/3G/4G systems for handheld devices **[24.1]**
- High-speed wireless connection to transfer multimedia contents between various devices **[24.2]**
- Improved coexistence between various wireless transceivers on a single chip **[24.6]**

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SPECIAL-TOPIC SESSION

Things All RFIC Designers Should Know (But Are Afraid To Ask)

Co-Organizers & Co-Chairs: **David Su**, *Atheros, Santa Clara, CA*
Arya Behzad, *Broadcom, San Diego, CA*

OVERVIEW

- The scaling of CMOS technology has enabled the proliferation of single-chip wireless systems-on-a-chip (SoCs) that integrate RF, analog, and digital circuits to form complete system solutions. Most high-volume wireless systems, ranging from cellular phones to wireless local-area networks, are based on single-chip solutions. Much of the attention at conferences, such as ISSCC, has been focused on the design of wireless SoCs. However, bringing a wireless SoC to market requires significant technical knowledge beyond IC design.

OBJECTIVE

- To provide an introduction of topics that are typically not well understood by RFIC designers, in part, because they are not sufficiently emphasized in most college curricula.
- To cover information that is critically important to the successful productization of wireless systems.

CHALLENGE

- How to achieve robust electrostatic-discharge performance?
- How to design a high-performance yet low-cost antenna?
- What packages can provide high pin counts and good RF characteristics?
- How to verify the correct functionality of the RF, analog, and digital circuits without running SPICE on the entire chip?
- How to test an entire wireless system in seconds?

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STRUCTURE

"ESD Design Challenges for SoC and RF"
Charvaka Duvvury, *Texas Instruments, Dallas, TX*
Rapid scaling of the silicon technologies has turned dealing with ESD into a nightmare for the IC designer. This is mainly due to: 1) Smaller geometries that make it more difficult at each node to design for the accepted ESD levels, and 2) Circuit-design advances for high-speed performance (for HSS and RF) that place restrictions on tolerable capacitance from the ESD device. These are further exacerbated by the trend towards SoC, high-pin-count packages, and other factors. This presentation will address the fundamentals of ESD models, and protection design techniques. This will be followed by outlining the common protection devices that are currently used at 65/45nm technologies and the impact of circuit design on the available ESD design window. Finally, the paradigm shift that is taking place across the industry to lower the ESD levels to accommodate IC design performance in general, and especially for RF, will be introduced.

"Antennas: From Fundamental Limitations to Design"
Nicolaos G. Alexopoulos, *Broadcom, Irvine, CA*
Information-processing components and systems are enabled by the transport of electromagnetic energy either in terms of guided waves in circuits or waveguides and propagating waves in space. Antennas are the transducer elements that transform guided waves to space waves and vice-versa. They act as a load to a transmitting system or as a generator with internal impedance for a receiving system. In antenna theory and design, precise knowledge of the spatial current distribution is necessary for the accurate design of antenna parameters, such as, input impedance, gain, directivity, efficiency, polarization, and bandwidth. Accuracy in input-impedance design is a first-order effect, while for the radiation pattern is a second-order effect in the context of current distribution. In general terms all AC circuits act as antennas, but with an efficiency that depends on the ratio of the circuit's largest dimension to wavelength. The presentation will discuss fundamentals in design methods relying on both analysis and synthesis procedures for single elements, as well as, array systems. A particular design using meta-material effects for wireless communications will be discussed.

"Packaging Options for Wireless SoCs"
Lawrence Larson, *University of California, San Diego, CA*
The performance of a radio-frequency integrated circuit can be dramatically affected by the package environment, yet packaging technology has received comparatively little attention compared to IC fabrication technology or RFIC design. As RF systems move to higher frequencies, and more exacting performance standards, the role of the package becomes increasingly important. At the same time, recent developments in packaging technology provide for new opportunities for high-performance single-chip system implementations. This presentation summarizes the key developments and trends in RFIC packaging, with particular attention to improvements in plastic package design, low- temperature co-fired ceramics (LTCCs), flip-chip approaches, and system-in-package (SiP) implementations.

"CAD for RFIC/SoC: What You Don't Know CAN Really Hurt You!"
Ravi Subramanian, *Berkeley Design Automation, Santa Clara, CA*
Successfully designing today's radios-on-a-chip (RoCs) and systems-on-a-chip (SoCs) requires efficiently managing the problems that come with design complexity – the sheer number of devices, the impact of noise, the number of operating modes, the impact of variability on performance, and the list goes on. With simulation and validation taking over 75% of project schedules, CAD tools are critical to efficiently managing the complexity and delivering predictability. In this presentation, we will cover the five things that all designers should know (and are afraid to ask) about this subject: (1) Where is most of the time on these projects really spent, and are the CAD breakthroughs following the pain?; (2) Using abstraction to manage complexity – does it really work?; (3) How can one accurately characterize complex RF blocks in nanometer technologies?; (4) What is state-of- the-art today for full-circuit and top-level validation? (Hint: It is not what you learned in college!) and (5) What problems are today's tools poor at solving?

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Wireless SoC Production Test Concepts for RFIC Designers

Joe Kelly, ***Verigy, Neptune City, NJ***

RFIC designers could benefit from understanding the many concepts of RF production testing and ATE (Automated Test Equipment). Primary focal points of this presentation are the impact of increasing levels of device integration, and the fact that RF production testing is driven by Cost-of-Test (CoT). RF devices at the final stages of production, that is, test, are no longer RF-only devices. They have combined RF, analog and digital baseband, and digital features, all working together. Considering that, ATE must be able to work within these domains, and production measurements need to be made that can correlate back to the device design parameters. Concepts in production testing such as system-level testing, multi-site testing, parallel and concurrent testing, load boards (DIBs), and key tests for each of the common RF device architectures, are discussed. Also presented are changes in the ATE industry and RF testing that are expected within the next five years.

RECAP

Five experts will address electrostatic discharge (ESD) protection techniques, practical antenna design, RF packaging, CAD tools for design and validation, as well as wireless production test. This evening session should provide practicing RFIC designers with an introduction to the basic concepts and, perhaps, answer some of the questions we have all been afraid to ask…

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TUTORIAL

Managing Linearity in Radio Frontends

Ranjit Gharpurey, *University of Texas, Austin, TX*

OVERVIEW

Radio-frontend linearity requirements can pose a major challenge in the design of receivers for several commercial wireless systems. In this presentation, we will explore circuit techniques and architectures that address this issue, with an emphasis on approaches that reduce the requirement for off-chip passive filters. Basic concepts related to frontend dynamic range, including noise performance and mechanisms for nonlinearity-induced performance degradation will be introduced. Design approaches that are useful for improving receiver linearity, such as feedback and feedforward; the use of on-chip filters and frequency-selective terminations; and approaches that utilize multiple receiver paths will be presented, along with relevant examples from practical wireless systems. The impact of these techniques on dynamic range will be considered.

- **Circuit techniques and architectures for linearity enhancement**
- **Nonlinearity-induced degradation mechanisms**
- **Concepts for frontend dynamic-range improvement**
- **Feedback and feedforward linearization techniques**
- **On-chip filters and frequency-selective terminations**
- **Multiple receiver paths**
- **Design examples from practical systems**

SPEAKER BIOGRAPHY

Ranjit Gharpurey is an Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. His primary research interests are in the areas of high-frequency and high-speed circuit design with emphasis on RFIC design for wireless applications, and on studies of parasitic noise sources in integrated circuits. He had 8 years of industrial experience with Texas Instruments prior to his academic career. He received his PhD from the University of California at Berkeley in 1995.

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GIRAFE DESIGN FORUM

Towards 4G RF Transceivers

OBJECTIVE

Digital cellular standards have emerged over the last 20 years. Today, 2G systems like GSM/EDGE are providing worldwide coverage for voice and basic data services. The increasing demand for true-mobile users for high-speed data services has forced the development of 3G toward HSPA. The next step in this evolution is the adoption of OFDM for cellular application in systems like WiMAX and LTE. The user equipment should be compatible to all standards from 2G up to 4G in order to provide the best possible experience to the end user. Therefore, the integration of RF transceivers has to cope with multiple frequency bands, multiple modulation schemes as well as MIMO techniques.

AUDIENCE

Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange.

The targeted participants are circuit designers and concept engineers working on wireless systems, who want to learn about the impact of 4G on the circuit and system design of RF transceivers.

SCOPE

Nanoscale CMOS provides the flexibility to integrate reconfigurable circuits, which are enhanced or assisted by elaborate digital techniques such as calibration, pre-distortion and modulation. Moreover, the speed of nanoscale CMOS will open the opportunity for new “Digital RF” techniques. Last but not least, the RF transceiver must address the issue of an increasing number of frequency bands in order to keep the phone form-factor constant. The elimination of bulky frontend filters and the reduction in the number of required power amplifiers will be a future challenge.

PROGRAM

The Forum will begin with a talk by **Atsushi Murase** (NTT DOCOMO) giving the operator’s point-of-view of the evolution from 3G to 4G and beyond. The next speaker, **Stefan Heinen** (RWTH Aachen University), will translate the system requirements into performance parameters of the RF part of the radio as a common base for following presentations in the Forum.

The second part of the morning will be focused on the industry’s view of the next generation of RF transceivers for cellular and nomadic applications. **Sven Mattisson** (Ericsson) will discuss the trends from 3G toward LTE. The presentation by **Chris Hull** (Intel) will give insight into the requirements of the RF transceiver for OFDM-based systems.

The first part of the afternoon will move the topic from the general transceiver requirements into a more-detailed discussion of the components and building blocks. The achievable figure-of-merit for the passive filters and diplexers has a major influence on the overall architecture of the radio. The newest developments in the field will be addressed by **Pasi Tikka** (EPCOS). The current trends in the reconfigurable ADCs will be covered by **Yiannos Manoli** (IMTEK).

The second presentation part of the afternoon will be devoted to the application of SDR in RF transceivers. **Asad Abidi** (UCLA) will share his view on SDR RF frontends. Finally, a more short-term industry view on real SDR soft transceivers will be presented by **Geof Dawe** (Bitwave Semiconductor).

The Forum will conclude with a panel discussion addressing the question “4G Introduction: Revolution or Evolution?”, where the attendees have the opportunity to ask questions of all presenters, and to share their own views.

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NOTES

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Wireline Subcommittee

- Overview
- Featured Papers
- Special-Topic Session
- Tutorial
- Forum
- Trends and Chart

ISSCC 2009 – WIRELINE

Subcommittee Chair: *Franz Dielacher, Infineon Technologies, Villach, Austria*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Subharmonically injection-locked PLLs for ultra-low-noise clock generation **[5.2]**
- A VDSL2 CPE AFE in 0.15µm CMOS with integrated line driver **[5.10]**
- A scalable 3.6-to-5.2mW 5-to-10Gb/s 4-tap DFE in 32nm CMOS **[10.1]**
- A 4-channel 10.3Gb/s backplane transceiver macro with 35dB equalizer and sign-based zero-forcing adaptive control **[10.5]**
- A 40Gb/s multi-data-rate CMOS transceiver with SFI-5 interface for optical transmission systems **[21.1]**
- An 80mW 40Gb/s 7-tap T/2-spaced FFE in 65nm CMOS **[21.4]**

APPLICATIONS AND ECONOMIC IMPACT

- Power dissipation has become a key issue in communication circuits as the overall energy consumption in the worldwide Internet infrastructure gets more and more attention. A number of developments presented here demonstrate record-low power-dissipation **[5.1; 5.5; 5.9; 10.1; 10.2; 16.3]**
- In many cases, replacing traditionally analog circuit blocks by advanced digital circuitry can improve the performance of high-speed communication circuits, thanks to the scaling down of CMOS technologies. Improved performance from digital operation will be demonstrated in several developments to be presented **[5.1; 5.3; 5.5; 21.6; 21.7]**
- Combining high-speed communication blocks with various types of drivers, such as those for LCD displays or very-high-speed digital subscriber lines (VDSL), present significant challenges in dealing with noise and interference from the driven devices. Solutions to these challenges can be found in **[5.7; 5.9; 5.10; 10.7]**
- Thanks to advanced submicron (with feature sizes currently from 65nm to 32nm) CMOS circuit performance is approaching speeds of 100GHz. Building blocks necessary for such speeds are already being demonstrated. CMOS circuit capability will enable the next generation of communication circuits that will demonstrate 100Gb/s serial transmission. **[16.2; 16.3; 16.4; 16.5]**

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SPECIAL-TOPIC SESSION

Will ADCs Overtake Binary Frontends in Backplane Signaling? [SE3]
Receivers with an ADC frontend are now competing against conventional receivers that have a binary frontend, which occupy larger silicon area and possibly consume more power. This session discusses the pros and cons and the design trade-offs of the two approaches to backplane electrical signaling. Each of our five panelists will predict whether the switchover to ADC-based designs will become inevitable.

TUTORIAL

CMOS Circuit Techniques for High-Speed Wireline Transceivers [T10]
This Tutorial covers modern CMOS design techniques for high-speed wireline communications operating at tens of Gb/s. Starting from an architecture-level illustration and explaining the necessity and applications of high-speed building blocks, this Tutorial presents popular design techniques and typical considerations for voltage-controlled oscillators, frequency dividers, and broadband amplifiers. Design methodologies will be discussed to illustrate circuit optimization. The Tutorial concludes with a case study to present state-of-the-art circuits.

FORUM

ATAC: High-Speed Interfaces [F5]
This Forum will cover the system challenges, and circuit solutions available to address chip-to-chip, board-to-board and system-to-system communications at data rates ranging from 3Gb/s to 40Gb/s. The performance limits and trade-offs of various equalization techniques, including transmit pre-emphasis, linear receive equalizers, decision feedback equalizers (DFE), and analog-to-digital conversion (ADC) followed by digital signal processing (DSP), will be presented. The overarching theme will be the design of circuits to enable next-generation data rates in both electrical and optical systems.

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Potpourri: PLL, Optical, DSL

Subharmonically Injection-Locked PLLs for Ultra-Low-Noise Clock Generation [5.2]

National Taiwan University; Industrial Technology Research Institute

A VDSL2 CPE AFE in 0.15µm CMOS with Integrated Line Driver [5.10]

Marvell; University of Pavia

PRESENT STATE OF THE ART *(THE PROBLEM)*

- There is a constant pressure to increase the robustness and precision of wireline systems, especially by decreasing the jitter generated in the transceivers. In particular, new techniques are needed to help re solve the difficult trade-offs that often come up in frequency-multiplier phase-locked- loop (PLL) blocks.
- Delivering high power (more than 14dBm) efficiently and with high bandwidth over a long distance in a 100Ω-terminated line, is very difficult to do using CMOS circuits, due to the low supply voltage available.

NOVEL CONTRIBUTIONS

- A new fundamental discovery of how injection-locking can be used in PLLs results in significantly lower random jitter than can be achieved by conventional techniques **[5.2]**
- An analog front-end (AFE) with a 14-bit ADC and line driver have been integrated onto a single CMOS chip. Novel circuit topologies for the line driver allow operation at 7V supply voltages without subjecting individual thick-oxide transistors to breakdown conditions. In addition, very high linearity is achieved. **[5.10]**

CURRENT AND PROJECTED SIGNIFICANCE

- Lower random jitter will allow better precision in PLLs while dissipating very low power. **[5.2]**
- A completely integrated VDSL2 AFE transceiver solution is an important development. **[5.10]**

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Multi-Gigabit Serial Links and Building Blocks

A Scalable 3.6-to-5.2mW 5-to-10Gb/s 4-Tap DFE in 32nm CMOS [10.1]

Intel

A 4-Channel 10.3Gb/s Backplane Transceiver Macro with 35dB Equalizer and Sign-Based Zero-Forcing Adaptive Control [10.5]

Fujitsu Labs

PRESENT STATE OF THE ART (THE PROBLEM)

- A number of applications, including video streaming, demand both high bit rate and very low-power dissipation.
- Transmission over a backplane made of legacy materials (e.g., FR4) presents a significant challenge into high-speed transceivers operating at bit rates of 10Gb/s and higher.

NOVEL CONTRIBUTIONS

- A number of novel circuit-design techniques, coupled with the use of an advanced 32nm CMOS technology, allows the design of a 10Gb/s equalizer that dissipates only 5.2mW. **[10.1]**
- Analog equalization techniques, including FFE and DFE, provide good equalization of challenging channels while dissipating reasonable power compared to digital equalization techniques. **[10.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- 10Gb/s operation with extremely-low power has been achieved. **[10.1]**
- Higher speed and better precision can be achieved, even when existing legacy infrastructure is used. **[10.4]**

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High-Speed and mm-Wave Circuits

An 18Gb/s Duobinary Receiver with a CDR-Assisted Decision Feedback Equalizer [16.1]

NEC

A 43.7mW 96GHz Phase-Locked-Loop in 65nm CMOS [16.2]

National Taiwan University

PRESENT STATE OF THE ART (THE PROBLEM)

- Limited bandwidth available with transmission media for data rates above 10Gb/s
- Tight timing constraints of DFE implementations
- Limited operation frequency of VCOs and frequency dividers in CMOS technology

NOVEL CONTRIBUTIONS

- Relaxed timing requirements for DFE in a duobinary-signaling scheme **[16.1]**
- First implementation of a 96GHz PLL **[16.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Technique enables transmission of high-speed data over lossy media **[16.1]**
- Basic technique enables the design of PLLs for mm-wave wireline/wireless applications **[16.2]**

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10Gb/s to 40Gb/s Transmitters and Receivers

A 40Gb/s Multi-Data-Rate CMOS Transceiver Chipset with SFI-5 Interface for Optical Transmission Systems [21.1]

NEC

An 80mW 40Gb/s 7-tap T/2-spaced FFE in 65nm CMOS [21.4]

University of California, Irvine

PRESENT STATE OF THE ART (THE PROBLEM)

- Building blocks for 40Gb/s have been implemented in SiGe and in CMOS, but they have not been integrated into a complete transceiver.
- 40Gb/s feedforward-equalizer (FFE) implementations in CMOS have been limited to 3 taps.

NOVEL CONTRIBUTIONS

- A fully-integrated 40Gb/s transmitter and receiver chipset is implemented in CMOS **[21.1]**
- The first 40Gb/s 7-tap FFE in CMOS **[21.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Chipset will enable the deployment of inexpensive, and low-power enterprise and metro optical networks at 40Gb/s **[21.1]**
- CMOS design enables the design of equalized 40Gb/s transceivers for long-haul optical links **[21.4]**

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SPECIAL-TOPIC SESSION

Will ADCs Overtake Binary Front-Ends in Backplane Signaling?

Organizer: **Ali Sheikholeslami,** *University of Toronto, Canada*
Co-organizer: **Robert Payne,** *Texas Instruments, Dallas, TX*

Chair: **Jerry Lin,** *Ralink Technology, Hsinchu, Taiwan*

OVERVIEW

Receivers with an ADC front-end are now competing with conventional binary front-end receivers, but they occupy larger silicon area and possibly consume more power. This Session discusses the pros and cons and the design tradeoffs between the two approaches in backplane electrical signaling. Each of our five speakers will predict whether the switchover to ADC-based designs will become inevitable.

OBJECTIVE

- To debate the current state-of-the art in backplane receivers.
- To compare ADC-based receivers to binary receivers in terms of power, area, and performance.
- To predict when or whether ADC-based receivers will dominate the market.

CHALLENGES

- Backplane applications demand for higher throughputs across existing high-loss channels.
- The demand for increased bandwidth is growing faster than the improvements in backplane technology.
- Can we rely on material improvements much longer?
- How will we get 50Gb/s across cabinet-sized distances?

CONTROVERSY

- History tells us that ADC-based systems will become the only viable solution, for example, think of hard-disk-drive read channels. Is this inevitable?
- What solutions are being developed today?
- What are customers purchasing? Where is the money?

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STRUCTURE

ADCs will Dominate at 20Gb/s and Beyond

Ichiro Fujimori, *Broadcom, Irvine, CA*

The advancements in CMOS technology have made interleaved ADCs, assisted by calibration, a viable solution for wired transceivers at a 10Gb/s data rate. Combined with the scaling of the DSP engine, the die area, and power of the ADC-based front-end has been rapidly approaching that of a conventional binary front-end.

For applications at 10Gb/s or lower, where most standards define “open-eye” compliance based on NRZ coding, the binary front-end remains the most economical solution. The ADC front-end is limited to niche situations like legacy backplanes and 10G LRM.

At data rates of 20Gb/s and beyond, an ADC front-end becomes the main stream. Analog equalization will be prohibitive in many applications even with the advancement in backplane technologies. The main driver is the adoption of multi-level coding, which effectively lowers the required bandwidth, that is, the Nyquist rate. Since at lower frequencies less equalization gain is needed to compensate channel loss, the quantization noise budget is relaxed for the target SNR. As a result, for higher-order coding (more levels), the ADC complexity will show a flatter dependency to data rate. Preliminary analysis over a moderate backplane shows that an ADC front-end with 32-PAM coding (pulse amplitude modulated signal with 32 levels) can be a common choice at 100Gb/s data rate. This transition to higher-order coding has been seen before in other highly successful technologies such as voice-band modems and digital subscriber lines.

Are Serdes, as We Know Them, Dead?

Andy Joy, *Texas Instruments, Northampton, Northants, United Kingdom*

The general drift towards ADCs in Serdes is seen by many as inevitable as what happened in the past with the HDD read channel, for example. However, I think we have a slightly different case here where channel speeds and equalization requirements are pushing forward at different rates. The need for an ADC on the front-end is only justified when complicated equalization is needed. This happens to be the case today where legacy backplanes are requiring more and more techniques to squeeze the most out of them. There will then be a new set of backplanes developed with better material and more research will lead to higher speeds. The newer backplanes will then allow a certain level of binary front-ends. These will then turn into the next generation of legacy and ADCs will again bear fruit.

When and how this will change in the future? How far can we rely on material improvements, and how will we transfer data at speeds of 50Gb/s across cabinet-sized distances? That is, are serdes as we know them dead?

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Let the Market Decide

Michael Sorna, ***IBM, Hopewell Junction, NY***

The overriding factor in determining whether a binary or an ADC-based approach will be a better solution is the nature of the market that a given serial link will serve. For high-link-count backplane applications, binary serial-link solutions will tend to be preferred to ADC-based ones. This preference will be determined by system-driven critical metrics and application constraints for links, including: present and expected future channel sets, tight area budgets, and tight power budgets. As the disparity between serial-data rate and supportable digital-logic clock frequencies grows, managing post-processing-driven latency associated with ADC-based links will emerge as a further challenge. ADC-based links are likely to thrive in areas where equalization requirements are more exotic and link counts are lower, including, for example, realizations of electronic dispersion compensation for optical systems. In the near-to-medium term, the area and power cost associated with highly sophisticated ADC-enabled equalizers will limit the degree to which this approach will be adopted in the mainstream backplane environment.

History Repeats Itself: ADCs Will Dominate

Hirotaka Tamura, ***Fujitsu Laboratories, Kawasaki, Japan***

In the mid-to-late 90s, there was controversy over ADC frontends versus pure analog ones for hard-disk drive (HDD) read-channel ICs. ADC-based front-ends won over analog counterparts, because the increasing bit density in the recording media called for complex signal processing that can only be achieved with digital circuits. History just repeats itself! The data rate, or bit density per unit time, is increasing while the loss in the backplane channel is not improved at the same pace. This works in favor of the ADC approach in the field of high-speed transceivers.

Are They Really That Different?

Jared Zerbe, ***Rambus, Los Altos, CA***

The only rational answer to this question is the classic engineering response: “it depends!“. This time, however, it depends on three critical factors — the environment, the desired speed, and the current-performance process node. The reason we now have ADC frontends on backplane transceivers is because process evolution, marching along with a relentless obedience to Moore’s Law with the entire industry behind it, has outpaced real demand for higher- performance links and backplane-systems upgrades. How long has 10Gb/s been “the number” for backplanes? If customers were demanding 20Gb/s today, we would not see ADCs in the solution space: ADCs would simply blow any realistic power and area budget.

Independently, when building either a bit-serial or high-speed ADC front-end for a medium-equalization performance link one rapidly comes to the conclusion that they are fundamentally not that different. I will point out some of the few real differences, and advantages and disadvantages.

Panel-format discussion with speakers and audience.

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TUTORIAL

CMOS Circuit Techniques for High-Speed Wireline Transceivers

Jri Lee, *National Taiwan University, Taipei Taiwan*

OVERVIEW

- General consideration of high-speed blocks
- Voltage-controlled oscillators
- Frequency dividers
- Broadband amplifiers
- Design methodology and case study

SPEAKER BIOGRAPHY

Jri Lee received the MS and PhD degrees in electrical engineering from the University of California, Los Angeles (UCLA), both in 2003. He joined National Taiwan University (NTU) in 2004, where he is currently an Associate Professor of electrical engineering. He is now serving on the Technical Program Committees of the ISSCC, Symposium on VLSI Circuits, and A-SSCC. Professor Lee received the Beatrice Winner Award for Editorial Excellence at ISSCC 2007, the Takuo Sugano Award for Outstanding Far-East Paper at ISSCC 2008, and the NTU Outstanding Teaching Award in 2007 and 2008.

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FORUM

ATAC: High-Speed Interfaces

OBJECTIVE

The goal of this Forum is to provide circuit designers with an opportunity to learn from leading experts about the design issues and system-level challenges that arise in the development of transceivers for a wide cross-section of application areas and associated standards. The transceivers for these different standards share some similarities but also marked differences. The audience will have an opportunity not only to learn about these similarities and differences, but also to develop an understanding as to how they arose and why they exist. Additionally, the audience will be able to garner insight into where these standards are heading, and what challenges lie ahead, in the future.

AUDIENCE

This Forum is targeted at designers who are interested in learning about the design issues and system-level challenges that must be overcome in the development of a variety of standards-based transceivers.

SCOPE

The standards covered will include PCI Express 3, USB 3.0, SAS-2, HDMI, 10GBASE-T and 10GbE small-form-pluggable (SFP+). Leading experts will describe the unique design challenges of each of these standards and the transceiver techniques required to overcome them. Additionally, the speakers will provide insight into what the future holds for these standards.

PROGRAM

The first speaker, **Gerry Talbot** (AMD), will cover PCI-Express (PCIE) electrical signaling. He will provide an overview of PCIE including its evolution from 2.5Gb/s to 8Gb/s, covering key specification aspects and will describe the enabling technologies for this standard to work. The second speaker, **Mike Pennell** (SMSC), will provide a physical-layer perspective for the latest universal serial bus (USB) interface, USB 3.0. He will focus on physical layer characteristics and challenges including power management, clocking, cable and connector, signaling, transmit and receive equalization, and compliance testing. The third speaker, **Robert Elliott** (HP), will cover transceivers for the serial-attached SCSI (SAS) standard starting with the physical layer established in SAS-1 and then moving on to the physical layer of SAS-2 which includes a doubling of the physical-link rate to 6Gb/s while supporting lossier, more challenging interconnects. The fourth speaker, **Jon Rogers** (Gennum), will address the transceiver challenges presented by the high-definition multimedia interface (HDMI) standard and the related Society of Motion Picture and Television Engineers (SMPTE) video-transmission standard. The fifth speaker, **George Zimmerman** (Solarflare), will present insights into transceiver design for the IEEE 10GBASE-T standard. He will focus on design considerations to minimize power and maximize the utility of a single-chip 10GBASE-T solution. The sixth speaker, **Ali Ghiasi** (Broadcom), will discuss the evolution of I/O technology for 10 gigabit ethernet (GbE) to the small-form-pluggable (SFP+) form factor which utilizes serializer/deserializer framer interface (SFI) for its electrical interface and leverages electronic dispersion compensation to compensate for both electrical, as well as optical dispersions. Additionally, he will discuss trends for higher speeds, 40GbE, 100GbE, as well as 17Gb/s Fibre Channels.

Finally, the Forum will conclude with a Panel Discussion in which these experts can voice their opinions on cutting-edge-design issues and the standards future that lies ahead!

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TRENDS IN WIRELINE COMMUNICATIONS

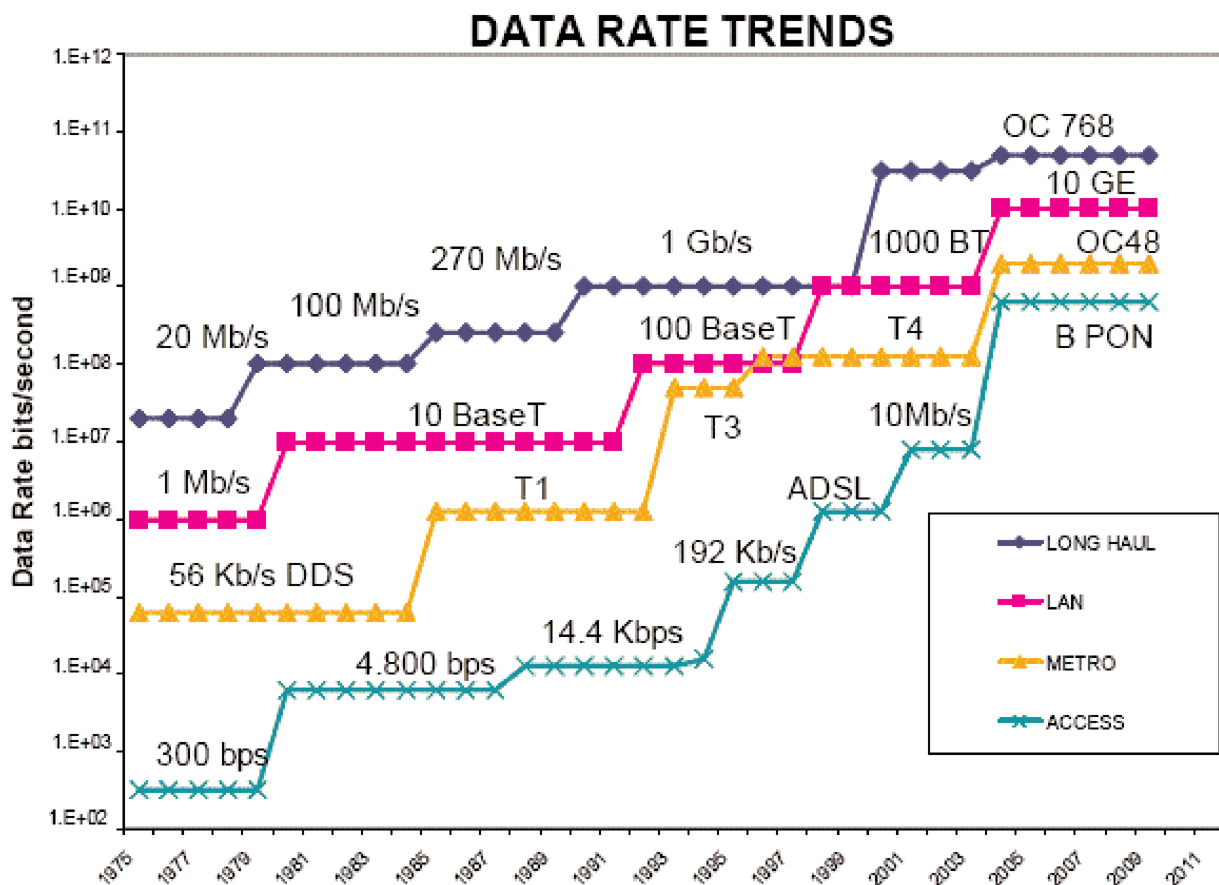
Wireline technologies are still driven by a continuing demand for more bandwidth, resulting from an increased use of high bandwidth services such as, YouTube. This demand can be fulfilled on the one hand by CMOS feature-size scaling to 32nm and on the other hand by innovative exploitation of more conventional, but less, expensive technology nodes. In addition, new techniques are emerging, such as, passive optical networks (PONs), targeting home connections with triple play services. The Wireline Sessions at the ISSCC 2009 will present papers reflecting these trends.

Network throughput is being upgraded to support consumer demand for “triple-play” (voice, video, and data). The deployment of gigabit passive optical networks (GPONs) provides home access data rates up to 10Gb/s and even more in the future. PON technology reduces system cost by sharing fiber between multiple customers, but challenges transceiver designers by requiring burst-mode operation of amplifiers and clock recovery with low latency at gigabit data rates. We expect continuing innovation in this area for the foreseeable future.

Up to 40Gb/s data rates are now readily available using power-efficient CMOS chips. This year, ISSCC 2009 presents a large selection of such designs for clock- and data-recovery (CDR), equalization in advanced CMOS nodes down to 65nm, many of which have an emphasis on power efficiency. Exploration of these developments fits well with the current concerns for energy consumption of the Internet, both nationally and globally.

In preparing for the next speed increase, several building blocks with operation speeds in the range of 100GHz will be presented at ISSCC 2009. VCOs, PLLs and frequency dividers in this speed range will be shown to be successfully implemented in advanced CMOS technologies with feature sizes from 32nm to 65nm.

The trend to replacement of analog building blocks by digital-signal processing is continuing. Several papers of this kind will be presented at ISSCC 2009, for example, “all digital frequency synthesizer” and “all digital phase generators/rotators”.



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ISSCC 2009
Session Overview
Press-Release Material

- Condition of Publications
- Session Overviews

CONDITIONS OF PUBLICATION

PREAMBLE

- **The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2009 in February in San Francisco.**

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FOOTNOTE

- **From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 56th appearance of ISSCC, on February 8th to 12th, in San Francisco.**

This and other related topics will be discussed at length at ISSCC 2009,
the foremost global forum for new developments in the integrated-circuit industry.
ISSCC, the International Solid-State Circuits Conference,
will be held on February 8-12, 2009, at the San Francisco Marriott Hotel.

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Imagers

Session Chair: *Jan Bosiers, DALSA Professional Imaging, Eindhoven, Netherlands*
Session Co-Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

The papers presented in this session introduce recent innovations in consumer, professional and scientific imagers. A trend toward further 2D and even 3D integration is clearly present, and key performance parameters such a noise, sensitivity and speed continue to improve.

The session starts with Paper 2.1 [MIT Lincoln Labs, Irvine Sensors, Forza Silicon] that presents a four-side-abuttable, back-illuminated, three-dimensionally integrated 1Mpixel CMOS image sensor for surveillance and astronomy. The first layer has photodiodes with 100% fill factor and is connected to a second layer consisting of SOI-CMOS pixel readout and selection circuitry. The next layers provide the digital system interface and serve as a mechanical support to the thinned imager. The butting gap is only 3 pixels (25μm) wide by design.

Paper 2.2 [EFPL Lausanne, TU Delft] introduces a radiation-tolerant CMOS image sensor for space applications. By careful design and layout, the SPAD-based photon counting functionality can resist high radiation doses of 1Mrad of gamma, 40krad of proton, and 1mGy of X-ray radiation.

A 4-channel, 20-to-300Mpixel/s analog front-end with very low noise for use in digital SLR cameras is presented in Paper 2.3 [Analog Devices]. By employing a nonlinear adaptive biasing technique a pixel frequency range from 5MHz to 75MHz per channel can be supported without compromising the 80dB dynamic range. Crosstalk is -85dB and channel mismatch is 0.01%.

Paper 2.4 [Toshiba] presents a 1/2.5-inch 8Mpixel CMOS image sensor with a staggered shared pixel architecture to suppress Gr/Gb sensitivity imbalance to 0.3%. An FD-boost operation enables both low dark random noise and large detection node capability.

Paper 2.5 [CSEM] introduces a system-on-chip combining a QVGA pixel array with a 32b DCP/MCU processor for vision applications. The sensor achieves a 132dB intra-scene dynamic range with logarithmic encoding.

A 3.3Mpixel CMOS image sensor with 2.2×2.2μm^2 pixels is presented in Paper 2.6 [Canon]. A column-signal-addition method that uses a PMOS column amplifier reduces random noise by 30% and doubles responsivity.

Paper 2.7 [Sanyo] introduces a charge-multiplication technique that is conventionally used in in CCD readout structures, to a CMOS image sensor for the first time. By impact ionization of the photo-generated electrons within each pixel, the sensor is made suitable for ultra high speed and low-light-level imaging.

Finally, Paper 2.8 [Aptina] introduces a VGA-format CMOS sensor with dual conversion gain that achieves a noise floor of less than one electron., A video processor for correcting optical warp and perspective adjustment for automotive applications is included in this imager.

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Session 3 Overview / High Performance Digital

Microprocessor Technologies

Chair: Sonia Leon, Sun Microsystems, Santa Clara, CA
Associate Chair: Fabio Campi, STMicroelectronics, Agrate Brianza, Italy

Despite Gordon Moore's own admonition that exponential transistor density scaling cannot go on forever, high-performance processor designers have continued to increase levels of chip integration, with resulting improvements in system performance. Growing core counts and cache sizes lead to faster systems but also result in numerous challenges. For one, off-chip communication becomes more of a performance bottleneck. Second, chip reliability, which is a requirement in the commercial market, becomes harder to achieve in the face of soft errors and manufacturing defects. Finally, efficient communication across such large chips at multi-GHz frequencies is becoming challenging. So, as process technology improvements have slowed, circuit innovations in these areas are more crucial to enabling processor designs to maximize performance through the concurrent optimization of process, circuits, and architecture tradeoffs. These innovations are evident in four papers, which show new processor designs, and system architectures, while the other four describe fundamental building blocks for next-generation digital systems, including secure cryptographic engines, clock/frequency switching, on-chip interconnect, and die-temperature monitoring.

The first two papers describe the next-generation multi-core processors implemented in a 9M 45nm high-   process. Paper 3.1 [Intel] marks another microprocessor milestone and introduces a 2.3B transistor Xeon processor including eight dual-threaded cores, four power domains, and increased reliability from double-error correction and triple-error detection in its caches. Paper 3.2 [Intel] expands the discussion to cover the entire processor family, which supports from 2 to 24MB shared L3 cache and I/O links providing 6.4 GT/s. Particular emphasis is placed on power management techniques including an on-chip power microcontroller and power gate transistors allowing power dissipation from sub-10W to 130W in different mobile, desktop and server segments.

Paper 3.3 [NEC] examines system trade-offs enabled by separating on-chip memory onto a second layer flip-chip bonded atop a base logic chip. This system-in-package uses high-bandwidth 10µm-pitch micro-solder interconnect to exploit the benefits of increased memory re-configurability for mobile applications. This solution enable high-throughput inter-chip communication in systems-in-package, relieving the area pressure induced by ever-enlarging on-chip memory sizes as well as enabling innovative mixed-technology solution where memory is built in different process flavors than the computing logic.

Paper 3.4 [Intel] presents the dynamic frequency switching system for clocking an Itanium processor. It switches between a pair of core PLLs with a single-cycle penalty and briefly throttles the cores to mitigate di/dt noise during switching. This ability allows the processor to deterministically follow dynamic workload and environmental conditions without performance penalty and to more tightly optimize and manage power dissipation.

Paper 3.5 [U Michigan] describes an area and power-efficient method to protect against differential power attacks on cryptographic systems and implements an AES engine using this technique. Using switched capacitors to enable a multiphase precharge-evaluate-discharge scheme isolates the computation from external observation.

Paper 3.6 [MIT] employs a number of traditional off-chip communication signaling techniques to drive increasingly resistive 10mm on-chip wires. Using a 3-tap FIR transmit filter in conjunction with a receive-side transimpedance amplifier provides 4Gb/s at 0.3pJ/bit, providing an innovative solution to area, power and bandwidth challenges imposed by increasingly critical long on-chip communication channels.

Simple, reliable but non-invasive temperature sensing represents a critical need for today's high-performance microprocessors and digital circuits. Paper 3.7 [Harvard, Cavium] describes an all-digital closed-loop temperature sensor suitable for monitoring die temperature. Tuning the frequency of a temperature-sensitive DLL to equal that of a locked DLL provides the chip temperature with ±2 degrees accuracy with 5kS/s over a range of 0 to 100ºC.

Paper 3.8 [Intel] addresses power consumption and I/O latency constraints of high-end microprocessors. It describes a 6-core x86 processor that employs low-leakage techniques to reduce standby current with sleep transistors covering both SRAM and peripheral circuits. It also optimizes the layout placement of off-chip I/Os towards the center of the chip to enable a 1.066GT/s front-side bus and reduce I/O latency.

These papers introduce new records in transistor integration, tradeoffs between physical and architectural designs, and flexibility from reconfigurable architectures. They also cover enabling techniques such as efficient high-bandwidth on-chip interconnect, secure cryptographic circuits, and fully-digital temperature sensing that indicate that Moore's law still has at least a few years left.

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High-Speed Data Converters

Chair: *Boris Murmann, Stanford University, Stanford, CA*
Associate Chair: *Dieter Draxelmayr, Infineon Technologies, Villach, Austria*

As the bandwidth requirements of modern communication systems continue to grow, data converters are being pushed toward the limits of integrated circuit technology. The converters presented in this session aim to leverage the advantageous properties of fine-line CMOS technology to increase their throughput, classically measured via Shannon's bound in terms of signal bandwidth and signal-to-noise (and distortion) ratio.

Driven by the stringent requirements of 10G BASE-T communications, the circuit presented in Paper 4.1 [Broadcom] demonstrates a new record performance point for CMOS current-steering DACs. This design was realized in 65nm technology and achieves 60dB linearity for input frequencies beyond 1GHz. Similarly, the converters described in Paper 4.3 [National Semiconductor] and Paper 4.7 [Analog Devices] push the speed-resolution product for ADCs. Both of these designs maintain high SNDR beyond Nyquist input frequencies, yielding aperture uncertainties of approximately 180fs and 65fs, respectively.

While advanced process technologies offer ever-faster transistors at high integration density, designers must cope with the challenges associated with low power supply voltages and generally poor analog behavior of standard transistors. This explains a continued trend toward digital calibration as well as analog circuit and architecture enhancement strategies, clearly visible throughout the contributions presented in this session (Papers 4.2, 4.3, 4.5 and 4.6).

The ADCs presented in Paper 4.2 [Intel] and Paper 4.5 [U Illinois Urbana-Champaign, Jilin U, TI, ITRI] leverage digital calibration techniques to realize power-efficient, high-speed time-interleaved arrays. In addition to offset and gain errors, these designs digitally correct radix errors in the underlying successive-approximation sub-converters. In the pipelined converter described in Paper 4.6 [UCLA], linear and nonlinear calibration is used to minimize the accuracy requirements in the architecture's residue amplifiers. Owing to these simplifications, the authors manage to achieve a conversion rate of 500MS/s, which is the highest speed published to date for a single-channel CMOS pipeline.

An example for the continuing quest toward architectural simplifications and modifications that best exploit the properties of a modern process is shown in Paper 4.4 [National Cheng-Kung U]. The binary search ADC uses architectural modifications that exploit the speed of modern transistors to reduce the number of decision elements. This idea enables significant savings in area and the 5b 800MS/s proof-of-concept implementation shows an excellent figure-of-merit in comparison to other low-resolution converters published to date.

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Potpourri: PLL, Optical, DSL

Chair: *Larry DeVito, Analog Devices, Wilmington, MA*
Associate Chair: *Miki Moyal, Intel, Haifa, Israel*

High-bandwidth communication applications call for some common enabling circuit building blocks. In particular, timing control and clock generation are critical functions of the transceivers that comprise chip-to-chip, board-to-board and system-wide data links.

Paper 5.1 [National Chiao Tung University] describes an all-digital frequency synthesizer capable of self-updating its digital loop filter to simultaneously provide a quick locking time as well as low jitter generation for its 10GHz clock output. Paper 5.2 [National Taiwan University, Industrial Technology Research Institute] shows a new circuit idea using subharmonic injection locking for radically lower jitter in a frequency multiplier PLL. Paper 5.3 [IBM T. J. Watson] shows a frequency-multiplier digital PLL which has wide tuning range and small die area, and also avoids the uncontrolled gain problem of a BB phase detector in an integer-N synthesizer resulting in lower jitter generation than the more common technique of fractional-N synthesizer. Paper 5.4 [HKUST] shows a simple and effective modification of an injection-locked divider which gives significantly larger locking range. Paper 5.5 [IBM T. J. Watson, IBM] shows an all-digital core building block of a CDR which creates a pair of quadrature signals with arbitrary phase relative to a single phase reference input.

Communication using light signals over optical fiber holds great promise. Speed increases over legacy long distance fibers cause enormous design challenges in equalization in both transmitter and receiver designs. In the remaining papers of this session, several advances in the practical art of sending and receiving optical signals are presented. Inevitably, in the access area, such advances will lead to exciting data rate of 10Gb/s.

Paper 5.6 [Arizona State University] demonstrates a disarmingly simple modification to a well-known circuit architecture which allows the design to be much more tolerant to the speed-limiting effects of photodiode capacitance. Paper 5.7 [Ewha Womans University] shows effective solutions to two common problems in optical links: pulse-width distortion in VCSEL drivers and gain variation in a receiver TIA. Paper 5.8 [NTT] builds on previous work to improve data recovery in burst mode optical networks providing both high speed and robustness. Paper 5.9 [Advantest] uses an idea borrowed from dispersion-impaired copper transmission lines to improve the performance of multimode optical fiber which also is plagued by dispersion.

Often in real-world situations optical fiber is not an option. There is an enormous installed base of plain old copper telephone wires. Paper 5.10 [Marvell, University of Pavia] describes a VDSL2 interface for customer premises which delivers an astonishing 200Mb/s data rate over 100 meters of legacy telephone wire.

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CELLULAR and TUNER

Chair: *George Chien, MediaTek, San Jose, CA*
Associate Chair: *Aarno Pärssinen, Nokia, Helsinki, Finland*

Low cost: that's one story in the cellular industry. With volumes well over 1B units/year and increasingly matured markets, volume growth will come in the developing world, which requires low cost. The other story in the cellular industry is the attempt to increase silicon value by increasing functionality. Adding 3G, GPS and mobile TV, to name a few examples, will encourage end users to upgrade to high-end phones.

Paper 6.1 [Skyworks] is an example of the effort to drive down cost in 2/2.5G cellular phones. With the digRFv2 interface, all analog/mixed-signal content is removed from the baseband IC, enabling full-speed Moore's-law scaling and increasing integration of multimedia digital functionality. Cost reduction at the other end of the transceiver is enabled by a closed-loop polar modulator that improves power efficiency enabling more talk time and eliminates SAW filters.

Papers 6.2 [ST-NXP Wireless, Ericsson], 6.3 [Skyworks, Spectra-Linear] and 6.4 [Qualcomm] all describe WEDGE (that is, WCDMA and GSM/EDGE multimode) transceivers. 2/2.5G and 3G radios are remarkably different: wideband versus narrowband, full-duplex versus half-duplex, continuous versus bursty. Combining radios with such drastically different requirements creates some very interesting challenges.

Paper 6.2 [ST-NXP Wireless, Ericsson] employs a mature and extremely inexpensive 0.25µm BiCMOS technology combined with aggressive packaging to make a very small RF system-in-package that includes all passive components. The only component needed externally is the crystal resonator. High receiver dynamic range enables the elimination of RX-band SAW filters in the 3G bands.

A WEDGE transceiver integrating the digRFv3 interface is presented in paper 6.3 [Skyworks, Spectra-Linear]. High TX SNR and RX dynamic range enable the elimination of up to 10 SAW filters in the 3G bands. The diversity receiver enables high-speed download in HSDPA applications.

A third WEDGE transceiver is presented in paper 6.4 [Qualcomm]. In addition to multi-band 2/2.5G and diversity 3G receivers, the transceiver supports GPS and has the largest number of receiver inputs.

Paper 6.5 [NXP] pushes the technology envelope with the only 45nm effort in the session. Using a local oscillator with 25% duty cycle the transmitter achieves a -159dBc/Hz noise floor while enables the elimination of TX SAW filters. The IC consumes just 22mW while producing 1dBm output power.

The session concludes with 2 tuner papers. Paper 6.6 [Broadcom] is the first paper describing a dual-tuner for DOCSIS-3.0, an emerging cable-modem standard that pairs up to 6MHz cable channels and employs up to 256QAM modulation to support more than 300Mb/s downloads. The tuner can select channels between 48MHz and 1GHz and employs a low-IF topology with a harmonic-reject mixer to eliminate SAW filters. Paper 6.7 [MaxRise] describes a tuner for ISDB-T a Japanese mobile TV standard. At 67mW and $4mm^2$ in 0.13µm, the tuner pushes the state-of-the-art in power dissipation and cost.

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DRAM

Chair: *Kazuhiko Kajigaya, Elpida Memory, Sagamihara, Japan*
Associate Chair: *Heinz Hoenigschmid, Qimonda, Neubiberg, Germany*

Although the worldwide economy suffered a financial slowdown in 2008, the performance of DRAM, its bit capacity, its power per chip, and its speed all improved while applications of DRAM further diversified. The capacity of DRAM chips reached 4Gb by using the most advanced 56nm CMOS DRAM technology. In addition, the DRAM density per chip is increased to 8Gb by stacking 4 DRAM dies through via-connections within one package: another density record in DRAMs! A low power DRAM has a high-bandwidth DDR2 interface up to 1Gb/s but at a low-voltage supply of 1.35V, which is advantageous in mobile applications. The speed of a graphic DRAM exceeds 7Gb/s/pin, improving 3D graphic presentations on HD panels. Furthermore, several novel designs in PLL and signal-sensing circuit techniques also show continuing innovations in this field.

The efforts of increasing DRAM bit capacity per chip are demonstrated in the first two papers. At ISSCC, until the late 90's, DRAM papers showing higher density were always a highlight but the progress stalled for several years. Paper 7.1 [Samsung] features the first 4Gb DRAM operating at 1.2V, in contrast to current standard DDR3 DRAMs at 1.5V, which has been made with a $6F^2$ memory cell to pack so many bits in a small package size. A new hybrid I/O sense amplifier is demonstrated, which is critical to the performance of an open bitline array architecture. Standby and operating currents are reduced through both state-driven clock control and a pattern/location-sensitive address/data-bus-control circuitry. Paper 7.2 [Samsung] shows an 8Gb DRAM with the industry-standard DDR3 protocol by using a new 3D through-silicon-via (TSV) technology with the master DRAM die at bottom and the slave DRAM dice on top. The power noise is reduced to 100mV by deploying extra power pads and a TSV check-and-repair scheme.

The result of efforts to reduce DRAM power but keep a high data bandwidth is shown in Paper 7.3 [Hynix]. Mobile DRAMs used to be relatively slow, but this paper demonstrates a very-high-speed 4.3GB/s 1Gb LPDDR2 SDRAM that consumes only 112mW by using a special power-reduction scheme.

Paper 7.4 [Qimonda] sets a speed record with a leading-edge GDDR5 Graphic DRAM using high-speed circuit techniques. The record data rate of 7Gb/s/pin is achieved by using a multiple-power-domain system together with a boosted transmitter. Paper 7.5 [Qimonda] demonstrates reliable single-ended I/O circuit techniques. At a data rate of 5.33Gb/s/pin, a receiver input sensitivity of ±50mV is achieved while the transmitter improves ISI by 32%. An advanced high-speed signaling concept is proposed in Paper 7.6 [Samsung]. A pseudo-differential encoding scheme enables data rates of 6Gb/s/pin without using a reference signal.

In the DRAM field, innovations and smart design continue. Paper 7.7 [Hynix] describes a phase- and delay-locked loop manufactured in 54nm CMOS, having a DLL for phase compensation and a PLL for jitter reduction. This paper also shows a pseudo-rank architecture, suppressing V_{DD} noise due to low V_{PP} pumping efficiency. Finally, Paper 7.8 [Hitachi], presents a low-V_t gated preamplifier (LGA) with fast sensing and local-I/O-driving capability. A 70nm 128Mb DRAM core operates at an array voltage of 0.9V and achieves 16.4ns row access and 14.3ns read access, showing a future direction for sub-1V gigabit DRAM.

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Session 8 Overview / Low Power Digital

Multimedia Processors

Chair: *Fumio Arakawa, Hitachi, Tokyo, Japan*
Associate Chair: *Thomas Tomazin, MediaTek, Austin, TX*

Continued demand for advanced multimedia devices has precipitated much research in the area of multimedia processing. This demand is fueled by the prolific creation of new HD content and the requirement for this content to be available to the consumer anytime, anywhere. The high data throughput, multiple encoding standards, and low power requirements needed to deliver this content necessitates innovation, high levels of integration, and new algorithms to tackle these diametric requirements. New applications, such as recognition processing, 3D HDTV, and mobile HD further burden the already onerous load that multimedia processors must carry. From subthreshold circuit techniques to highly integrated deep-submicron SoCs, we see strong evidence of the advancement in the state-of-the-art in multimedia processors.

This session explores several recent advancements in multimedia processors, and offers innovative solutions to extreme low-power image processing, recognition processing, and mobile multimedia.

The session starts with paper 8.1 [NXP Semiconductor, TU Eindhoven, National U Singapore], which describes a multistandard 65nm CMOS JPEG encoding which delivers 15fps VGA image processing with only 200nJ/frame energy consumption at 0.4V.

The next two papers both show innovation in the area of machine object recognition: Paper 8.2 [Keio U] employs Haar-like feature and cascaded classifier techniques to perform detection and recognition of image and video. Paper 8.3 [KAIST] shows a 201.4GOPS real-time multi-object recognition processor using a bio-inspired neural perception engine.

An implementation of the now defacto Blu-ray Disc standard is presented in paper 8.4 [MediaTek]. The highly integrated SoC supports multiple protection, video and display formats.

Paper 8.5 [National Taiwan U] describes a 4096x2160p multiview video encoder chip for use in the emerging field of 3DTV applications.

The session concludes with two papers addressing multimedia processing in the mobile space. A very highly integrated single-chip application and baseband processor is presented in paper 8.6 [Panasonic]. All the latest low-power and integration techniques are employed to deliver HSDPA mobile standard, 3D graphics, WVGA image processing, and very-low-power audio processing. Finally, paper 8.7 [Renesas] has the first disclosure of a full-HD (1080p30) mobile application processor. The processor supports H.264/MPEG-2/MPEG-4 video codecs in a 65nm CMOS processor supporting 1080p30 real-time playback at only 342mW.

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Data Converter Techniques

Chair: *Bernhard Boser, University of California, Berkeley, CA*
Associate Chair: *Aaron Buchwald, Mobius Semiconductor, Irvine, CA*

Modern IC technologies with reduced intrinsic gain and voltage supplies present many challenges for achieving linear and well-controlled gain. This session highlights several diverse innovations and techniques that are inspired to circumvent these problems in the design of high-precision data converters.

Three pipeline converters introduce different approaches to reduce amplifier power dissipation. Paper 9.1 [UC San Diego] employs digital background calibration to correct linear and nonlinear errors using an on-chip DSP.

Papers 9.2 and 9.3 take a more drastic approach and eliminate the amplifier completely. In Paper 9.2 [U Toronto, Broadcom] passive voltage stacking replaces the error amplifiers used in conventional pipeline stages. Clock distribution dominates the power dissipation of the resulting circuit suggesting additional power scaling in future IC processes.

The converter described in Paper 9.3 [MIT] is based on the zero-crossing technique first presented at ISSCC 2006. The design consumes only 88fJ per conversion-step while operating at 50MS/s with 10 ENOB resolution. This performance is enabled with a new differential design that achieves good common-mode rejection without an explicit common-mode-feedback circuit.

Three papers perform quantization in time rather than amplitude. Paper 9.4 [U Michigan, National] compares the input to the ramp and exploits the low delays of a delay-line interpolator realized in 90nm CMOS to boost resolution. Unlike single-slope converters, this solution does not require a track-and-hold circuit.

Paper 9.5 [MIT, SiTime] relies on a VCO for amplitude-to-time conversion. Feedback reduces distortion from the VCO which doubles as a first-order noise shaper for a 4th-order continuous-time $\Delta\Sigma$ loop. The $\Delta\Sigma$ converter described in Paper 9.7 [Texas A&M, Qualcomm] employs a 3rd-order noise-shaping filter followed by a pulse-width modulator and time-to-digital conversion with 80ps resolution.

Two more $\Delta\Sigma$ converters rely on amplitude quantization. Paper 9.6 [MediaTek] uses a low-latency DEM shuffler to reduce loop delay, hence giving the amplifier more time to settle. A multipath topology further reduces amplifier power dissipation, resulting in an FOM of 0.15pJ per conversion-step.

Paper 9.8 [IMEC, Vrije U Brussel, Ghent U] describes a configurable bandpass $\Delta\Sigma$ modulator. The conversion bandwidth is adjustable from 100kHz to 2MHz to meet the specifications of GSM, UMTS, and Bluetooth standards. To reduce power dissipation, the first stage in the cascade architecture operates at one quarter the speed of the rest of the system.

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Multi-Gb/s Serial Links and Building Blocks

Chair: *Hui Pan, Broadcom, Irvine, CA*
Associate Chair: *Daniel Friedman, IBM T. J. Watson, Yorktown Heights, NY*

Multi-Gb/s serial links are critical to driving advances in application environments ranging from high-performance computing and networking to consumer products. In virtually all these environments, system designers demand ever-increasing throughput over difficult channels, and that this throughput be delivered within strictly limited power and area budgets. These demands create a formidable set of challenges for serial-link design.

In both the backplane and consumer application interconnect context, frequency-dependent channel loss has made integrated equalizers a common element of serial-link design, resulting in the exploration of a wide variety of equalizer approaches. Increasing the effectiveness of clock-and-data-recovery (CDR) circuits, required for applications in which clock forwarding is impractical, is another theme driving serial-link technology advances. Looking ahead, the industry's ever-increasing appetite for bandwidth will drive further growth in serial link usage. Meeting this demand will require link designs in ever-finer line-width CMOS technologies as well as designs tailored to future high-density packaging technologies.

This session presents serial-link advances relevant to backplane and consumer applications, describing new approaches to equalizer design and to CDR circuits. Equalizer designs range from a high-performance adaptive design at 10.3Gb/s in 90nm CMOS to a 4-tap decision-feedback equalizer (DFE) realized in 32nm CMOS. Clock and data recovery circuit entries range from embedded clock designs for LCD drivers to a new wide-range reference-free design approach.

The session starts with Paper 10.1 [Intel], which describes a scalable 3.6mW-to-5.2mW 5Gb/s-to-10Gb/s 4-tap DFE that is implemented in a 32nm CMOS technology. It results in a highly compact design that is the first to be realized and evaluated in this technology node.

Paper 10.2 [IBM T. J. Watson, MIT] explores the design of DFEs suited to signaling at rates approaching 10Gb/s in the context of future ultra-dense packaging technologies such as silicon carrier. This equalizer is also demonstrated to be effective for 10Gb/s signaling over typical backplane channels.

Paper 10.3 [Pohang University] presents a 650Mb/s-to-8Gb/s CDR that does not require a reference and performs automatic acquisition of data rate. This design achieves an extremely wide lock range while occupying just $0.108mm^2$ and consuming just 88.6mW from 1.2V when operating at peak data rate.

A new approach to linking a linear phase detector to a digital CDR circuit for use in a 10Gb/s receiver is described in Paper 10.4 [Hitachi]. This linkage is enabled by a new track-and-hold phase detector which feeds a charge redistribution ADC to create a digital data stream that is processed by the CDR circuit.

Paper 10.5 [Fujitsu Laboratories] presents a transceiver macro featuring a hybrid adaptive linear equalizer and a 1-tap DFE to achieve equalization of channels with half-baud-rate loss of up to 35dB in a compact low-power design implemented in 90nm CMOS. The transmitter features 3-tap fixed pre-emphasis.

An HDMI receiver featuring an adjustable bandwidth CDR and a 2-stage analog equalizer is presented in Paper 10.6 [MediaTek]. The digital phase interpolator-based CDR in this design automatically controls its CDR loop bandwidth by changing deserializer width as the incoming data rate changes.

Finally, Paper 10.7 [NEC, NEC Electronics] describes a clock-embedded interface for full-HD 10b 120Hz LCD drivers developed by NEC. This design features a novel CDR architecture that achieves significant power reduction yet allows robust operation in the high-noise environment in which the interface must operate.

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TD: Trends in Wireless Communications

Chair: *Hoi-Jun Yoo, KAIST, Daejeon, Korea*
Associate Chair: *Siva Narendra, Tyfone, Portland, OR*

Wireless communications has made this world more productive by not only enabling untethered communication systems, but untethered control and computation systems as well. In this session, several technology and application trends that have potential to significantly change the way we will control, communicate and compute in the future are demonstrated.

Paper 11.1 [CEA-LETI-Minatec, CEA-Spintec, Hitachi and STMicroelectronics] presents a spintronic-based oscillator that operates from 4GHz to 10GHz. In this paper the authors present a broadband spintronic oscillation system integrated with a CMOS amplification system that has potential to reduce system cost and power leading to more energy efficient multi-band wireless systems.

Papers 11.2 and 11.3 present novel uses of UWB based radio systems. In 11.2 [Royal Institute of Technology, KU Leuven] the authors present a 10Mb/s 14μW RFID with 14m operating range based on UWB uplink and UHF downlink in 0.18μm CMOS. With such a high data-rate, long-range, low-power, remote-powered RFID system several novel applications including precise position. Paper 11.3 [MIT and U Arizona] describes for the first time a wireless system that controls the motion of a moth. The system consumes 3mW and demonstrates the potential for extending motion control to flight control in the foreseeable future.

In Paper 11.4 [U Florida, TI, NXP] researchers discuss the possibility of applying CMOS technology to THz applications (300GHz to 3THz) through demonstration of Schottky diodes with a cut-off frequency of 2THz and several key blocks including oscillator, modulated signal generator and diode detector with on-chip patch antenna, all operating between 100GHz and 400GHz.

Researchers in Paper 11.5 [Philips] develop a wideband digital signal to human body coupling interface with a high input impedance receiver. It uses a frequency band from 1MHz to 30MHz and receiver correlation for synchronization and signal detection thereby providing a data rate of 8.5Mb/s at 2.75mW power consumption.

Papers 11.6 and 11.7 present two organic RFID transponder systems. In 11.6 [IMEC, KHLim, Polymer Vision, TNO Science and Industry, KU Leuven] a 128b organic RFID transponder is presented that is 2x faster than prior published results with higher levels of integration enabling WORM memory, a basic anti-collision protocol, and Manchester encoding. In 11.7 [PolyIC], researchers from Germany show for the first time CMOS organic transistors used to build an RFID system. Measurements show no degradation in the performance of the RFID transponder system after several months of operation.

Paper 11.8 [CSEM, EPFL] demonstrates for the first time a thermally-compensated silicon resonator to realize an accurate low-power real-time clock with better than 5ppm frequency accuracy consuming 3μA. In Paper 11.9 [U Washington] a 500μW fully-integrated wireless neural data transmission interface that can communicate over 15m is presented. By extending the wireless range that interfaces electronic systems to the neuronal system, one could envision processing and actuation of prosthetic devices.

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RF Building Blocks

Chair: *Hooman Darabi, Broadcom, Irvine, CA*
Associate Chair: *Nikolaus Klemmer, Ericsson Mobile Platforms, Raleigh, NC*

In the past few years, there has been a large interest in wideband reconfigurable receiver architectures and building blocks where several bands or applications can be simultaneously covered with optimum use of hardware. Several examples of software-defined radios (SDRs) have demonstrated such capabilities. Large out-of-band blocker suppression, low-noise and low-distortion capability, and wideband operation remain among the biggest issues. Particularly, low-noise amplifiers, down-conversion mixers, and frequency-generation circuits are among the most interesting RF building blocks that have evolved significantly to address such challenges. Lower power consumption, smaller size, higher integration and a smaller number of external components, along with wider bandwidth are the main driving factors for innovative architectures and circuits. The low cost and high level of integration available in CMOS makes it the most appropriate technology for such challenging designs.

This session explores the most recent advances in various radio receiver building blocks, including LNA's, mixers, and LO-generation circuits. It offers a broad set of solutions for several communications applications, both on architectural and block levels. On the system side, there are numerous opportunities for receiver architectures with higher immunity to large interferers to enable SDRs that inevitably lack a front-end filter. On the circuit side, RF building blocks with higher linearity and more tolerance to jammers are desirable.

The session starts with paper 12.1 [University of Pavia], which describes a broadband LNA for TV-Tuner applications. It focuses on off-chip passive-component removal by active suppression of even-order distortion generated in the amplifier itself and achieves outstanding dynamic range. An example of a broadband LNA combining positive and negative feedback to achieve high amplifier output SNR via noise cancellation is described in paper 12.2 [Georgia Tech, Samsung]. A 2dB noise figure is achieved while maintaining -3.2dBm IIP3 and achieving excellent power consumption of 3.6mW. Paper 12.3 [Caltech] demonstrates an alternative solution for a broadband LNA up to 10GHz. It is an extension of the conventional distributed amplifier where individual amplifier gain stages are selectively weighted to reduce amplifier noise. Layout considerations lead to the inclusion of inductor coupling coefficients as additional degrees of freedom to minimize area.

Paper 12.4 [U Twente] presents a high-linearity broadband frequency downconverter, highlighting the advantages of 4-phase, passive RF signal-current commutation for conversion efficiency and dynamic range. Without the use of an LNA, the mixer achieves competitive noise performance and outstanding linearity performance. Paper 12.5 [Toshiba] describes a current re-use double-balanced 4-quadrant multiplier employed as a very low-voltage low-power down-conversion mixer. Together with a passive cyclic RF+LO combiner, the circuit achieves an outstanding FOM of 20.8dB for mixers of any kind.

Paper 12.6 [Intel, Milan Poly] describes a rational frequency divider to prevent local-oscillator pulling in transceivers. Divider output spurs are suppressed by more than 30dB using a number of calibration loops addressing divider phase switching, buffer slew rate, and delay mismatch via a stochastic TDC. A low-power baseband section for a fast-hopping frequency synthesizer for wireless networks is described in paper 12.7 [Eindhoven University of Technology, Broadcom, Holst Centre]. The paper shows the clever use of single-sideband, harmonic-reject mixing, integer frequency division, and programmable RC-filtering that can be used to generate low distortion synthesizer output with 350μW power consumption.

Finally, the last two papers show examples of broadband highly linear receiver architecture techniques. Paper 12.8 [U Twente] presents a receiver architecture for broadband software-defined radio applications. It uses cascaded single-sideband harmonic-reject mixers to achieve high robustness against reciprocal mixing due to LO harmonics. High levels of dynamic range and harmonic suppression are achieved without the need for additional calibration or trimming. A variation of paper 12.8, showing the use of digital adaptive interference cancellation in conjunction with a single-stage harmonic-reject mixer is described in paper 12.9 by the same group. This allows a further dynamic-range and robustness improvement in this type of receiver.

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Flash Memory

Chair: Mark Bauer, Numonyx, Folsom, CA
Associate Chair: Dae-Seok Byeon, Samsung, Hwasung, Korea

Every year industry analysts predict that the bit growth of nonvolatile memory will slow down and fall off Moore's Law curve. Industry engineers and university researchers continue to prove the analysts wrong as we see in this session. The demand for high-density low-cost solid-state non-volatile memory continues to push the limits in lithography, multi-bit storage and low-power-memory subsystems. All six papers in this session report solutions to meet the demand for more non-volatile bits in emerging applications such as solid-state disks.

The most advanced lithography ever reported for a NAND flash memory uses MLC techniques to create a 32Gb device in a 34nm process. The highest density monolithic flash memory is also reported. Last year at ISSCC 2008, the conference saw for the first time a NAND flash design with 3 bits per cell. This year, a 64Gb NAND flash memory stores 16 levels in a cell for an unprecedented 4 bits per cell Two papers report on advancements in 3-bit-per-cell capability. One paper describes a 32Gb memory in a 48nm process and the other describes a 32Gb memory in a sub-35nm technology. In addition to advancements in density, two papers address power issues associated with building large memory sub-systems. One paper removes charge pumps from the memory device and uses an off-chip inductor with an integrated voltage regulator to reduce die area and increase power efficiency. The other paper presents an inductive-coupling technique for wireless interfaces between a stack of discrete flash devices.

The session starts with Paper 13.1 [Intel], demonstrating a 34nm 32Gb MLC NAND flash memory that uses a scaling-efficient array architecture with a mixed-string driver and a center-page buffer, resulting in 9MB/s program throughput. To minimize the routing impact, the datapath employs 4-way pipeline architecture and a pre-decoded redundancy-matching scheme. The analog architecture delivers precise and flexible voltages to optimize cell-disturbance mechanisms.

Paper 13.2 [U Tokyo, Toshiba] describes how the power consumption of 3D integrated SSD is reduced by using a boost-converter-based adaptive-voltage generator. By optimizing the frequency and duty cycle of a digitally controlled oscillator, power consumption, voltage rise-time and the voltage-generation time decreases by 88%, 73% and 85%, respectively. The total power consumption of a NAND flash memory system is reduced by 68%.

Paper 13.3 [Hynix] demonstrates 48nm 32Gb 8-level NAND flash memory that achieves a program throughput of 5.5 MB/s with a 4KB page depth. A pass-bit detector scheme is used in conjunction with a program algorithm to minimize program verify steps to improve write performance. With this innovation, program throughput improves by 30% as compared to the conventional case.

The first 32Gb NAND flash memory designed for a microSD card is presented in Paper 13.4 [Toshiba, Sandisk]. The extended column scheme reduces the chip size by 1% because the approach eliminates the redundancy circuit such as column address latches and their control circuits. The row decoder circuit is designed to reduce the pump load, resulting in the reduced pump area.

Paper 13.5 [Keio U, U Tokyo] presents an inductively coupled programmable bus using 0.18µm CMOS process for reduction of power consumption in SSD. The wireless interface using relayed transmission decreases the power consumption by 50%. This can be extended to interface many NAND Flash chips in parallel making the savings significant. In addition, I/O circuit layout area reduces to 1/40th of the conventional wire bond approach and helps achieve a data rate of 2Gb/s.

Paper 13.6 [Sandisk, Toshiba] demonstrates a 64Gb 4-bit NAND flash memory with 43nm CMOS process which achieves a remarkable program throughput of 5.6MB/s. The three-step program method is applied to improve the program performance by suppressing a cell coupling effect. Moreover, a sequential sense concept reduces program verify and read time which is an important factor of program performance.

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Digital Wireless and Reconfigurability

Chair: *Kees van Berkel, ST-NXP Wireless, Eindhoven, Netherlands*
Associate Chair: *Pascal Urard, STMicroelectronics, Crolles, France*

In the world of wireless communication, the quest for higher bit-rates, lower energy per bit, and lower integration costs is progressing relentlessly. In addition, we see more and more application of wireless links to ranging and telemetry.

This quest builds on rethinking architectures to achieve low power and low costs, by moving functions from the analog domain to the digital domain or vice versa, and by integrating all functions, RF and baseband, analog and digital, on a single die. Furthermore, high bit-rates are achieved by applying multiple antennas and algorithmic innovations. Finally, the ever increasing signal processing loads at minimal power budgets require pushing the limits of parallelism and reconfigurability at low supply voltages. The session Digital Wireless and Reconfigurability has it all.

Paper 14.1 [KU Leuven] describes a single-chip solution for IR-UWB, the Impulse Radio flavor of UWB. By implementing the pulse recovery in the analog domain they achieve an impressive 110pJ/pulse. With 660nJ a wireless ranging operation at 4.5m distance with sub-cm accuracy is demonstrated.

Paper 14.2 [MIT] is a IR-UWB baseband solution that emphasizes the reduction of the synchronization accuracy to as little as ±1ns, allowing them to reduce the synchronization time by one order of magnitude to 31.2ns. At 0.55V the chip draws only 1.6mW.

GPS is the best-known application of wireless ranging technology. Paper 14.3 [MediaTek] describes a fully integrated SoC consuming only 34mW during tracking and 45mW during acquisition, with a superior sensitivity of -165dBm to enable in-door usage.

MIMO is a key technology to achieve higher bit rates for standards like WiMAX and LTE. Paper 14.4 [U Toronto] describes a 4x4 MIMO Detector that applies a smart tree-traversal algorithm, achieving a 655Mb/s throughput at 126mW dissipation.

Paper 14.5 [STMicroelectronics] describes a solution for channel multiplexing of multiple satellite channels onto a single cable to dozens of set-top boxes. By moving the RF channel selection to the digital domain power is reduced to as little as 1W by addressing some interesting challenges: 1GS/s ADCs, 1GS/s DACs, and 1GS/s (I)FFTs.

Extremely low power consumption for programmable accelerators is the goal of Paper 14.6 [Intel]. By applying SIMD, novel reconfigurable datapath circuits, dual supply-voltage hopping, and fine-grained power management they achieved an impressive operation range from 230mV to 1.3V and a power efficiency up to 494GOPS/W.

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Display and Imager Electronics

Session Chair: *Iliana Fujimori-Chen, Analog Devices, Wilmington, MA*
Session Co-Chair: *Oh-Kyong Kwon, Hanyang University, Seoul, Korea*

TFT-LCD remains the dominant technology for large-format and mobile displays. High image quality and low cost are the main factors pushing the limits of the driving electronics. The former requires an increase in the number of gray levels, faster settling time and precise channel-to-channel and chip-to-chip matching. The latter, namely cost reduction, is accomplished by area shrinkage.

Active-matrix OLED (AMOLED) is an emerging technology that promises better image quality, lower power and lower manufacturing cost. Currently, AMOLED displays suffer from random variations in V_t, requiring compensation techniques within the pixel. Digital driving techniques can mitigate image degradation caused by V_t-shifts with two-transistor pixels, but conventional pulse-width-modulation digital driving techniques lead to false-contour noise.

Paper 15.1 [KAIST, Samsung] describes a method to achieve higher performance at lower cost: a piecewise-linear 10b DAC for an active-matrix LCD (AMLCD) that has higher effective bit resolution than a linear 10b switched-capacitor DAC and lower area than a conventional 8b resistor DAC.

Paper 15.2 [Purdue U, KAIST, Samsung] offers improvements similar to those described in the previous paper, namely higher performance at lower cost. In this case, a 10b DAC for a mobile AMLCD combines a 6b resistor DAC with a 4b interpolation amplifier to improve accuracy and area efficiency.

Paper 15.3 [Brookman Lab, Shizuoka U] describes a CMOS image sensor with column-parallel single-ended 13b cyclic ADCs. The sensor achieves a vertical fixed-pattern noise of $0.1e^-_{rms}$, a dynamic range of 71dB, and a read noise of $4.7e^-_{rms}$. The ADCs are implemented in a 5.6μm pitch and perform two conversions in 6.83μs.

Paper 15.4 [Purdue U, LG Electronics] describes a digital drive method for AMOLED displays based on pulse-density modulation (PDM). The digital drive allows a small simple pixel circuit and minimizes pixel-to-pixel variability arising from manufacturing variations in V_t, while the PDM eliminates the false contour issue associated with a PWM drive, resulting in improved image quality.

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High-Speed and mm-Wave Circuits

Chair: *K. R. (Kumar) Lakshmikumar, Conexant Systems, Red Bank, NJ*
Associate Chair: *Jae-Yoon Sim, Pohang University of Science and Technology, Pohang, Korea*

Very-high-speed wireline and wireless communication systems offer many opportunities and challenges. There are two different approaches to realize such systems. The first one is to employ modulation techniques that make more efficient use of the limited available bandwidth. The other approach is to take advantage of the advancements in CMOS technology to build ever faster circuit functions like equalization, clock and data recovery (CDR), etc. The papers in this session give a flavor of both of these approaches covering emerging applications such as 100G Ethernet, mm-wave wireless 100GHz-range sensing and imaging, and anti-collision radar systems.

As the data rate exceeds 10Gb/s, the limited bandwidth of the channel poses severe challenges for the design of systems with NRZ data. Multilevel signaling can reduce the bandwidth requirement. Duobinary modulation uses 3 levels and requires only 75% of the bandwidth of NRZ spectrum. Paper 16.1 [NEC] describes a 90nm CMOS duobinary receiver operating at a data rate of 18Gb/s with power consumption of 100.2mW from 1.2V supply.

Paper 16.2 [National Taiwan University] demonstrates a PLL with the highest frequency reported to date, 96GHz. The PLL is implemented in 65nm CMOS and consumes 43.7mW from a 1.2V supply. The paper focuses on the design of VCO and prescalers which are the highest frequency subcircuits.

In order to provide wide range of oscillation frequencies in 100GHz band, an array of four switchable LC-VCOs, implemented in 32nm SOI CMOS, is demonstrated in Paper 16.3 [IBM, Qualcomm, IBM T. J. Watson]. The VCOs cover the frequency bands ranging from 83.2 to 96.7GHz and from 100.1 to 104.3GHz.

As a power-efficient solution to frequency division at high frequencies, injection-locking technique is gaining popularity. Two injection-locked frequency dividers (ILFDs) are presented in next two papers: Paper 16.4 [National Taiwan University, Faraday Technology, Chip Implementation Center] presents an ILFD that is implemented in 0.13mm CMOS and operates at 38 and 57GHz with a dual-mode feature of divide-by-2 and divide-by-3. Finally, Paper 16.5 [National Taiwan University] demonstrates a 65nm CMOS distributed LC circuit operating at 128.24 to 137GHz consuming 5.5mW from a 1.1V supply.

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TD: Energy-Aware Sensor Systems

Chair: *Alison Burdett, Toumaz Technology, Abingdon, United Kingdom*
Associate Chair: *Shuichi Tahara, NEC, Tsukuba, Japan*

The development of miniature wireless sensors capable of operating autonomously on very limited energy supplies enables a wealth of new applications in areas ranging from environmental and habitat monitoring to healthcare and personal safety. These energy-aware sensor systems are required to implement fairly sophisticated signal processing and control functionality at average power levels which permit operation from very small batteries or even by harvesting ambient energy.

This session introduces a range of techniques which strive to improve or enhance the energy efficiency of autonomous sensor systems, either by reductions in system power consumption or by the development of improved energy storage, transfer and conversion methodologies.

The first three papers in the session focus on system-level implementations of particular energy-aware sensor applications.

The session opens with Paper 17.1 [Infineon Technologies], which describes a complete system for tire pressure monitoring, incorporating bulk acoustic wave (BAW) resonators to achieve a compact and power-efficient 2.11GHz FSK transceiver.

Paper 17.2 [National Taiwan U] demonstrates a release-on-demand drug delivery SoC for implantable applications. Eight addressable 100nL reservoirs are integrated by CMOS-compatible post-IC processing, whose contents can be released by rupture of the membranes by electro-thermal heating on receiving the appropriate wireless commands.

A self-configuring system for continuous health monitoring is presented in Paper 17.3 [KAIST]. A 12μW sensor chip incorporates an ECG AFE, 120kb/s data rate transceiver and power harvesting adaptive threshold rectifier and occupies 4.8mm^2 in 0.18μm CMOS. The companion network controller chip locates the sensor positions and wirelessly provides power and data to selected sensor nodes, while dissipating 5.2mW from a 1.8V supply.

The next five papers in the session focus on energy delivery methods. Paper 17.4 [U Freiburg and Micronas] demonstrates a stabilized power supply realized by monolithically integrating micro fuel cells within an extended CMOS process, delivering a maximum output power of 450μW/cm^2. The associated control circuitry including an LDO and programmable timing network consumes an average power of 435nW to achieve a system efficiency of up to 89% at a constant 3.3V output voltage.

Paper 17.5 [Stanford U and U Illinois at Urbana-Champaign] presents a highly efficient wireless power delivery system for implanted medical devices. By employing simultaneous conjugate matching, the receiving antenna area is reduced to 4mm^2, which is a reduction of 100x compared to previous designs. A high-efficiency rectifier and regulator are integrated in 0.13μm CMOS and deliver 140μW at 1.2V DC from a 0.25W 915MHz source and 4cm^2 transmit antenna through 15mm of tissue.

Energy harvesting from piezoelectric sources is the focus of Paper 17.6 [MIT]. Power extraction improvement of 4.2× over conventional full-bridge rectifiers is achieved by a bias-flip rectifier, which efficiently shares the required inductor with switching DC-DC converters to reduce the overall system component count.

Paper 17.7 [UC Davis and Agilent Technologies] is also concerned with efficient energy harvesting, and presents a power management IC which can take inputs from multiple energy sources. An energy-aware switched capacitor AC/DC converter and a flexible charge recycling DC/DC converter are fabricated in 0.25μm CMOS and achieve efficiencies of 84% and 74%, respectively.

Paper 17.8 [IMEC, KU Leuven, RMA] demonstrates an efficient and compact power management circuit for thermal harvesters, particularly aimed at body-worn wireless sensor nodes. For this application the thermal harvester output can vary from 10 to 1000μW, and the power management circuit automatically adapts the number of stages and the switching frequency to achieve optimal performance depending on the input power level. This new control algorithm leads to a system efficiency of up to 70%.

The final paper in this session is Paper 17.9 [U Barcelona], which implements an SoC for managing the functionality of a microbot in ultra-low-leakage 0.13μm CMOS. The SoC integrates an 8051 microprocessor with sensor and actuator interfaces, communication and control circuitry and timers, and exploits the event-driven nature of the robot tasks to maintain power consumption below 1.5mW.

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Ranging and Gb/s Communication

Chair: *Didier Belot, STMicroelectronics, Crolles, France*
Associate Chair: *Yorgos Palaskas, Intel, Hillsboro, OR*

Silicon IC implementations for ranging applications such as radar in the 24GHz and 77GHz millimeter-wave frequency bands have recently appeared . These low-cost silicon BiCMOS or even CMOS-only solutions will eventually enable the penetration of ranging applications in the consumer and automotive markets. Anti-collision radar is clearly one of the more likely applications in this field.

The first part of this session explores the most recent developments in ranging applications in silicon.

Papers 18.1, 18.2, and 18.3 all focus on automotive radars. Paper 18.1 [U Catania, STMicroelectronics] describes an analog correlation receiver operating in the 24GHz band and implemented in SiGe BiCMOS. The short-range radar transmits UWB pulses of 300ps, corresponding to 5cm ranging resolution. A dual-band transceiver that can operate at both 24GHz and 77GHz for current and upcoming automotive radar specifications is presented in paper 18.2 [UC Irvine]. Fabricated in a BiCMOS technology, the transceiver chip achieves an output power of more than 10dBm while consuming 615mW. A 77GHz transceiver targeted for continuous- time frequency-ramp modulation radar implemented in 90nm CMOS is presented in paper 18.3 [Fujitsu Laboratories]. The chip consumes 920mW at output power of 6.3dBm.

The transceiver presented in paper 18.4 [CEA-LETI-Minatec] achieves ranging with 30cm accuracy and data communication up to 31Mb/s. In contrast to the previous papers, the 4-to-5GHz UWB frequency band is used here. The non-coherent impulse radio is highly digitized, consumes only 45mW and is implemented in 0.13µm CMOS.

The second part of the session focuses on very-high-data-rate Gb/s communications. Such systems can be used in a variety of applications such as high-definition video wireless transfer and fast download of large files over short-range distances. The 60GHz UWB ISM band seems suitable to achieve data rates in the order of 1-to-5Gb/s. Here CMOS technology is the key to low-cost and widespread adoption of the new communications systems.

Paper 18.5 [UC Berkeley] shows a fully integrated low-power 60GHz transceiver including baseband circuitry implemented in 90nm CMOS. The paper demonstrates 4Gb/s QPSK communications over a 1 meter wireless link. The chip consumes 170mW in transmit mode and 138mW while receiving.

Paper 18.6 [National Taiwan University] uses OOK modulation to achieve 2.5Gb/s over a distance of 4cm. The transceiver has been realized in 90nm CMOS and has a low-loss dipole antenna attached. The transmitter consumes 183mW and the receiver 103mW.

The session ends with paper 18.7 [NEC] showing that high data rates can also be achieved at lower frequencies. The digital hopping UWB transceiver operates at 7GHz to achieve a 2.88Gb/s data rate. The traditionally-used LO frequency-hopping scheme is replaced by a frequency-hopping polyphase filter. Fabricated in 90nm CMOS, the receiver consumes 156mW.

This session contributes to increasing the know-how of emerging applications in ranging and Gb/s wireless communications, in order to provide state-of-the-art design solutions for future low-cost silicon-based products in the consumer and automotive markets.

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Analog Techniques

Chair: *Doug Smith, SMSC, Austin, TX*
Associate Chair: *Yoshihisa Fujimoto, SHARP, Nara, Japan*

A wide variety of modern analog circuit design is in full view in Session 19. Circuits in advanced semiconductor processes, such as those that include FinFETs, require a rethinking of existing analog techniques. The sophistication of chopper-stabilized instrumentation amplifiers continues to take great strides forward. Useful circuits with pW power consumption are now in the analog designers repertoire. Unique new filter topologies deliver improvements in key parameters and predict future increases in filter figure of merit.

This session starts with two papers in the area of chopper-stabilized instrumentation amplifiers. Paper 19.1 [TU Delft] demonstrates an amplifier with a 1/f corner of 1mHz using a unique narrowband filtering technique for ripple reduction. The output ripple is AC coupled into a demodulator generating a signal which is proportional to the ripple amplitude. Paper 19.2 [National Semiconductor] also describes an amplifier, but in this circuit a ping-pong input, chopper stabilization, and autozeroing techniques are all combined in the input stage to reduce 1/f noise and input offset. The amplifier achieves a CMRR of 140dB.

Paper 19.3 [University of Michigan] describes an extremely-low-power oscillator that is implemented in 0.13µm CMOS and is intended for sensor applications. The oscillator receives its power from a charge holding technique reminiscent to current copier circuits and achieves a power consumption of 150pW.

Paper 19.4 [TU Vienna] describes an improved 65nm CMOS comparator with lower delay than previously reprted comparators at supply voltages under 1V. This is achieved by cleverly separating the feedback paths in a conventional latch. At 0.6V, the sensitivity is 90.2mV at a frequency of 700MHz.

Paper 19.5 [Texas A&M University] demonstrates an LDO in 0.13µm CMOS with –56dB PSRR at 10MHz using a unique summation technique which reduces the effect of input ripple on the output voltage.

A sub-1V 32nm SOI FinFET bandgap is demonstrated in Paper 19.6 [University of Twente, NXP]. This design is interesting both because of the use of a lubistor as the bandgap diode element as well as a unique way the PTAT and CTAT voltages are combined via matched OTAs.

The final two papers are in the area of continuous-time filters. Paper 19.7 [Toshiba] presents an interesting tuning scheme for an active-RC filter utilizing a $\Delta\Sigma$ modulator which controls the duty cycle of a CMOS resistor bypass switch that sets both the effective resistor value and spectrally shapes the resultant switching noise. The resulting filter is used in a Bluetooth channel-select bandpass filter which achieves a 6.3kHz step cutoff frequency control in 90nm CMOS. Paper 19.8 [University of Pavia] describes a 4th-order lowpass filter in 90nm CMOS. This circuit uses a novel in-band noise-reduction scheme in cross-connected cascade devices to achieve in-band noise below the kT/C level and a 75dB SFDR while consuming only 1.25mW of power.

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Session 20 Overview / IMMD

Sensors and MEMS

Chair: *Christoph Hagleitner, IBM, Rüschlikon, Switzerland*
Associate Chair: *Kofi Makinwa, Delft University of Technology, Delft, Netherlands*

Sensors and MEMS are becoming ubiquitous and essential building blocks inside the electronic gadgets and information systems that we use in our daily lives. The availability of small, reliable and inexpensive sensor systems is a key factor that will enable many of the future information technology systems that we envision today. The main challenges include miniaturization, system integration, cost and power consumption.

This session shows recent developments that advance the state of the art. Temperature sensors have become ubiquitous, and this session highlights two systems that set new standards with respect to accuracy and process technology. Two MEMS-based papers on a gyroscope and a microphone show the continuing trend to miniaturize, integrate more functionality and reduce cost at the system level. The session also includes two papers that show progress towards nano-biosensors, and concludes with two sensors for thermal imaging and range-finding applications.

The session starts with two temperature sensors. Paper 20.1 [Intel] shows that temperature sensors based on the bandgap principle can still be used at the 32nm technology node. The paper explains techniques that are used to realize a temperature sensor with sufficient accuracy for microprocessor thermal management applications. Paper 20.2 [TU Delft, FUSM, Holst Centre] presents a temperature sensor with 0.1ºC accuracy over the military temperature range from -55ºC to 125ºC, and can also operate over an extended range spanning 200ºC.

Paper 20.3 [Helsinki University, ELMOS] shows an interface circuit for a 2-axis accelerometer that explores circuit techniques to reduce area and therefore system cost without compromising performance.

The next two papers present readout circuits for nanosensors used in bio-applications. Paper 20.4 [Politecnico di Milano] shows a capacitive readout circuit with a resolution in the attoFarad range. Paper 20.5 [U Bologna, Silicon Biosystems, U Salento, U Milano-Bicocca] presents a system that uses a current readout technique to detect ion channel activity.

The MEMS microphone presented in Paper 20.6 [Pulse, Lund U, TU Denmark] uses a combination of two microphones and an innovative interface circuit to achieve significant improvements in SNR without redesigning the micromachined part of the system.

The last two papers in the session are devoted to special imaging applications. Paper 20.7 [U Vienna] presents a range-finding sensor system that can suppress ambient light up to 120kLx. Finally, Paper 20.8 [IMS CHIPS] presents a thermal imaging camera that uses a logarithmic CMOS imager and a subtraction technique to measure temperature independent of the emissivity.

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10-to-40Gb/s Transmitters and Receivers

Chair: *Naresh Shanbhag, University of Illinois, Urbana-Champaign, IL*
Associate Chair: *Takuji Yamamoto, Fujitsu Laboratories, Kawasaki, Japan*

High-density high-speed applications such as network switches, routers, and blade servers continue to drive the demand for ever-higher data rates and increased levels of integration. Similarly, on the optical side, enterprise, metro and long-haul links drive similar needs. The result is continued pressure on circuit designers to develop innovative multi-Gb/s CMOS transceivers and building blocks for such transceivers that operate at higher and higher rates and provide more performance per mW. This session highlights the advances made in implementing transmitter and receiver circuits in CMOS for the 10-to-40Gb/s range.

The first two papers present a 40Gb/s transceiver chipset and a transmitter in 65nm standard CMOS. Paper 21.1 [NEC] is a fully integrated transmitter and receiver packaged in a plastic BGA, covering a range of data rates from 39.8Gb/s to 44.6Gb/s based on SFI5.1. Power dissipation of each chip is 2.8W. Paper 21.2 [Fujitsu] is an SFI5.2-compliant serializer IC, which supports a single 40Gb/s output for OC-768 VSR and dual 20Gb/s outputs for DQPSK. The chip consumes 1.8W and 1.6W in the 40Gb/s and 20Gb/s modes, respectively.

The next two papers focus on building blocks needed to design 40Gb/s transceivers. Paper 21.3 [UC Irvine] presents a 40Gb/s full-rate 2:1 MUX in 0.18µm CMOS consuming 776mW of power. It uses a full-rate dynamic retimer to reduce deterministic jitter, and a push-push VCO topology to achieve a 40GHz oscillation frequency. Paper 21.4 [UC Irvine, Broadcom] discusses a 40Gb/s T/2-spaced 7-tap FFE implemented in 65nm CMOS. The equalizer employs active and passive delay elements to achieve high-speed operation. It consumes 80mW from a 1V supply.

Paper 21.5 [National Taiwan University] describes a 20Gb/s full-rate linear CDR with automatic frequency acquisition, the fastest full-rate linear CDR reported in CMOS. The CDR is based on a full-rate VCO and novel mixer-based linear phase detector. The design occupies an area of 0.97x0.88mm^2 in 90nm CMOS and consumes 154mW from a 1.5V supply.

Paper 21.6 [IBM T. J. Watson] presents a 5-tap DFE receiver that achieves 11.1Gb/s operation while consuming only 78mW. The 0.22mm^2 65nm CMOS receiver includes logic to calibrate the summer bias current to compensate for process variation and data rate. Its performance is demonstrated on a 30-inch PCB trace and a 16-inch Tyco backplane.

Finally, Paper 21.7 [Broadcom] provides a description of a DSP-based AFE for use in 10Gb/s backplane and multimode fiber applications. The transceiver consumes 500mW and occupies 3mm^2 in 65nm CMOS. The RX is based on a digitally calibrated 6b interleaved ADC that achieves 31.6dB SNDR and 39dB SFDR with a 5GHz input. The TX features a 3-tap FIR filter with only 2.9ps$_{pp}$ of ISI and the random output jitter is measured to be only 0.38ps$_{rms}$.

The papers in this session predict that CMOS will continue to find applications formerly served by BiCMOS process technologies. It is expected that transceivers for upcoming optical standards such as those at 100Gb/s will also be based on CMOS.

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Session 22 Overview / RF

PA and Antenna Interface

Chair: *Michael Zybura, RFMD, Scotts Valley, CA*
Associate Chair: *Hiroyuki Sakai, Panasonic, Osaka, Japan*

Silicon-based power generation continues to grow as an area of research and advanced-product development, to overcome unfavorable transistor speed-breakdown trade-off. This presents a worthy challenge for designers to leverage a large number of low-voltage transistors to produce high power levels at higher frequencies. The applications span a wide frequency range requiring some of the most demanding specifications of CMOS technology. These include current- and next-generation cellular front-ends, power amplification for mm-wave communications, radars, and RF imaging. In the cellular market, there is growing demand for efficient power generation for non-constant-envelope modulation schemes, while meeting exacting specifications, low cost and enduring harsh environments. Although the classical solution to this problem has been to use linear power amplifiers, alternative solutions involving new linearization techniques or direct power synthesis are gaining traction. In the mm-wave arena, the increasing bandwidth demands have made V-band a realistic option for gigabit wireless communications where ever-finer geometries are facilitating the inevitable march of CMOS chipset solutions. Silicon designs also keep pushing the envelope on the air interface using a broad set of exciting approaches that address many of the salient issues faced in these applications, including adaptable antenna matching and a tunable duplexer. Some of the most recent developments that continue to advance this front are presented.

Paper 22.1 [University of Southern California] describes a power amplifier for imaging applications with ultra-wide instantaneous bandwidth. The seven-stage PA design employs a unique topology to achieve a 0.75-to-3.75GHz 3dB bandwidth with 21dBm of saturated output power.

Paper 22.2 [Caltech, Toshiba] again challenges convention. Merging the transmit mixer and power amplifier, state-of-the-art cell-band efficiencies at watt-level powers are demonstrated across an octave of bandwidth in 0.13um CMOS. At 1.8GHz, 31.3dBm output power is achieved with 42% PAE. With 16QAM modulation, PAE is nearly 20% with an average output power of 25.8dBm and an EVM of 5.2%.

Paper 22.3 [UC Berkeley, Intel] describes continued progress on fully integrated CMOS PA's. A 90nm CMOS 2.4GHz linear amplifier produces a saturated power of 30dBm and 33% PAE. A novel bypass network provides stability and 28dB of gain. EVMs better than -25dB are demonstrated at 22.7dBm under OFDM-modulated signal drive

Two V-band mm-wave power amplifiers are presented next. Paper 22.4 [TU Delft, IBM] pushes the 60GHz state-of-the-art performance using a three-stage PA on the 65nm node. Producing 11.5dBm of saturated power with 15dB of gain, the inductively-coupled PA yields 11% PAE from a 1V supply. In paper 22.5 [KU Leuven, IMEC, Vrije Universiteit Brussel], the authors show a 45nm push-pull 60GHz amplifier with a P1dB of 8.4dBm and a saturated power of 13.8dBm.

Paper 22.6 [Arizona State University] presents a closed-loop adaptive antenna-impedance-tuning system. The mixed-signal approach replaces the need for an ADC and can scan more than 4000 antenna-matching states in 4.1msec. Return-loss improvement of >15dB is demonstrated.

Finally, a 40nm CMOS tunable integrated duplexer is shown in Paper 22.7 [Broadcom, UCLA]. More than 50dB of isolation is attained across nearly 1GHz with a hybrid-transformer-based design tuned for the WCDMA band.

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PLLs and Clocks

Chair: *Ivan Bietti , STMicroelectronics, Grenoble, France*
Associate Chair: *Changsik Yoo, Hanyang Univ. Seoul, Korea / Silicon Image, Sunnyvale, CA*

Circuits that generate local oscillator and clock signals are essential blocks in almost all modern electronic systems. The phase-locked loops (PLLs), delay-locked loops (DLLs), and oscillators that perform these tasks and their required performance specifications are extremely diverse, and the overall performance of the systems in which they are used often depends on their quality. In wireless transceivers, PLLs are used to generate high-frequency local oscillator signals with extremely low phase noise for upconversion and downconversion of the transmitted and received signals. In wireline transceivers low-jitter clock signals are required for high-speed data communication. In digital circuits, PLLs and DLLs are used to generate and properly align clock signals. In extremely low-power applications such as sensor network nodes and biomedical implant devices, relaxation oscillators with enhancements to ensure frequency stability are emerging as viable clock signal sources.

The relentless increases in speed and circuit density of CMOS technology and the resulting performance enhancements of communication and computation systems has fueled extensive and sustained research and development efforts in circuits for local oscillator and clock signal generation. The circuits are inherently analog in nature, but increasingly must be implemented in CMOS technology optimized for digital circuitry. Therefore, significant research effort has been devoted to the development of new techniques that enhance analog performance despite CMOS process limitations such as reduced voltage headroom and increased device leakage.

In this session, five of the papers are on PLLs. Paper 23.1 [Arizona State University, Intel] presents a wide-bandwidth fractional-N Type-I PLL with phase-noise cancellation. A new phase-and-frequency detector (PFD), charge pump, and sampled-loop-filter configuration is utilized to avoid practical difficulties associated with conventional Type-I PLLs and facilitate precise phase-noise cancellation. Paper 23.2 [University of Twente, National Semiconductor] presents an integer-N PLL with a new gain-controlled phase detector that directly samples the VCO. It eliminates the divider used in most conventional PLLs and achieves a high phase-detector gain, thereby, reducing power consumption and phase noise. Paper 23.3 [National Chip Implementation Center, National Central University] presents a PLL capable of rapid frequency hopping enabled by a new extended-range PFD and charge pump topology that reduces the number cycle slips during frequency transitions. Paper 23.4 [Ratio Microelectronics, Fudan University] presents a fractional-N PLL with a new automatic frequency-control block to maintain constant loop bandwidth over a wide tuning range and a half-integer fractional divider to reduce phase noise from the modulator. Paper 23.6 [National Taiwan University] presents an integer-N PLL with on-chip loop filter based on a thin-oxide MOS capacitor with adaptive leakage compensation.

The other three papers of this session address the challenges in clock generation and distribution in different application areas: Paper 23.5 [Tsinghua University, Samsung Electronics] presents a novel technique to finely tune the phase of the input clock with sub-ps resolution. This method can be of great interest for synchronous links, clock-recovery systems and for clock distribution. The 38μW 3.2MHz relaxation oscillator in Paper 23.7 [Institute of Microlectronics, Physical Logic] uses a self-clocked offset-cancelling comparator to achieve ±0.4% and ±0.25% frequency accuracy over supply and temperature.

Finally, Paper 23.8 [Matsushita Electric Industrial] demonstrates the use of power-averaging-feedback technique to overcome the sensitivity to variations in supply voltage and temperature. The 45μW 14MHz oscillator shows ±0.16% and ±0.19% frequency variation over supply and temperature, respectively.

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Wireless Connectivity

Chair: *Mototsugu Hamada, Toshiba, Kawasaki, Japan*
Associate Chair: *Mark Ingels, IMEC, Leuven, Belgium*

Wireless devices have been dramatically growing in the market over the past ten years and are now connecting person-to-person, person-to-devices and devices-to-devices for better quality of life everywhere. This trend requires each wireless device to be highly integrated, low-cost, high-performance and low-power. The reduction of external components leads to lower cost and smaller devices. At the same time, wideband multimode capability is desired to cope with emerging standards, while offering backward compatibility with existing infrastructure.

The papers in Session 24 present various ICs and circuit techniques that enable higher levels of wireless connectivity. WPAN(WiMedia), WLAN and WiMAX come together in this session. Depending on the communication distance and required bit-rate, these wireless standards complement each other to provide universal connectivity. In addition, future medical care will increasingly rely on wireless communication between various implantable and body-wearable sensors.

The session begins with a software-defined receiver in 45nm CMOS. Paper 24.1 [IMEC, KU Leuven] describes a front-end receiver operating from a 1.1V supply and covering a selectable band from 0.1 to 5GHz. The paper demonstrates the compatibility with many existing standards, such as mobile digital TV/radio, 2G/3G/4G cellular standards, WLAN and WPAN.

The next two papers demonstrate significant advancements in WiMedia design. Paper 24.2 [NXP, ST-NXP Wireless] describes an inductorless WiMedia SoC designed in 65nm CMOS. Elimination of inductors from high-frequency circuits is accomplished with the clever utilization of ring oscillators and inverter-like amplifiers. The RF and digital baseband occupy only 3.3 x 3.3 mm^2. Paper 24.3 [University of Modena and Reggio Emilia, University of Pavia] presents a new method to enlarge the frequency coverage in UWB design. A reconfigurable mixer that can switch between the fundamental mode and the sub-harmonic mode is utilized so that the tuning range requirement of the VCO is relaxed.

Papers 24.4 and 24.7 [both Analog Devices] address an IEEE 802.15.4 WPAN transceiver SoC operating at 2.4GHz. The first paper discusses the receiver while the latter presents the transmitter. The chip utilizes digital-assisted RF techniques to improve the power versus accuracy trade-off. At the receiver antenna diversity is provided, while the transmitter is based on a directly-modulated VCO.

Paper 24.5 [Marvell] presents the first integration of a 2x2 MIMO dual-band dual-mode direct-conversion transceiver for WiMAX/WLAN applications. The chip covers 2.3GHz to 2.7GHz and 3.3GHz to 3.9GHz while occupying only 12.4mm^2 in 90nm CMOS.

Paper 24.6 [University of Washington, Intel] presents another 45nm CMOS design. The direct-conversion transmitter operates from 5 to 6GHz and achieves high linearity and multistandard operability in deep-submicron CMOS.

Paper 24.8 [University of Washington] presents an extremely low power GPS receiver. The low-power operation is accomplished by aggressive current reuse in the stacked quadrature LNA-mixer-gate-modulated VCO cell.

The session concludes by highlighting emerging medical applications of wireless technologies. Paper 24.9 [KAIST] presents a dual-band body-area network 0.18um CMOS transceiver supporting 30-to-70MHz body-channel communication and 402-to-405MHz medical-implant communication. Concurrency is exploited to lower power consumption through efficient duty-cycling.

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Session 25 Overview / IMMD [AP70]

Medical

Chair: Albrecht Rothermel, University of Ulm, Ulm, Germany
Associate Chair: Timothy Denison, Medtronic, Minneapolis, MN

Biomedical applications of electronic circuits and systems cover many sensing paradigms, ranging from the electrical signals in the brain to pressure in blood vessels to molecular detection of DNA. Recently, the field has focused on monitoring biological parameters for health care applications both in the clinic and to support fundamental research. In these systems, the optimization of sensor sensitivity and specificity must be balanced with other requirements like power, telemetry, and the overhead of external circuitry. Recent trends in the scaling of circuits, in combination with novel sensing and circuit architectures, are enabling the next generation of medical electronics with a positive impact on health care.

The challenge of scaling systems for implantable applications is addressed in Paper 25.1 [Case Western], which presents a complete system for *in-vivo* monitoring of blood pressure in genetically engineered mice. By adapting RFID technology, the sensor eliminates the need for an implanted battery while providing a telemetry signal for data download.

Enhanced interfacing to the nervous system is crucial for the next generation of devices for treating neurological disorders, and breakthroughs in medical electronics are driving both advances in clinical applications as well as fundamental research. Paper 25.2 [Case Western, Illinois State] provides the first integrated circuit for merging electrical and chemical sensing from a single electrode. The dual sensing paradigm helps to enable basic research that studies how chemical transmitters affect circuit behavior, which could improve our understanding of how therapeutic devices like deep-brain stimulation work and might be improved. Paper 25.3 [North Carolina State, Georgia Tech] enhances multi-electrode neural interfaces by enabling higher bandwidth of dataflow from the implanted sensor with a novel transmitter scheme. This approach helps to break the logjam for getting neural data out of the brain for analysis without lossy compression. An alternative approach to telemetry is to extract key data from the neural signal and run algorithms within the implant. Paper 25.4 [National Taiwan U, UC Santa Cruz] presents a flexible digital-signal-processing-based approach that can be configured for a number of neural engineering problems, most significantly closed-loop epilepsy stimulation. Using a multiprocessor SoC, the device extracts key information within acceptable power limits for implantation.

The final papers address the issue of system integration to reduce the overhead of molecular sensing. Paper 25.5 [UT Austin] presents a fully integrated 7x8 fluorescent-based biosensor microarray for DNA detection applications. The sensor integrates a precise long-pass filter and fiber optical faceplate to enhance the rejection ratio of excitation light to fluorescence. Paper 25.6 [Caltech] describes a magnetic-particle sensor array that does not require external magnetic fields. The sensor can be fabricated in standard CMOS technology and thus eliminates the need for expensive post-processing. Requiring no heavy permanent magnets or power-hungry electromagnets, the integrated sensor shows promise for hand-held medical diagnostic applications.

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Switched-Mode Techniques

Chair: *Francesco Rezzi, Marvell Semiconductor, Pavia, Italy*
Associate Chair: *Philip Mok, Hong Kong University of Science and Technology, Hong Kong*

Switched-Mode Power Converters have long been used in electronic devices due to their capability to efficiently transfer power to a load both as regulators (such as DC-DC or AC-DC converters) or as signal power amplifiers (such as Class-D stages). It is only in recent years, however, that such switching techniques have found widespread use in portable devices with an ever-increasing level of integration due to their inherent capability to preserve battery life and reduce the power losses that determine undesirable temperature increases and impair long term reliability. Furthermore, switching power amplifiers are the preferable and mainstream choice when a large amount of power needs to be delivered to the load such as in the case of high-fidelity Class-D audio amplifiers.

Switched-mode regulators usually rely on external filtering in the form of a lossless LC-tank to attenuate the undesired high-frequency components of the output or reduce supply ripple originated by the switching activity. These bulky components have been long the main obstacle to the use of switched-mode regulators in embedded applications. In recent years, research has been focused on the reduction in size and in the number of these components, either by increasing the switching frequency and/or by adopting single-inductor multiple-output (SIMO) solutions. On the other hand, audio Class-D amplifiers have been plagued with a series of issues such as poor PSRR, limited linearity, poor light-load efficiency and high frequency EMI emissions that need to be addressed with improved closed-loop control and careful design of the output power stages. EMI reduction techniques will allow the elimination of the external filter with significant cost and size saving. Efficiency improvement over the entire range of output power is also an important parameter for portable applications. This session presents three DC-DC converters and three Class-D power amplifiers that address and offer solutions to some of these problems.

The session starts with Paper 26.1 [KAIST, JDA Technology, LG Electronics] that presents a SIMO switching DC-DC converter with vestigial current control. The SIMO converter provides 5 regulated outputs plus an additional auxiliary output terminal. The overall energy from the SIMO is controlled to be slightly larger than all of the outputs need and the excessive energy is stored at the auxiliary terminal. The excessive energy is recycled back to the supply at the end of each switching period to enhance the overall efficiency of the converter.

Paper 26.2 [Georgia Tech] demonstrates an effective way to power up micro-sensors using a micro-scale Li-ion battery and a micro-fuel-cell with a dual-input dual-output single-inductor charger/supply system. The micro-fuel-cell continuously provides energy to the sensor during standby and recharges the micro-Li-ion battery, while the battery can supply peak transmission power to the sensor during signal transmission.

Paper 26.3 [HKUST] describes a digitally assisted quasi-V^2-control buck converter. By using an on-chip RC filter connected across the inductor and a digitally adapted delay compensator, the converter operates stably without using a large ESR capacitor that is necessary for conventional V^2-control converter. The load recovery time is less than 3μs.

Paper 26.4 [Texas Instruments] describes a way to reduce EMI radiation out of a 20W full-bridge Class-D output stage by carefully controlling the common-mode variation at its output. The paper shows a significant reduction of the EMI emissions that meets the FCC Class-B standard making filterless operation possible.

Paper 26.5 [Texas A&M University] presents 2 different architectures for controlling a clock-free Class-D power stage using a sliding-mode control. The driver achieves a peak efficiency of 90% at 250mW with quiescent power consumption below 1mW that enhances the light-load efficiency of the drivers making it attractive for portable application.

Paper 26.6 [NXP] addresses once again the problem of EMI emissions on a half-bridge Class-D output stage with an adaptive gate drive technique that minimizes the EMI emission due to the reverse recovery diode. The Class D output stage delivers a whopping 460W into an 8Ω load with a very smooth transition between the positive and negative ±40V rail.

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Session 27 Overview / Memory

[AP74]

SRAM and Emerging Memory

Chair: Peter Rickert, *Texas Instruments, Dallas, TX*
Associate Chair: *Hideaki Kurata, Hitachi, Tokyo, Japan*

Technology scaling by Moore's Law drives an ever-increasing demand for embedded memory on today's stand-alone and embedded microprocessors and consumer electronics. SRAM scaling is a challenging area requiring design innovation resulting from critical scaling issues such as transistor mismatch, threshold voltage variation, and leakage reduction all under low-voltage operation. These issues are being addressed by designers to continue the scaling trend at 45nm and beyond. Furthermore, significant changes in process technology such as high- metal-gate have been introduced to facilitate the scaling of these important memory blocks.

This session addresses the application requirements with a combination of design innovations in both SRAM and emerging technologies in advanced CMOS processes. These papers describe the full spectrum of device operation, covering scalability, low-power, high-speed and high-density applications. Another important aspect is that applications require high-performance and high-density non-volatile memories. The last two papers in the session target these applications.

Paper 27.1 [Intel] describes the industry's first 32nm high-density and high-performance SRAM in a high- metal-gate technology. Designed for high-end microprocessor applications, this SRAM is capable of operating at 4GHz at 1.0V. Power-down circuit enhancements previously adopted in 45nm are further extended in this 32nm SRAM macro. The fully functional 291Mb chip is tiled using 128Kb sub-arrays and a $0.171\mu m^2$ bitcell and realizes an area efficiency of 72%. The next SRAM, Paper 27.2 [Toshiba], describes a variation-tolerant, dual-power-supply SRAM in 40nm CMOS using a level-programmable wordline driver. This macro features the smallest reported SRAM cell in 40nm ($0.179\mu m^2$) and achieves three orders of magnitude improvement in bitcell failure rate compared to conventional techniques.

The next few papers concentrate on emerging memory technologies. Paper 27.3 [Innovative Silicon, AMD] describes a novel 4Mb DRAM memory macro using a floating-body SOI bitcell that is compatible with an SOI logic process. The macro features a single-ended capacitively coupled sense amplifier that results in 2ns read latency and a 4ns random cycle. The capacitorless memory cell achieves a macro density of $0.21mm^2$/Mb.

The demand for high-speed, high-density, non-volatile memory in consumer electronics motivates the next two papers. Paper 27.4 [NEC] describes a 32Mb MRAM design with a high-speed SRAM interface that achieves a 12ns access time. The 2-transistor, 1-magnetic-tunnel-junction (2T1MTJ) bitcell achieves the highest capacity ever reported in stand-alone MRAM chips. The design features a boosted wordline technique that facilitates a 2× reduction in cell area.

Finally, Paper 27.5 [Toshiba] describes the highest level of integration of a chain FeRAM architecture with 128Mb of density. This stand-alone product features a 1.6GB/s DDR2 interface, which is 8× faster than the previously reported non-volatile memory. The $0.252\mu m^2$ bitcell is the smallest announced at the 0.13μm technology node.

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TD: Directions in Computing and Signaling

Chair: *Ali Keshavarzi, TSMC, San Jose, CA*
Associate Chair: *Satoshi Shigematsu, NTT Microsystem Integration Laboratories, Atsugi, Japan*

In emerging high-performance dependable computing systems, there is a strong need to consider new device and interconnect options. Such systems must not only interface with new constraints (i.e., inter-chip communication without wires), but should also efficiently interface with external world signals. In this session we focus on different components of this complex system covering a range of topics from computing with nanomagnets, to contact-less signaling and testing. We also cover new exciting and diverse applications such as EMI surface distribution detection and integrated single-chip cameras and more.

Energy-efficient, fast, optical I/O technology is being developed for Tera-scale computing systems. Paper 28.1 [Intel] presents an optical I/O architecture utilizing 90nm CMOS circuits, VCSEL/detector array and polymer waveguides. The authors show a 10Gb/s/channel data rate with 11pJ/b energy efficiency while showing a path for achieving 20Gb/s at 1pJ/b for their future integrated systems.

Paper 28.2 [Keio U and NEC] highlights the subject of testing research. Testing is critical in achieving scaled low-cost VLSI systems. The authors of paper 28.2 propose a low-power testing solution for 3D-integrated systems based on inductive coupling that achieves about 20% lower cost with minimal additional overhead. These results point to trends in new contact-less testing applications.

Paper 28.3 [U Tokyo and Max Planck Institute] demonstrates an exciting application for low-voltage CMOS organic technology that interacts with silicon chips. The authors show detector circuits in their stretchable electronic medium to measure EMI radiation from electronic equipment by wrapping the flexible detector sheet around electronic equipment with sensitivity of -70dBm. This will bring about new testing solutions.

Paper 28.4 [Technical U Munich and U Notre Dame] is a direction paper that investigates a new computing paradigm with coupled magnets. The authors will stimulate the ISSCC audience with futuristic programmable ferromagnetic computing devices that are energy-efficient at rates of less than 10aJ/switching event. These elements are capable of parallel information processing with the extra benefit of interconnect-free nonvolatile computing that is immune to radiation.

Finally, the session concludes with a set of papers in the exciting field of 3D integration. Paper 28.5 [Toshiba] presents an application of 3D chip stacking using TSV (Through-Silicon-Via) technology for a chip-scale camera. The authors reduced the volume of their imager system by half and lowered the cost by 25%. This camera chip will be the first high-volume product utilizing TSV technology.

Paper 28.6 [Kyushu Institute of Technology] discusses another interesting application and a methodology for future vision systems. The authors demonstrate their cellular neural network based contour generation approach on a small-scale silicon array that is targeted to the larger goal of future 3D and brain-like vision systems.

Finally, paper 28.7 [Keio U, Renesas, and Hitachi] concludes these exciting trends by demonstrating for the first time communication channels between 3D-stacked microprocessor and memory chips with contact-less inductive coupling link technology. The authors show that their energy-efficient link is capable of 1pJ/b at a data communication rate of 19.2Gb/s per link. Their channels are area-efficient at 0.15mm^2/Gb/s. These results are significantly better than conventional DDR2 results. They show that the microprocessor and SRAM can be from different technologies running at their respective optimized power supply voltages while communicating in close proximity via inductive coupling.

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mm-Wave Circuits

Chair: *Francesco Svelto, University of Pavia, Italy*
Associate Chair: *Piero Andreani, Lund University, Lund, Sweden*

Nanoscale silicon ICs prove to be suitable for applications at ever-increasing frequency. In recent years, building blocks and even complete transceivers operating at mm-wave (24GHz, 60GHz, 77GHz etc.) have been presented at this conference, and investigations beyond these frequencies are well under way. Applications are foreseen in the areas of ultra-high-speed wireless communications, security, remote sensing, medical imaging, and detection of explosives and chemical agents. High-definition mobile interface (HDMI) for wireless video down-streaming and cable replacement, and automotive radars for active cruise-control systems are expected to hit the market shortly. IC designers are actively leveraging the inherent speed of scaled CMOS while overcoming the inevitable problems associated with advanced processes, such as low breakdown voltage, small intrinsic gain, limited output power capability, and higher parasitic resistance. Meanwhile, the introduction of architectures such as phased arrays, borrowed from the military, is expected to improve the sensitivity of receivers and the radiation efficiency of transmitters. This session presents advances in the design of mm-wave building blocks in silicon technologies, covering voltage-controlled oscillators, phase-locked loops, amplifiers, and front-ends.

Paper 29.1 [UC Santa Barbara, IBM] shows a 150GHz 8dB-gain amplifier capable of 6.3dBm output power while consuming 25mW from 1.1V. The chip is realized in 65nm digital CMOS. The session continues with insights into the design of W-band amplifiers, proposed in paper 29.2 [Helsinki University of Technology]. Operating around 100GHz with a -3dB bandwidth of 21GHz, the amplifier employs passive components shielded from the substrate and achieves 13dB gain, 7.5dB noise figure, and a saturated output power of 10.5dBm. Paper 29.3 [UCSD] introduces a new amplifier topology, combining the features of traveling-wave and cascaded amplifiers. Built in a 0.12µm SiGe BiCMOS process, the amplifier displays an unconditionally stable gain as high as 26dB at 100GHz, with a -3dB bandwidth of 14GHz and a power consumption of 82mW from a 2V supply.

Paper 29.4 [U Minnesota] presents new phase-generation schemes, based on injection locking, for local oscillator phase shifting in phased-array receivers. Operating at 2.4GHz, the chip demonstrates operation of three channels in the array. Each channel includes a down-converter and a phase-shifting locked oscillator. The adder is also integrated on the chip, realized in 0.13µm CMOS. A maximum gain of 20dB and a signal-to-noise-ratio improvement of 9dB are demonstrated. The total power consumption is 42mW.

Paper 29.5 [IMEC, KU Leuven, Vrije Universiteit Brussel] reports a 57-to-66GHz 45nm CMOS front-end. The prototype shows 26dB gain and 6dB NF while consuming 19mA from 1.1V supply. The chip is ESD-protected and occupies only 0.023mm^2.

Paper 29.6 [IMEC, Vrije Universiteit Brussel], presents a quadrature PLL in 45nm CMOS. The chip includes two quadrature VCOs, with an aggregate tuning bandwidth between 57GHz and 66GHz, and a tunable injection-locked prescaler. The phase noise at 61.6GHz is -82dBc/Hz at 3MHz offset, for a power consumption of 78mW from a 1.1V supply. The reference spur level is -42dBc.

Finally, paper 29.7 [Hitachi] reports a technique for collecting the output second harmonic, using a loop- ground transmission line, in a 46GHz-to-59GHz wide-band push-push VCO in 0.18µm SiGe BiCMOS. A high output power of 1.2dBm and a low phase noise of -108dBc/Hz at 1MHz offset are achieved with a power consumption of 120mW from 3V.

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This and other related topics will be discussed at length at ISSCC 2009,
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Processors Achieve Breakthrough Levels of Integration

Despite Gordon Moore's own admonition that transistor size scaling cannot continue forever, high-performance-processor designers continue to increase the level of chip integration, with resulting improvement in system performance. Growing numbers of processors and increased cache size lead to faster systems, but also make off-chip communication an important performance bottleneck, decrease chip reliability in the face of soft errors and defects making error correction a commercial necessity, while making distribution of a clean clock and a clean power supply an increasingly difficult task. Circuit innovations in these areas have become crucial to advancement processor design.

At ISSCC 2009 engineers from Intel will highlight a family of next-generation 45nm processors that set breakthrough records in transistor count and performance, using a number of such circuit innovations. A processor incorporating eight dual-threaded 64b x86 cores and a large shared L3 cache employs four power supplies, 16 phase-locked-loops (PLLs), and 8 delay-locked-loops (DLLs). Error-correction code in the memories corrects double-bit errors and detect triple-bit errors for higher system reliability and availability. Other processors based on the same x86 core form a wide family of products, all sharing a number of base technologies, such as a coherent point-to-point scalable interconnect that increases off-chip bandwidth up to 6.4 gigatransfers per second over a conventional copper bus. Also, power-gate transistors shut off individual idle cores to completely remove their idle power; architectural state is stored in chip memory and restored when the core wakes up. A dedicated microcontroller manages the unified power state of the processor based on environmental conditions, processor frequency, voltage, and workload. Finally, a different 45nm integration of six x86 cores demonstrates the benefits of a low-leakage technology process and a layout optimization that places off-chip I/O pads toward the center of the chip.

This and other related topics will be discussed at length at ISSCC 2009,
the foremost global forum for new developments in the integrated-circuit industry.
ISSCC, the International Solid-State Circuits Conference,
will be held on February 8-12, 2009, at the San Francisco Marriott Hotel.

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Cheaper and More Power-Efficient SoCs Through 3D Integration

SoC complexity continues to increase as vendors cram more and more functionality into their products. As a direct consequence, more SRAM memory must to be included in order to support increased functionality and integration. Integrated SRAM causes area and power to increase. Furthermore, it is statically allocated (at design time) to functional blocks and may be underutilized if such functional blocks are not used or stay in the sleep mode for certain applications. In addition, due to the static allocation, memory bandwidth requirements may not be efficiently addressed for all possible applications.

At ISSCC 2009, in San Francisco, engineers from NEC, in Paper 3.3 present an interesting solution to this problem. In their improved structure, SRAM is separated on a different chip which is stacked on top of the high-functionality SoC containing a number of IP cores. Communication between the two chips is accomplished through newly developed high-density inter-chip electrodes spaced at a 10μm pitch as opposed to the current microbump solution which has a 50μm pitch. The SRAM chip contains multiple SRAM blocks that can be dynamically reconfigured with very low latency through switch arrays and connected to the IP cores on the main SoC. Timing between the IP core and the memory chip is matched through retiming circuits. The 2D structure of the memory arrays on the SRAM chip also allows bandwidth control so that the memory bandwidth can be matched to the IP core requirements. Moreover, the closer proximity of the memory to the IP core results in lower access latency which increases performance.

This technology has the potential to lower the cost and power requirements of SoCs by moving the embedded memory to a standalone stacked chip that can be customized for the application by appropriate choices of memory size, latency, and bandwidth. Due to the reconfiguration capabilities of this method, more products and applications can be enabled from a single SoC design. The potential cost reduction can be quite significant!

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An All-Digital Temperature Sensor with One-Point Calibration for Thermal Monitoring

Modern microprocessors need on-chip temperature sensors for thermal monitoring and power management to detect hot spots and to monitor overall chip temperature in order that the chip stay within the allowed power envelope. The temperature sensors should be small in area and power, and be realized using all-digital techniques.

The method described is based on temperature-dependent CMOS inverter delays and uses two fine precision delay-locked loops, one to synthesize a temperature-independent delay reference in a closed loop and the other as a temperature-only-dependent delay line. The use of an all-digital method allows easy porting to advanced technologies. As well, this technique gives a high measurement bandwidth (5000 samples/second), which allows fast transient temperature tracking during processor operation. The method allows a one-point calibration, greatly simplifying testing. Power dissipation is only 1.2mW and temperature accuracy is within ±2.3ºC.

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Bringing Home the Bandwidth!

Our connected society is linked by a fibre-optic backbone to meet our insatiable appetite for more and more bandwidth. A fundamental requirement in implementing high-speed long-distance communication is for precision timing, without which data cannot be accurately transmitted. At ISSCC 2009, engineers from National Taiwan University and Industrial Technology Research Institute (Paper 5.2) will present a new concept for timing generation that delivers this needed accuracy at a dramatically lower cost, for the circuits that are used to send and receive data in tomorrow's networks.

But, not everyone has optical fibre into their home - there is an enormous installed base of plain old copper telephone wires using digital subscriber line (DSL) services to supply data to a bandwidth hungry consumer. However, today's sluggish 0.5Mb/s to 8Mb/s DSL interfaces cannot deliver the triple play of voice, data, and high-definition video. To overcome these limitations, engineers from the University of Pavia and Marvell (Paper 5.10) describe a fully-integrated VDSL2 interface which delivers an astonishing 200Mb/s data rate to the home over 100 meters of legacy-copper telephone wires!

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Mobile Internet for Everyone!

High-speed mobile Internet is entering a new era of integration. The high-speed packet access (HSPA) technology for 3rd generation cellular systems will enable new services and improved user experience for consumers both in business and leisure. Internet is driving wireless technology development, and data traffic is rapidly overtaking voice communications in cellular networks. Especially in Europe, the networks are being upgraded to provide multi-Mb/s data rates for mass markets. Growing markets boost technological advances but also demand highly-cost-efficient solutions. The Internet experience will be adapted to a mobile context. Convergence of the Internet and mobile phones will redefine the way we understand the Internet in coming years. Mobility and the Internet open the door for new services that can be built on top of high-speed connectivity and awareness of the location. Advanced mobile phones are in fact Internet devices that can be used both for consuming and creating content. Music, photographs and streaming video will be distributed in increasing amounts. Those include services both produced by the media industry, as well as, people sharing their own experiences with each other. Of course, all of this should be possible anywhere in the world. But, that has posed tremendous challenges for the engineering community required to provide solutions that, until recently, we could only dream about. Although the mobile Internet will probably result in a more significant change in social relationships in the coming years, there is also a strong demand to bring even higher-speed Internet with cable to homes.

At ISSCC 2009, a new level of advancement in integration will be described. The chips presented will eliminate most of the expensive and bulky SAW RF filters, ensuring global adaptivity. Globally, fragmented spectrum allocations call for chipsets that are capable of operating in more than ten different RF band combinations. Without extensive removal of filters, the solutions would be too expensive for mass markets. At the same time, highly-adaptive circuits and systems are required to allow backward compability with older networks, including 2nd generation GSM that is still a highly-efficient solution for voice calls. Conventionally, this has been a major bottleneck especially in RF integration. At ISSCC 2009, solutions that have surmounted these hurdles will be presented.

At ISSCC 2009, a system-in-package (SiP) receiver with transmitter functionality on the same ASIC, resulting from the joint effort of ST-NXP Wireless and Ericsson Mobile Platforms (Paper 6.2), will be described. An RF single-chip transceiver with standard digital interface from Skyworks Solutions and Spectra-Linear (Paper 6.3), and an RF transceiver with GPS functionality from Qualcomm (Paper 6.4) will present a new era in radio communications. All three developments exhibit a high level of integration, but also a selection of different technological and architectural choices. The SiP transceiver by ST-NXP Wireless and Ericsson Mobile Platforms demonstrates well-balanced approach to partitioning the system between ASIC and lower-cost technologies within the same package. The CMOS solution from Skyworks Solutions integrates a significant part of the digital functionality in the RF chip and uses a standard digital interface to allow compatibility with different digital-processing platforms. The transceiver by Qualcomm shows the highest level of RF functionality. It employs two receive branches where the second signal chain can also be configured to GPS functionality whenever position is requested.

Low-cost ubiquitous Internet is enabled by the cellular transceivers that will be presented at ISSCC 2009. With these innovations pervasive mobile Internet is ready to stimulate new modes of creativity by individuals and communities.

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DRAMs Enter the Next High-Performance Stage

Although the worldwide economy suffered a financial slowdown in 2008, the performance of DRAM, its bit capacity, its power per chip, and its speed all improved while applications of DRAM further diversified.

Details of these dramatic positive developments in the face of economic decline will be detailed at ISSCC 2009, in San Francisco. Engineers from Samsung will present a DRAM with a chip capacity that has reached 4Gb by using the most advanced 56nm CMOS DRAM technology (Paper 7.1). Interestingly, at the same time, the DRAM density per chip can be increased to 8Gb by stacking four DRAM die and joining them through via connections, all within one package to achieve another density record in DRAMs (Paper 7.2).

As well, at ISSCC 2009, engineers from Hynix will present a low-power DRAM a with high-bandwidth DDR2 interface providing up to 4.3GB/s but using only a low-voltage supply of 1.35V (Paper 7.3). Such a supply is very advantageous in mobile applications.

As well, the speed of graphics DRAM has reached 7Gb/s/pin. Engineers from Qimonda will present the world's fastest memory chip intended to make 3-dimensional graphics presentations on HD (high-definition) panels more lively (Paper 7.4).

Details of the implementation of this new scheme will be revealed at ISSCC 2009 at the San Francisco Marriott Hotel in February.

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Full-HD Video Will Be Affordable, Soon

The latest technologies in display panels, digital storage, and broadcasting, are driving High-Definition (HD) video into the mainstream. Even Full-HD is appearing quickly, since it provides higher resolution (1920x1080) than HD (1280x720). However, the handset, which is the most affordable and easily accessible device for capturing video, offers only up to DVD resolution (720x480: D1) today. The realization of an HD video solution is still challenging for availability in 2009. All of this is due to its high power consumption and memory bandwidth, not to mention Full-HD resolution on the horizon. Another key player in the Full-HD world, Blu-ray, is still not as affordable as basic DVD players because the complexity of the system and the diversity of disc formats make it expensive.

This year, at ISSCC 2009 in San Francisco, several new SoC realizations will be presented to make Full-HD video affordable to the consumer world. They introduce breakthrough technologies which reduce power consumption and implementation area. Renesas will introduce the first Full-HD Mobile-Application Processor in 65nm to support multi-standard video codecs (MPEG-2, MPEG-4, and H.264) for handsets. A low power consumption of 342mW is achieved while playing H.264 video at Full-HD resolution running at 166MHz. This is only 55% of the power of the media processor that appeared in ISSCC 2008. With the introduction of this SoC, it is likely that the first handset with Full-HD camcording capability can be introduced to market in 2009 or 2010.

At ISSCC 2009, engineers from MediaTek will introduce the first fully-integrated backend SoC for Blu-ray players including content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3. They further lower the system cost by reducing area by 14.36% by sharing the computation resources. This Blu-ray SoC integrates the HDMI 1.3 outputs by applying a direct-digital synthesizer (DDS) and a new transition-minimized differential signaling (TMDS) structure to reduce the additional external capacitor and to improve the jitter performance. This cost-effective solution will make Blu-ray players less expensive and more affordable.

As well, engineers from National Taiwan University will introduce a scalable video-encoding chip which supports both multiple-HD and Full-HD resolution. The chip can decode video up to 1-view Quad Full-HD (4096x2160), 3-view Full-HD or 7-view HD for multiple or 3D-display applications. This highest encoding resolution is achieved by employing a cache-based prediction core, that results in a 79% reduction in system bandwidth, and a 95% reduction in on-chip SRAM area. Thus the writing is on the screen: Video resolution up to Full-HD is no longer limited to large or costly systems.

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Affordable Bandwidth: CREATIVE DESIGN in Advanced CMOS

Got enough bandwidth? Come to Session 10 of ISSCC 2009. You will learn how to get it affordably. Nowadays, Internet traffic is handled at data centers distributed around the world by switching and routing chips which communicate with each other through multi-gigabit transceivers over legacy backplanes that use over half-century-old FR4 materials. Correspondingly, the amount of data that can be transferred in and out of a chip in a second is limited by the speed of each port, and the number of ports available. The number of ports which can be integrated in a chip is limited primarily by the power dissipation of each port: How fast each port can run is limited by the imperfection of legacy backplanes used by most of today's servers.

This year, at ISSCC 2009, engineers from Intel (Paper 10.1) and Hitachi (Paper 10.4) will present circuit techniques that can efficiently realize key functions of the transceivers compensating for inevitable channel impairments. Intel will demonstrate the lowest power consumption to date using a creative circuit implemented in the most advanced 32nm CMOS technology. As well, Hitachi will demonstrate the first 10Gb/s transceiver for lossy legacy backplanes, dissipating only 230mW. These are important milestones! Critically, the 10Gb/s rate at which they can operate is the rate at which copper and fibre channels can seamlessly exchange data, allowing legacy copper systems to be upgraded effectively by the selective addition of intervening fibre links.

Based on these state-of-the-art transceivers, we can project that as CMOS device geometry gets even smaller, some day in the near future you can sit in your couch enjoying high-definition videos over the Internet at an affordable price.

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RF Spintronics and Its Merger with CMOS

Electrons act as if they are spinning, and this spin property makes electrons behave like tiny bar magnets. While the dominant paradigm of today's electronics is to control the flow of charges carried by electrons, taking advantage of the "electron magnets" for signal processing has been of intense research interest over the past few decades. This spintronics paradigm is aimed at benefiting, if not replacing, the current kind of electronics to a substantial degree, with the advantage of significantly lowered use of energy.

One recent spintronics technology involves building a radio-frequency oscillator using the motion of electron magnets. By injecting a spin-polarized current, which contains electron magnets lined up along the same direction, through a thin ferromagnetic layer where electron magnets can freely change their directions, one can induce wobbling motions of the free electron magnets in the ferromagnetic layer. The period of these wobbling motions typically lies at a radio frequency, thus, corresponding to a radio frequency signal.

The spin-based RF oscillator is advantageous over conventional LC oscillators in terms of area and tuning range. The area can be more than 10× smaller than an LC oscillator, and the tuning range is many times larger than an LC oscillator. At ISSCC 2009, engineers from CEA, Hitachi, and ST (Paper 11.1), will describe how they build upon the concept of the spin-based RF oscillator. For the first time their work reconfirms the tuning range advantage (85%), and the area advantage (50× smaller than a corresponding LC oscillator), but it also demonstrates its inter-operation with CMOS electronics (for example, injection locking of a CMOS oscillator). Using a spin-based RF oscillator in conjunction with current CMOS electronics is the key contribution of this work.

The 2007 Nobel Prize in physics went to the discovery of giant magnetoresistance (GMR), which marks the birth of spintronics, and has had a great impact on data-storage applications. It remains to be seen if spintronics would benefit and change signal-processing electronics, but like all technological advances and failures, its ultimate success would be determined by continued research activities. The spin-based RF oscillator represents an interesting facet of spintronics, in which its usefulness can be assessed in conjunction with CMOS electronics.

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Insect Cyborgs and Micro-Robots!

For decades, scientists and engineers have been fascinated by cybernetic organisms, or cyborgs, that fuse artificial and natural systems. Cyborgs enable harnessing biological systems that have been honed by evolutionary forces over millennia to achieve astounding feats. For example, moths can detect a single pheromone molecule. Thus, moth cyborgs could perform tasks at scale and efficiencies that would normally seem incomprehensible. Semiconductor technology is central to realizing this vision offering both signal-processing and communication capabilities, as well as low weight, small size and deterministic control. At ISSCC 2009, engineers from MIT (Paper 11.3) will present an emerging cyborg application involving moth-flight control and demonstrate an early-stage version involving a UWB-radio-controlled chip employing 2.5mW power.

Another exciting application of semiconductors is microrobots. These simple autonomous robots are mobile physical platforms that are primarily focused on motion. They are designed to move, sense, take decisions, communicate and work cooperatively with others of their own kind. Area and weight are critical issues that dominate the design of these simple machines that have their own scavenged power source. This year, at ISSCC 2009, engineers, from the University of Barcelona (Paper 17.9), will describe an optically-programmed chip including all of the controller functions needed by a tiny few mm^3 autonomous microrobot.

Microelectronics are beginning to enable very low-power microsystems that promise truly revolutionary applications and innovations!

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"Body Language" – A New Personal-Communications Paradigm

With the growth of the ageing population, continuous health monitoring and efficient drug delivery are crucial for quality patient care and therapy. For continuous monitoring, vital signs have to be acquired by on-the-body sensors and transmitted for better diagnosis and earlier detection of health problems. The health data provided by the body network can then be used for such things as targeted drug delivery for localized cancer diagnosis and therapy. To this end, compact and energy-efficient integrated micro-systems are currently being developed for body communication.

This year, at ISSCC 2009, engineers from KAIST (Paper 17.3) will present a health-monitoring chest band which includes an array of silk-screened coils that are used to both communicate with and power wirelessly the many sensors placed on different parts of the chest to capture vital signs such as temperature, ECG, blood pressure, skin conductivity, respiration and many other parameters. The sensor network can configure itself depending on the sensors available on the body thanks to a new 15mm^2 network controller chip integrated in 0.18μm CMOS. It also provides the electrical power to the sensors electronics through magnetic coupling and highly-efficient voltage rectifiers. The 0.18μm CMOS 4.8mm^2 sensor is embedded on bandages that contain the coil and all the integrated electronics that converts the AC voltage from the coil to supply a DC voltage to the chip and transmits back the collected signals. The chip is also able to acquire very low level signals, process and transmit them to the network where they are collected and eventually stored or transmitted forward. The main new features that were developed by this Korean group is the self-configured network combining energy-efficient powering and communication with an ultra low-power (12μW) sensor chip.

Although the data collected from sensors on or in the body can be transmitted through a wireless body area network (WBAN), one could also use the body itself as a transmission media using its conductive properties. This way of transmitting signals is called body-coupled communication or BCC. The transmitter for BCC can be realized using two transceiver devices capacitively-coupled via two electrodes to the body: The transmitter generates a variable electric field, while receivers sense the corresponding potential gradient on the body. As well, engineers from Philips Research (Paper 11.5) will present their development of a low-power wideband transceiver for BCC. It uses a frequency band from 1 to 30MHz, avoiding the interference that can occur at higher frequency. The BCC transceiver can achieve an 8.5Mb/s data rate with a sensitivity of 350μV for a 10^{-3} bit error rate (BER) and consumes 2.75mW from a 1.2V supply. The circuit is implemented in 0.13μm CMOS. The low-power operation is achieved thanks to a very simple analog-circuit implementation using analog correlators.

Finally, engineers from National Taiwan University (Paper 17.2) will present a novel implantable release-on-demand drug-delivery wireless-coupled device, which can precisely control key therapeutic parameters. A 3x3mm^2 spiral inductor working as an antenna for communication, a rechargeable lithium-ion battery and a PCB containing a chip which includes an array of 8 reservoirs of 100nl are integrated in a system-in-package (SiP). The reservoirs can be individually addressed to release the drug after the rupture of a membrane due to electro-thermal heating. The membrane operation is similar to the blowing of an electrical fuse. The eight reservoirs are monolithically integrated on the back of a CMOS chip using a CMOS-compatible post-IC fabrication process. The low-power CMOS chip, integrated in a 0.35μm process, is a complete system-on-chip (SoC) including a receiver, a microcontroller and a switch array to individually address the drug reservoirs. The command is received from an external OOK transmitter, operating in the 402 to 405MHz MICS band, which can communicate the required parameters to release the desired drug from the corresponding reservoir. The overall system is sufficiently small (actually a cylinder of about 5mm diameter and 4mm height) which can be implanted into the body in order to release the drug at the specific location.

The symbiosis of wireless body area networks, body-coupled communication and smart drug-delivery and smart measurement systems will significantly impact healthcare monitoring. This will assure the accuracy and timeliness of diagnoses supporting personalized therapies for lowered cost of healthcare.

Such developments portend the future of body-focused communications in the area of healthcare, particularly for the aged!

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Organic Electronics Growing!

Traditional electronics allows the integration of billions of tiny transistors on small, brittle pieces of silicon crystal that we call chips. Silicon electronics is fast, accurate and reliable, but is stiff and cannot cover large and flexible surfaces, such as, a newspaper, snack packaging, or a bottle of milk.

On the other hand, organic electronics is a new development where transistors are made using carbon-based (organic) materials, such as, common plastic. In this way, electronics can be printed on thin, flexible and large films. Organic electronics is excellent for most applications where silicon electronics has problems: It can be manufactured at room temperature; it can be bent; it is fast to produce, and can cover very large surfaces. However, organic electronics has problems in areas of performance in which silicon excels: It is slow; it is not accurate; it is vulnerable to noise, and to the variability of the production processes. Also, the complexity of electronic functions that can be implemented with carbon-based materials is rather limited (thousands of organic transistors integrated in a circuit are currently a world record, while billions is the record for silicon).

At ISSCC 2009, two new trends in organic electronics will be seen to emerge: On the one hand, carbon-based electronics will be shown to have become increasingly more complex and robust. Engineers from IMEC, Polymer Vision and TNO Science and Industry (Paper 11.6) will describe the first organic RFID tag, one containing 128 bits of data, an information content similar to low-end silicon RFIDs. Such organic RFID transponders could be printed on the packaging of common goods: A bottle of milk or a box of cookies, replacing the usual bar code but carrying far more information. RFIDs on retail items would enable great improvements in logistics and retail organization. Organic electronics are normally made using only p-type transistors. Integrating both p- and n-type transistors in an organic CMOS technology increases robustness against electric noise coming from the environment and makes it possible to reduce the operating voltage. The first complementary organic type RFID transponder, using n- and p-type transistors, will be presented by engineers from PolyIC (Paper 11.7).

On the other hand, in an effort to combine the best of silicon and of organics, engineers and researchers from the University of Tokyo and the Max Planck Institute, (Paper 28.3) will present a foil sheet able to map EMI on large surfaces. It is built as a flexible foil where organic circuits are wired to silicon chips using stretchable interconnects. Organic circuits are large and flexible and can be directly attached to the foil. They manage the interconnection between small, specialized silicon chips that can pick up the electromagnetic radiation present at different points on the foil. This is just an example of the possibilities of integrating large and flexible organic circuits with fast and accurate silicon. Applications such as, intelligent touch-sensitive displays, electronic interactive whiteboards, “intelligent floors” to monitor the presence and activity of people in a room, are other examples.

Thus, organic electronics is rapidly advancing, becoming increasingly more complex and robust, even complementing silicon!

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NAND Flash Goes to 34nm CMOS, to 64Gb, and to 3D Stacking

NAND Flash once had severe problems with device scaling that prevented them from achieving high capacity, and high performance. Now, these limitations are being overcome by advanced design techniques. Devices, processes, and packages are being optimizated to new levels of performance. Such are the developments to be described at ISSCC 2009 in San Francisco.

Engineers from Intel will describe the first published NAND Flash memory in advanced 34nm CMOS with 32Gb capacity (Paper 13.1). This mulit-level-cell (MLC) chip has a read time of 50μs, programming time of 900μs, and write throughput of 9MB/s. To boost performance, this Flash uses a center-page buffer shared between upper and lower half-planes.

To overcome severe inter-cell capacitive coupling that can cause program and erase disturbances which prevent usual NAND Flash from further scaling, this MLC NAND device uses a 33-cell string to minimize edge effects, and avoid high-precision voltage regulators needed to compensate wide cell-parameter variations. Furthermore, dedicated voltage regulators are designed for cells in different string locations. They can be trimmed by DACs and multiplexed to generate proper voltages on demand.

As well, engineers from Sandisk and Toshiba (Paper 13.6) describe a 64Gb Flash, the highest capacity in a single-chip NAND Flash yet reported. In 43nm CMOS, this memory packs 4-bits per cell to improve memory density with 5.6MB/s write throughput, with a novel all bit-line (ABL) architecture, a three-step programming method, and a sequential-sensing concept for read-verify-write.

If the memory capacity is not enough for SSD, engineers from Keio University and University of Tokyo (Paper 13.5) enable stacking up to 64 chips using inductive-coupling techniques. Demonstrated in 0.18μm CMOS, this technology uses a wireless interface to communicate between chips to reduce power consumption by 2×, I/O area by 40×, to achieve 2Gb/s data rate. These techniques can reduce the number of packages by 8× to achieve even smaller form factor.

More implementation details will be revealed at ISSCC 2009 at the San Francisco Marriott in February.

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"Who Needs Wires?"

Circuit designers have found a new way to connect micro-chips without wires. Using micro-coils on each chip and magnetic interactions, data can be transferred among micro-chips without bondwire connections. This wireless approach potentially reduces cost, area, and power consumption, significantly.

At ISSCC 2009, engineers from San Disk and Toshiba (Paper 13.5) will present a very exciting application of such inductively-coupled wireless links. Application within Solid-State Disks (SSD) is revealed for the first time. Flash memory chips are required within an SSD. By removing the data-communication wires among the flash memories and replacing them with wireless links, the power is reduced by half and the communication circuit area by 40 times. The net benefit is that the users of notebook PCs will enjoy longer battery life and lower cost for the SSD.

As well, at ISSCC 2009, engineers from Keio University, Renesas Technology and Hitachi (Paper 28.7) will introduce the application of wireless links to a processor system. A wireless link between a processor and a memory is shown to reduce the communication power by 30 times and area by 3 times. Again, the primary benefit is that the battery in your portable device will last longer. Previously, wireless links have been used to transfer digital signals but the circuit innovation to be presented by engineers from Keio University and NEC (Paper 28.2) will expand the application to the analog domain. In the applications described, this chip promises to reduce cost in chip testing.

In the future, when new wireless chip-link technology comes into full play, who will need wires in connecting micro-chips?

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Breakthroughs in Body Monitoring

Body-area networks are appearing for various body-centric applications such as sports, personal heath care, and medical applications. Today, wireless standards (such as Bluetooth and Zigbee) enable products in this area. But this approach is bulky and energy consuming, using such technology wireless sensor nodes placed around and even on the body require batteries, making them heavy and awkward. Correspondingly, the goal for the future is to create wireless sensor units and networks not using batteries at all, but exploit energy which can be scavenged from the body or from the environment. Applications for such potentially small wireless connected systems are numerous, ranging from already-existing heart rate monitors for athletes, to more futuristic sleep-detection and emotion-monitoring devices improving, for instance, your driving safety.

This year, in February, at ISSCC 2009, engineers from the Massachusetts Institute of Technology and Katholieke Universiteit Leuven will show fully-integrated pulse radio receivers, combining analog RF circuitry and the digital baseband circuitry which reduce the power consumption for wireless communication. Such developments, in the future, will enable the creation of battery-less wireless sensor units for on-body application. This field of research is still moving quickly, with many experimental designs on display. By next year, we may see the commercial appearance of pulse radio in such low-energy applications.

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Antennas: Why Use One When More is Better?

Ever wonder why taxis have many antennas nowadays? It could be that they are equipped with AM/FM radio, dispatch radio, or even TV. Or, it could be that one of the wireless receivers has more than one antenna. More antennas not only offer better wireless-reception quality but also can support "high-rate" wireless communication that provides higher throughput than available with traditional single-antenna receivers.

This year at ISSCC 2009, engineers from the University of Toronto (Paper 14.4) will present an IC that achieves four times the bit rate of a single-antenna receiver. This novel detector IC uses the so-called "spatial multiplexing" technique, which distributes the transmission data among four transmitting antennas. The receiver, using four receive antennas, can then decouple the information streams that have been mixed during wireless transmission and reconstruct them through a smart and efficient tree-type search. In the end, four times the data are sent in any given time interval, without requiring more precious spectrum, thus significantly increase the achievable data rate.

The IC to be reported is low cost and consumes much less power, and provides higher bit rates than previous designs. Its simple design and small area allow easy integration within future handheld wireless-communication receivers, such as WiFi, WiMAX, and 4G.

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CMOS mm-Wave Circuits Portend Consumer Systems

Newly emerging techniques such as mm-wave sensing and imaging, and anti-collision radar systems require low-cost building-block solutions for the frequency range of 100GHz and beyond. Such systems can improve the overall quality of life, for example, by enabling safer cars and replacing hazardous X-rays. Historically, mm-wave circuits have been the realm of costly compound- semiconductor devices. Now, with advancements in CMOS technology, the operating speed of CMOS transistors is steadily increasing.

This year, at ISSCC 2009, Session 16, on "High-Speed and mm-Wave Circuits", will present advances in CMOS clock-generation circuits breaking the barrier of 130GHz set earlier. With a creative design, engineers from National Taiwan University (Paper 16.5) will demonstrate that achieving such astounding speeds is possible using a 65nm CMOS process.

As well, engineers again from National Taiwan University (Paper 16.2), will present a PLL that is implemented in 65nm CMOS with the highest-reported frequency of operation (96GHz). These papers confirm the feasibility of designing mm-wave wireline/wireless systems in CMOS by providing power-efficient solutions for frequency division at high frequencies.

These benchmark developments will encourage the technical community to carry out further research in mm-wave circuits for higher speeds. As well, look forward to more-diverse applications.

This and other related topics will be discussed at length at ISSCC 2009,
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In-Tire-Pressure Monitoring
A Major Step in Automotive Security

Currently, electronic tire-pressure monitoring provides a significant contribution to automobile security. The US has pioneered this topic: They have mandated tire monitoring in all new cars; such a system would warn drivers of out-of-bounds tire pressure. The sensor used in most systems is a micromachined silicon-based device. Silicon controlled by a logic chip is used to control the CMOS integrated circuit. The sensor is intended to use power-saving features allowing a small battery to operate for more than ten years. The entire miniature system is mounted on the rim of each tire.

A second generation tire-pressure monitoring system has recently emerged. In it, the sensor is embedded in the rubber tire itself, providing major additional information besides pressure: Tire friction detection through the tire–road interface, allowing side slip and traction to be monitored; Furthermore, we may obtain information about wet/dry road condition for engine control and provide feedback to the power train; Other parameters of interest are load detection, tire temperature, wear, and wheel speed. Much of this information could even be used for car-to-car communication purposes to improve safety and provide early warning to other drivers.

Each tire may in addition be equipped with an identification number for fleet management control input of ABS parameters, and location of the tire. Moreover, the identification number can prevent incorrect or damaged tires from being improperly mounting on the car.

Thus, in-tire pressure monitoring appears attractive. But, this option comes at a price. Do we need a lot of new sensors? The answer is NO! The existing pressure sensor and an acceleration sensor (which already exists in today's systems to detect movement of the car) will do! Other restrictions and specifications are much more critical. However, the weight of the complete system is limited to 5 grams (0.2 ounces); otherwise the tire would become unbalanced. This fact limits the size of the battery and consequently demands very low-power consumption. Furthermore, a high degree of robustness is required; the device will have to withstand acceleration of up to 3000g. This level of acceleration makes a 5 gram sensor unit appear to weigh as much as 15kg!

At ISSCC 2009, engineers from Infineon Technologies (Paper 17.1) will provide a first demonstration of an in-tire pressure-monitoring system. 3D vertical integration of silicon chips and the use of an energy scavenger limit the weight and size of both the electronics and the power unit. 2.45GHz bulk-acoustic-wave-based resonators are used to reduce the power consumption, and sophisticated power-down methods are employed for the same purpose. A molded interconnect device is used as a housing to provide the lowest possible outline at maximum robustness. A hardware demonstration is operational. Various measurements will be shown at the coming ISSCC.

Does this result mean that we may enjoy the benefit of an in-tire sensing system soon? We must admit that a lot more work has to go into that research topic before we will see it in cars. It may take another 10 years from now before weight, volume and power consumption of the in-tire pressure-monitoring system will have been further reduced, and robustness will have been further enhanced to allow market deployment.

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Chips that Save Lives!

CMOS technologies are enabling rapid progress in biomedical applications. Such a life-saving chip is to be reported at ISSCC 2009, in San Francisco, in February.

Engineers, from National Taiwan University (Paper 17.2), will present the first implantable CMOS drug-delivery system-on-chip (SoC), in which wireless controller/actuation circuitry and a drug-delivery array are monolithically integrated. This SoC device can be applied for localized diagnosis/therapy of cancers, or the immediate treatment for those predictably subject to a heart attack, by releasing drugs such as nonapeptide leuprolide acetate or nitroglycerin. This system can be implanted by minimally invasive surgery and allows physicians to make non-invasive therapy modification by using the wireless capability.

This wireless drug-delivery device is realized in a standard CMOS technology. The drug reservoirs are fabricated by CMOS compatible post-IC processing and addressable by an on-chip microcontroller unit. An on-off-keying (OOK) wireless circuit is also integrated in the same die for receiving external commands. Upon receiving wireless commands, the drugs can be released into the body by the rupturing of the membranes covering the drug reservoir.

Potentially, this innovation can give every patient a virtual in-body pharmacy that is wirelessly accessed by the attending physician.

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An end to the Energy problem …!

Modern electronics is providing exceptional computational power in an ever-smaller volume. Recent technological achievements enable a move of the present and established nomadic wireless functionality towards emerging wearable, implantable, and structurally-embedded diagnostic sensor systems in the body and elsewhere. To be practically relevant, these systems must be very small and should be able to operate autonomously for a long time (months or even years). On the other hand, as systems continue to shrink, less energy is available on-board and this will reduce the energy autonomy of the system.

To overcome this trend and to radically solve this energy problem for miniature sensor systems, a new energy source paradigm is needed. This new paradigm is energy harvesting (often called energy scavenging) which converts energy from a natural ambient and essentially inexhaustible source such as vibrations, light or temperature differences into electrical energy. Recent technological advances are making this conversion process more and more efficient and, currently, tens to hundreds of microwatts are being harvested by miniature energy harvesters. In principle that should allow powering of wireless sensor elements.

But there is still a hurdle: in contrast to a battery, the electrical output of the harvester is not as well-behaved. It is either too high, too low or variable, and therefore can not be directly used by an electronic system. As a consequence, a power-management circuit for rectification and voltage regulation is needed. But, this circuit draws valuable energy from the system. It should therefore consume only a fraction of the generated power and should be very efficient in its conversion.

At ISSCC 2009, engineers from Massachusetts Institute of Technology (Paper 17.6), University of California, Davis and Agilent Technologies (Paper 17.7), and IMEC (Paper 17.8) are presenting breakthroughs for more-efficient voltage conversion and regulation of the power generated by vibrational, solar and thermal energy harvesters, respectively. The power managers that will be reported are each more efficient, both for rectification (85% peak efficiency) and for regulation (80% peak efficiency), smaller in size (by using a smaller number of passive components, or a fully-integrated solution), and smarter (by being energy aware and able to handle multiple-source inputs) while, at the same time consuming very little power (as low as 0.9μW) on their own.

Recognizing the importance of this new energy-harvesting paradigm, a Special Evening Session is fully devoted to Next-Generation Energy Scavenging Systems.

The exciting developments that will be reported at ISSCC 2009, effectively remove the last hurdle to ubiquitous sensor systems, the energy problem, making energy autonomous sensor systems a practical reality in the next few years.

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Silicon form Safety

Radar techniques used in automotive applications can estimate the distance and speed of other vehicles to prevent accidents and save lives. Automotive radars can also increase driving comfort by automatically controlling the speed and distance between vehicles, a feature known as "Auto-Cruise Control". Regulatory authorities around the world aim at having most vehicles equipped with automotive radar safety features within the next decade. Commercially available automotive radars are typically implemented in GaAs technology. The resulting higher cost, limits the target market to trucks and high-end cars. Silicon technologies and low-cost assembly techniques will enable widespread adoption of automotive radars in mainstream vehicles.

Large bandwidths are typically required for high-resolution ranging. For this reason two wide frequency bands around the world have been allocated for automotive radar applications, 22 to 29 GHz and 77 to 81GHz. Typically radar schemes transmit an appropriate signal, and measure the time-of-flight delay to estimate distance. The transmitted signal can be: (1) A sequence of very short wide-bandwidth UWB pulses, or (2) A constant-amplitude frequency-modulated continuous-wave (FM-CW) signal. In both cases, delivering high output power at these frequencies is a key implementation issue for silicon technologies.

At ISSCC 2009, engineers from UC, Irvine (Paper 18.2) presents a fully integrated pulse-based UWB transceiver targeted for automotive radar applications. The chip, implemented in BiCMOS, includes digital impulse generation and radio front-end transmitter and receiver. The IC generates very short 1ns pulses and transmits them with a state-of-the-art output power of 14dBm at 24GHz to achieve a ranging resolution of 15cm. It also provides multifrequency capability to cover short- and long-range radar requirements at 24 and 77GHz, respectively. This dual-band operation is enabled by a dual-band LNA followed by wide-band mixers and a dual-band frequency synthesizer. This presentation and others in Session 18, highlight the advances in CMOS automotive radar. These advances will enable low-cost solutions that will be available on most cars, improving automotive safety for all.

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Blu-ray Movie Downloads in Seconds!

Today, downloading a Blu-ray movie takes about 10 minutes on a standard wireless LAN connection. With new Gigabit-per-second (Gb/s) wireless it will only take about a minute. This technology will enable new markets such as downloading a movie at a kiosk before boarding a train or plane, or wireless real-time video transmission to a high-definition TV without the need for expensive clumsy cables.

These and similar consumer-market applications are technology drivers for Gb/s communication, but it must be emphasized that such applications are very sensitive to cost. Silicon-based technologies and low-cost package and assembly techniques will be required for enabling widespread adoption of the applications in consumer markets. Fast file downloading might be implemented in a portable device, further requiring low power dissipation for extended battery life.

The extremely-high data-rates required for multimedia applications pose significant challenges for the radio circuitry, module design and baseband processing. Obtaining Gb/s communications requires very-wideband channels. Two possibilities are being explored: (1) Using UWB (ultra-wideband) technology up to 11GHz, which might be sensitive to interference because of low transmitted power requirements, and (2) Exploiting under-utilized bandwidth at 60GHz, which is very challenging for the implementation of the RF section, especially in low-cost digital-oriented CMOS technologies.

At ISSCC 2009, engineers from UC, Berkeley (Paper 18.5) will present a fully- integrated transceiver for up to 5Gb/s wireless communications. The chip is implemented in a low-cost 90nm CMOS process and consumes minimal battery power. For the first time, 60GHz CMOS RF parts integrate all the required radio components such as amplifiers, frequency generation and baseband circuits. It also replaces conventional digital-baseband signal processing with advanced techniques using signal conditioning, and time-domain equalization to minimize power consumption.

Packaging and antenna assembly are among the big remaining challenges in the 60GHz frequency range. Engineers from National Taiwan University (Paper 18.6) will present an interesting approach to integrating a CMOS radio and planar antenna on a low-cost manufacturable 60GHz module.

The advanced integration and high-speed access enabled by the 60GHz CMOS modules presented in this Session will enable extremely fast downloads, and low-cost solutions, opening new markets for wireless Internet applications.

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Amplifiers—Alive and Well!

The rumored death of traditional analog has been greatly exaggerated! Although we think of the world as "going digital", the truth is that traditional analog functions are more important than they ever were. Think about it: What takes the tiny signal from your camera's image sensor and boosts it to the point that digital circuits can even recognize it? What takes the gigabytes of data from your MP3 player and turns them into the current required to drive a loudspeaker or headphones? Airbag sensors? Blu-ray drives? Cell phones? That's right; it's our old friend the analog amplifier! But make no mistake: These are not your father's amplifiers! New solid-state amplifiers go well beyond what was possible only a few years ago! This year, at ISSCC 2009, progress is evident on two fronts: precision and switching.

Precision is required to make accurate measurements and its primary enemy is electronic noise. In one example (Paper 19.1), Dutch engineers at the Delft University of Technology have found a way to get low-frequency noise down to astonishing levels: Compared to a traditional integrated-circuit amplifier, its low-frequency noise is roughly a hundred-thousand times smaller! This enables measurements of unprecedented precision. For example, delicate state-of-the-art manufacturing equipment can be stabilized by measuring temperature of critical components to a resolution of one micro-degree Celsius (about 2 millionths of a degree Fahrenheit).

The second frontier fpr amplifier development is power efficiency. Amplifier designers have recently taken a radical new approach. Instead of a smooth steady output, these new amplifiers periodically short your loudspeaker to the power supply! Why is this good? Incredible efficiency! The output—when filtered—delivers high-quality audio at power efficiencies that are many times higher than in old-style amplifiers. This translates to longer battery life, and smaller lighter equipment. This technology is such a breakthrough that it is already widely used in cell-phone speakers and portable audio devices. The latest generation, referred to as "Class-D" amplifiers, to be highlighted at ISSCC 2009 provide power in a wide range: from 1% of a watt (Paper 26.5) up to 460 watts (Paper 26.6).

Clearly, the venerable amplifier is not dead! Indeed, the research to be presented at ISSCC 2009 will reveal a renaissance in the amplifier, the most fundamental of electronic circuits.

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10Gb/s Keeping Internet Rolling

Use of the Internet is exploding! Both the number of users and the amount of data per user are increasing at a dramatic rate. The continuing boom in demand has created bottlenecks in both its electrical and optical data-delivery systems. This in turn has created an urgent need for the development of small low-use CMOS transceivers operating in the 10-to-40Gb/s range. Such chips must not only handle incredibly difficult environmental conditions, but also do so while consuming less power per bit than ever before.

This year, engineering researchers from around the world will demonstrate their ability to rise to the occasion in the “10Gb/s-to-40Gb/s Transmitters and Receivers” session at ISSCC 2009 in San Francisco, in February 2009.

Key presentations will include one from NEC deserving a fully-integrated 40Gb/s transceiver chipset in 65nm CMOS for optical-transmission systems that consumes only 2.8W (in Paper 21.1) and UC Irvines presentation of an 80mW 40Gb/s feedforward equalizer in 65nm (in Paper 21.4).

The presentations at ISSCC2009 will not only demonstrate that researchers have been able to make CMOS the enabling technology for solving today’s most difficult problems, but also provide insight about how such advances will continue in the future, and how CMOS has found a home at 100Gb/s, and beyond.

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Reconfigurable Radios for Universal Connectivity

Today, users of wireless technology are overwhelmed by an alphabet soup of standards, as well as, disparate and incompatible technology. Many people dream of a single device that would enable universal connectivity and multi-standard operability. The solution to this problem today is to use dedicated transceivers optimized for each standard. But, a mobile device may contain dozens of radios and many ICs in order to offer connectivity to various 2G/3G standards, Wireless LAN and PAN networks. This solution results in a power- and area-hungry device that requires a large battery. As well, most wireless devices are missing a key ingredient, a high-speed low-range connection for data synchronization. If UWB solutions are to fill this gap, there is a need for a low-cost compact transceiver.

With the advances to be presented at ISSCC 2009, one can clearly envision a future where a single integrated circuit replaces the function of dozens of radios today. This single chip can adapt and work with the user as he/she moves from the desktop, where a high-speed UWB transceiver downloads a movie onto the mobile device, to the WiFi network as the user roams in the building, to a WiMax or 4G network as he/she leaves the building and goes to her next appointment, never losing a broadband data connection. While travelling, the radio maintains a WiMedia connection to the automobile to deliver high-quality audio content and a Bluetooth connection for hands-free voice communication. The radio seamlessly switches between various 2G/3G/4G networks since it is a “software defined radio” (SDR). In theory, the radio can even adapt to a new standard, perhaps a specialized standard which is country- or region-specific.

At ISSCC 2009, in San Francisco, two presentations from IMEC and KU Leuven (Paper 24.1) and from NXP Semiconductors and ST-NXP (Paper 24.2) will describe single-chip breakthroughs for full-featured low-cost transceivers. Paper 24.1 presents an SDR that is reconfigured to work with many standards. Compatibility with GSM, DVB-H, LTE, WLAN 11g, WiMAX, and WLAN 11n are demonstrated in a single transceiver front-end. Paper 24.2 presents an inductorless CMOS WiMedia UWB chip that can enable high-data-rate communication while occupying a very small die size, partly through the elimination of inductors in the transceiver.

The flexibility promised by such reconfigurable radio ICs promises an incredible flexibility for consumers in the inceasingly mobile world!

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This amplifier really does go to 11!

- The stereo in your car is a space heater! So is your iPod, your boom box and so on, for pretty well every music source you own.

- Most of the time, when you're listening, 90% of the energy from the battery goes into heat, not sound! It gets more efficient—only 75% goes into heat—if you turn the volume all the way up, but your ears and your neighbors might object! This inefficiency drives up your electricity bill, drives down your battery life, and makes the radios, music players, stereos that you own, larger, heavier, and even more expensive. But it doesn't have to be this way...

- Enter Class-D. Instead of generating a signal that varies continuously to replicate the sound wave, Class-D is a switching amplifier, one whose output is either "on" or "off." The trick is that it switches on and off very very fast, so that on average, the average value is the desired signal. This turns out to be wildly more efficient! In fact, only 5% of the power might go into heat. This makes a huge difference: To provide a 1W output power, you need only 1.05W from the battery, instead of 10W as required by an amplifier with only 10% power efficiency. That's 10 times the battery life!

- But, Class-D was invented decades ago. Why doesn't your stereo use it? Well, it turns out that there's a bit of a catch. All that switching on and off generates electronic noise (engineers and the FCC call it "EMI", or electromagnetic interference), which interferes with... your stereo, your iPod, your cell phone, and your TV. So what to do? You need the switching to get efficiency, but what do you do about the noise?

- The two main sources of the EMI noise in Class-D amplifiers are power-supply overshoot and common-mode noise. The addition of bulky inductor-capacitor (LC) filters and large decoupling capacitors are the traditional defense against EMI noise in these systems. But, recently, a variety of techniques have been demonstrated which attempt to reduce the generation and/or impact of EMI in audio systems.

- Now, it has been shown that by cleverly controlling the switching the EMI noise can be eliminated at the source. Engineers folks at Texas Instruments (ISSCC 2009 in Paper 26.4) have found a way to go "filterless" with a new modulation scheme. Other engineers from NXP (Paper 26.6) will describe an amazing power delivery of 460W in a amplifier without the typical voltage overshoot and reliability problems. Come and see how such new techniques have advanced the state-of-the-art for efficiency, power delivery, and system cost reduction.

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High-Performance and Low-Power Cache with High-κ Metal-Gate Technology at 32nm

At ISSCC 2009 (Paper 27.1), engineers from Intel will present the industry's first 32nm high-performance and low-power SRAM for high-end microprocessor applications. This SRAM memory achieves 4GHz performance at a 1.0V supply for a 291Mb implementation in 32nm silicon.

The combination of advanced high-κ metal-gate technology and advanced power-management schemes enables high-performance and low-power SRAMs. These illustrate an overall SRAM scaling trend-line that continues to follow Moore's Law.

Details of the implementation will be revealed at ISSCC 2009 at the San Francisco Marriott in February.

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Intel Eyes Light for Chip Links!

As microprocessors transition from single processing cores to many cores on a single chip, the demands for moving data onto and off the chip are increasing. Future computing chips will require bandwidths exceeding 1TB/s . (To put this into perspective, this means that chips need to move the equivalent of two copies of the 20-volume Oxford English Dictionary onto or off the chip every second.) Such overwhelming bandwidth requirements will also necessitate new approaches that limit the energy required to send each bit.

Light has long been used for long-distance communication and forms the physical backbone of computer networks, and telecommunications. Increasingly, photons are displacing electrons for shorter and shorter distance communications. The challenge, however, is in integrating the required photonic and electro-optic devices on silicon chips. This year, at ISSCC 2009, engineers from Intel (Paper 28.1) will outline its vision for the future of photonic chip-to-chip interconnects. Initial efforts have focused on hybrid implementations, in which gallium-arsenide lasers and detectors are packaged with silicon transceivers delivering up to 18Gb/s in each optical channel. With an eye to the future, however, Intel will present progress in integrating waveguides, detectors, and modulators directly onto silicon CMOS chips. Such approaches will also allow different wavelengths of light to be employed for additional bandwidth enhancement in a technique known as wavelength-division multiplexing. Integrated germanium detectors will be demonstrated with bandwidths exceeding 35GHz, as well as, polymer-based electro-optic modulators with bandwidths exceeding 10GHz.

Such developments will light the way to future high-performance computing!

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One Step Closer to the Universal Radio

Modern mobile communication systems place ever-increasing requirements on radio receivers for mobile terminals. More and more standards and frequency bands need to be covered, in particular due to the so-called digital dividend. Indeed, the progressive replacement of analog TV systems by digital ones, frees additional frequencies that will be used to extend the capacity and geographic coverage of mobile communication networks. Traditional radio receivers are designed for specific frequencies, and do the processing required for recovering the information in the analog domain. With the advent of low-power and highly integrated digital circuits, it becomes possible to do all the processing in the digital domain, enabling flexibility and programmability. This opens up the prospect of a universal radio receiver, one able to adapt to any standard or frequency band as required by the user. Still, an analog radio front-end close to the antenna is required. It needs to cover a very large frequency range while having improved noise and linearity compared to existing radio receivers. This is the most serious problem to overcome before the universal radio receiver can happen.

This year, at ISSCC 2009 in San Francisco, in February, new front-end architectures will be introduced by engineers from the University of Twente. In their design, selective front-end filters and low-noise preamplifiers are replaced by novel mixers that are able to adaptively cancel the residues of interferers which may corrupt the wanted signal. This is achieved through a multipath architecture and either analog or digital signal recombination. The analog approach shows good performance, but the digital one is even superior. Through advanced algorithms, it is actually possible to estimate the imperfections of the analog front-end, circuits and apply appropriate corrections in the digital domain. The interferer cancellation can be made almost perfect. The front-ends presented cover a frequency range from 400 to 900 MHz while being totally insensitive to interferers from other bands without the need for a pre-filter placed at the antenna input. This development opens real opportunities. In the near future, a radio will be able to address all standards and bands with a single circuit. Immediate benefits will be reduced overall size and cost to the user, while bringing total connectivity everywhere in the world.

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The (RF) Power of CMOS

Power amplifiers are among the most important components in low-cost wireless systems but they are also the most difficult to realise! In handheld systems, battery life is dominated by the efficiency with which RF power can be generated and transmitted through an antenna. The cost of handheld systems, such as mobile phones, is also critical. CMOS circuit techniques are rapidly emerging that enable high efficiency and low cost by combining digital transceivers and power amplifiers on a single chip. One potentially paradigm-changing approach to 4G handheld communications power-generation is presented. In essence the role of the power amplifier has been absorbed by the frequency up-converter, or mixer (now deemed “power-mixer”). Not only is the PA role subsumed, but the function, which previously had been performed with exotic materials such as GaAs, now is done in standard CMOS; this is both cheaper and more easily integrated with the remaining functions in the cellphone.

While efficiently producing power is a critical aspect, getting it out of the antenna is another hot topic. Without good design, mismatches and RF interference substantially increase battery power consumption and reduce delivered power, thus reducing operating range and signal integrity. CMOS-based circuits are proving to be a fruitful means for signal conditioning at the PA-Antenna interface. Novel circuit ideas shown herein enable more efficient coupling and tunable interference protection.

Other highlights of this Session include a CMOS power amplifier for portable UWB systems that can enable firefighters to search for trapped people by looking through the walls of a burning building. Thanks to the commercial availability of the latest process technologies, designers are now able to miniaturize such UWB, amplifiers enabling a variety of applications from mission-critical public safety systems to in-home wireless networks capable of streaming high-definition television programs at 60GHz (for Wireless HDMI).

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Silicon Crosses the 100GHz Barrier

This year's ISSCC features the latest advances in silicon-based technologies that extend mm-wave operation clearly beyond 100GHz. In particular, three amplifiers presented in the Conference break the 100GHz barrier.

Engineers from the University of California, Santa Barbara, in collaboration with IBM Microelectronics, will describe the prototype of an amplifier operating at 150GHz with an output power of 6dBm and a bandwidth of 27GHz (Paper 29.1). Realized in a 65nm digital CMOS process, the circuit consumes only 25.5mW from a 1.1V supply.

Another CMOS amplifier to be described by engineers at the Electronic Circuit Design Laboratory of the Helsinki University of Technology in Finland (Paper 29.2) is centered at 100GHz, and features the highest-reported RF output power at that frequency (+10dBm) and lowest reported noise figure (7.5dB). The amplifier is based on a 65nm CMOS baseline technology and consumes 86mW from a 1.2V supply.

Turning the focus from CMOS to SiGe BiCMOS, engineers from the University of California, San Diego will report (Paper 29.3) a 100GHz "constructive wave" amplifier that has a peak gain of 26dB. The wideband, millimeter-wave amplifier is implemented using a cascaded traveling-wave topology that constructively adds to signal power in the forward path, while canceling backward-traveling signal energy. The amplifier is implemented in 0.12µm SiGe BiCMOS and consumes 82mW from a 2V supply.

Silicon chips enabling circuits and systems for the 60GHz and 77GHz mm-wave bands have already been reported at recent ISSCC Conferences. The potential applications for these circuits are for Gb/s short-range communications and automotive radar. Radio applications beyond 100GHz also include medical imaging systems, and chemical sensing systems. Existing 100GHz implementations rely on GaAs or InP technologies, but silicon is threatening to dominate all but the high-power circuit domains at mm-wave frequencies, as device speeds increase with technology scaling. CMOS provides the added attraction of system-on-a-chip (SoC) integration.

These developments, to be reported at ISSCC 2009, herald the rapid development of Silicon integrated circuits for mm-wave applications.

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